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Question Paper Code : 11287

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

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Third Semester

Electrical and Electronics Engineering

EE3302 – DIGITAL LOGIC CIRCUITS

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compute the binary equivalent for the decimal number 25.
2. Highlight the primary purpose of error detection codes in digital data transmission.
3. Convert the BCD number 1001 to Excess-3 code.
4. Depict the symbol of a 4-bit binary adder.
5. Give out the state table of a 2-bit binary counter.
6. State the next state of a T flip-flop if T = 1 and current state = 0.
7. Define a race condition in asynchronous circuits.
8. Specify the need of flow stability in asynchronous sequential circuits.
9. Propose a VHDL code to implement a 2-input AND gate.
10. Justify the requirement of a test bench in VHDL simulation.

PART B — (5 × 13 = 65 marks)

11. (a) Compare TTL and CMOS families for a 4-bit logic circuit in terms of speed, power consumption, and fan-out.

Or

(b) Minimize $F(A, B, C, D) = \sum(0, 2, 5, 7, 8, 10, 13, 15)$ using K-map and implement the simplified circuit.

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12. (a) Design and implement a BCD to Gray code converter using combinational logic.

Or

(b) Design an 8-to-3 priority encoder with truth table, logic diagram, and Boolean expressions.

13. (a) Design a Moore sequential circuit for a sequence detector that detects 101 patterns with state diagram and table.

Or

(b) Design and implement a serial-in serial-out shift register using D flip-flops.

14. (a) Compare PROM, PLA, and PAL in terms of flexibility, speed, and programming.

Or

(b) Analyze the following asynchronous sequential circuit described by the transition table. Detect whether any race conditions exist. If present, explain the type of race and suggest methods to eliminate it.

Present State (Q1 Q0)	Input X = 0	Input X = 1
00	00	01
01	11	10
10	01	00
11	10	11

15. (a) Design and Develop a VHDL program for D flip-flop with clock and asynchronous reset.

Or

(b) Compare the combinational and sequential circuit modeling in VHDL with an example for each and required diagrams.

PART C — (1 × 15 = 15 marks)

16. (a) Design a traffic light controller using synchronous sequential logic (Moore machine) and provide the necessary state diagram, state table, logic diagram, and timing diagram.

Or

(b) Design an asynchronous sequential circuit for a sequence detector with hazard-free operation. Include flow table and logic diagram.

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