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Reg. No. : E N G G T R E E . C O M

Question Paper Code : 11247

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

Fifth Semester

Electronics and Communication Engineering

EC3552 — VLSI AND CHIP DESIGN

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(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define threshold voltage of a MOS transistor.
2. What is body effect in MOSFET?
3. Define propagation delay in digital circuits.
4. What is a stick diagram?
5. Define pipelining in digital circuits.
6. What is synchronous design circuits?
7. What is the role of capacitance in interconnect delay?
8. What is memory core?
9. Define fault model in VLSI testing.
10. What is scan design?

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PART B — (5 × 13 = 65 marks)

11. (a) Explain the ideal and non-ideal I-V characteristics of MOS transistor with neat diagrams.

Or

(b) Discuss technology scaling in CMOS circuits and analyze its impact on power consumption and performance.

12. (a) Explain the layout design process using stick diagrams and layout diagrams with an example.

Or

(b) (i) Discuss the design and operation of static CMOS logic gates with suitable diagrams. (8)

(ii) A CMOS gate has C_L = 15 pF, V_{DD} = 3.3 V and f = 20 MHz. Evaluate the Power dissipation. (5)

13. (a) Describe the working of dynamic latches and dynamic registers used in VLSI circuits.

Or

(b) Explain the self-timed circuit design approach and compare it with synchronous design.

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14. (a) Explain the interconnect parameters : resistance, capacitance, and inductance and their effects on VLSI circuits.

Or

(b) (i) Design and explain high-speed adders and multipliers used in sequential digital circuits. (7)

(ii) Explain the architecture of memory and its building blocks with neat diagrams. (6)

15. (a) (i) Explain the ASIC design flow from specification to fabrication. (7)

(ii) Model the faults associated with CMOS design. (6)

Or

(b) (i) Describe the wafer-to-chip fabrication process flow in VLSI technology. (6)

(ii) Write and explain a Verilog test bench for testing a digital circuit. (7)

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PART C — (1 × 15 = 15 marks)

16. (a) (i) A digital pipeline processor has 5 stages. Each stage requires 4 ns for processing and the pipeline register delay is 1 ns. Evaluate,

(1) Clock cycle time,

(2) Time required to process 10 instructions without pipelining,

(3) Time required to process 10 instructions with pipelining,

(4) Speedup achieved. (8)

(ii) Realize the function $F = \Sigma m(1, 5, 6, 7)$ using

(1) Pseudo nMOS logic and

(2) Static CMOS logic. (7)

Or

(b) (i) Apply the concept of 3 stage pipelining to $\log(|a_n + b_n|)$ and find the number clock period for $n = 3$ to get the output. (7)

(ii) Generate the test vectors for the combination functions $F = (AB + BC + CD)$ using automatic test pattern generation for the stuck-at-0 fault at node B. (8)

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