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Question Paper Code : 11237

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

Third Semester

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Electronics and Communication Engineering

EC3352 — DIGITAL SYSTEMS DESIGN

(Common to : Electronics Engineering (VLSI Design and Technology)/
Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Using Boolean algebra techniques, simplify the expression:
 $F = A'.B.C + A.B'.C + ABC' + A.B.C$
2. Convert the following Boolean expression into standard SOP form:
 $AB'C + A'B' + ABC'D.$
3. What is parity generator and checker?
4. Differentiate multiplexer and encoder.
5. Differentiate latches and flip-flops.
6. What is the need for counter? Where it is used?
7. Differentiate stable and unstable states.
8. What is a state table?
9. Differentiate Fan-in and Fan-out in the context of logic families.
10. Define noise margin. How does it affect performance?

PART B — (5 × 13 = 65 marks)

11. (a) Simplify the Boolean function $F(w, x, y, z) = \sum(1, 3, 7, 11, 15) + d(0, 2, 5)$, Implement the function using NAND gates only.

Or

- (b) Simplify the Boolean function $F(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 14)$ using tabulation 10 method and draw the logic diagram.
12. (a) Construct the full adder and binary parallel adder with necessary diagrams and truth tables.

Or

- (b) (i) Implement the following functions using de-multiplexer.
 $f_1(A, B, C) = \sum m(1, 5, 7)$, $f_2(ABC) = \sum m(3, 6, 7)$ (6)
- (ii) Design a 2-bit magnitude comparator. (7)
13. (a) (i) Design a master/slave JK flip flop and explain its operation. (6)
- (ii) A sequential circuit with two D flip-flops A and B, one input x , and one output z is specified by the following next state and output equations:
 $A(t+1) = A' + B$, $B(t+1) = B'x$, $z = A + B'$
- (1) Draw the logic diagram of the circuit (2)
- (2) Derive the state table (2)
- (3) Draw the state diagram of the circuit. (3)

Or

- (b) (i) Elucidate the operation of 4-bit ring counter. (6)
- (ii) Design a 4-bit universal shift register. (7)
14. (a) Explain the types of hazards. Implement the following function $F(A, B, C) = \sum(0, 1, 3, 4, 8, 12)$ by a hazard free two level OR-AND gate network.

Or

- (b) What are races? Name the types of races. Show the possible occurrence of races in asynchronous sequential circuits? Provide the solution to overcome the races.

15. (a) (i) Realize the 2-input NAND gate using CMOS logic. (6)
- (ii) Implement the following function using PROM. (7)
- $F1(X, Y, Z) = \sum m(1, 2, 4, 6)$, $F2(X, Y, Z) = \sum m(0, 1, 2, 6, 7)$
 $F3(X, Y, Z) = \sum m(2, 6)$.

Or

- (b) (i) Compare the various logic families (any four) programming digital logic. (8)
- (ii) Differentiate ROM, PROM, EPROM, EEPROM and EAPROM. (5)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a 3 to 8 decoder with 2 to 4 decoder. (7)
- (ii) Design the 8-bit arithmetic and logic unit and explain the operation. (8)

Or

- (b) (i) Design a 4-bit up and down counter using D-flip flop. (7)
- (ii) Design a BCD to Excess 3 code convertor using PLA. (8)