

Reg. No. :

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Question Paper Code : 30039

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

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Second Semester

Computer Science and Engineering

CS25C06 — DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION(Common to : Computer Science and Design/Computer Science and Engineering
(Artificial Intelligence and Machine Learning)/Computer Science and Engineering
(Cyber Security)/Computer Science and Engineering (Data Science)/Computer
Science and Engineering (IoT)/Computer and Communication Engineering/Artificial
Intelligence and Data Science)

(Regulations 2025)

Time : 3 hours

Maximum : 100 marks

CO – Course Outcomes

CO1	Identify basic digital components and their functions in a computer system.
CO2	Apply Boolean algebra and number systems to design simple digital circuits and simulate them using tools.
CO3	Analyze instruction sets, arithmetic units, and performance metrics to evaluate processor design.
CO4	Engage in continuous learning to update with advancements through evolving computing trends.

BL – Bloom's Taxonomy Levels

(L1-Remember, L2-Understand, L3-Apply, L4-Analyze, L5-Evaluate, L6-Create)

Answer ALL questions.

PART – A (Total Marks = 40)**[Q. No. 1 to Q. No. 10 ; $10 \times 1 = 10$ Marks (Multiple Choice Questions)****Q. No. 11 to Q. No. 20; $10 \times 3 = 30$ Marks]**

Q.No.	Questions	Marks	CO	BL
1.	Which Boolean law is represented by the expression $A + AB = A$? (A) Distributive Law (B) Absorption Law (C) De Morgan's Law (D) Associative Law	1	1	2

2.	For an n-variable Karnaugh Map, how many cells (minterms) are present in the grid? (A) $2n$ (B) n^2 (C) 2^n (D) 4^n	1	1	1
3.	What metric is used to measure a computer's floating-point instruction execution speed? (A) MIPS (B) CPI (C) MFLOPS (D) Throughput	1	2	1
4.	If a processor has a Clock Rate of 2GHz and executes instructions with an average CPI of 1.5, what is the MIPS (Million Instructions Per Second) rating? (A) 750 MIPS (B) 1000 MIPS (C) 1333 MIPS (D) 3000 MIPS	1	2	2
5.	Which of the following digital circuits is NOT a combinational circuit? (A) Multiplexer (B) Decoder (C) Full Adder (D) Flip-Flop	1	2	2
6.	Which Flip-Flop is commonly referred to as a "transparent latch"? (A) JK Flip-Flop (B) SR Flip-Flop (C) D Flip-Flop (D) T Flip-Flop	1	3	2
7.	Which type of hazard occurs when two instructions require the same hardware resource simultaneously? (A) Data Hazard (B) Control Hazard (C) Structural Hazard (D) Branch Hazard	1	3	2
8.	Microprogrammed control units are easier to modify because they store control signals in: (A) Flip-flops (B) Control Memory (ROM) (C) Logic Gates (D) ALUs	1	3	3

9.	If a cache is full, which replacement policy removes the block that hasn't been referenced for the longest period of time? (A) FIFO (First-In, First-Out) (B) LFU (Least Frequently Used) (C) LRU (Least Recently Used) (D) Random	1	4	2
10.	Which of the following interface standards is widely used for connecting high-speed solid-state drives (SSDs) and hard drives (HDDs) inside a computer? (A) USB (B) PCI (C) SATA (D) Bluetooth	1	4	2
11.	Define Minterm and Maxterm.	3	1	2
12.	Convert the Boolean expression $F = A + B^1C$ into canonical Sum of Products (SOP) form.	3	1	2
13.	What are the different classes of computers?	3	2	1
14.	Distinguish between Von Neumann and Harvard architecture.	3	2	1
15.	Compare Combinational and Sequential Circuits.	3	2	2
16.	What is Booth's Algorithm?	3	3	2
17.	State the three main types of pipeline hazards.	3	3	2
18.	What is the difference between SIMD and MIMD?	3	3	1
19.	Define DMA.	3	4	2
20.	What is Bus Arbitration?	3	4	2

PART – B (5 × 12 = 60 marks)

Q.No.		Questions	Marks	CO	BL
21.	(a)	Explain the rules for K-Map simplification. Simplify the Boolean function $F(A, B, C, D) = \sum m(0, 2, 3, 8, 10, 11, 12, 14)$ using a Karnaugh Map.	12	1	2
		OR			
	(b)	Detail why NAND and NOR gates are called universal gates. Provide step-by-step logic diagrams showing how to implement all basic gates (AND, OR, NOT) using <i>only</i> NAND gates or <i>only</i> NOR gates.	12	1	2

22.	(a)	Discuss about the various stages of Instruction Execution cycle. Give example.	12	2	5
	OR				
	(b)	Explain about different performance metrics which helps to evaluate how efficiently a computer operates.	12	2	3
23.	(a)	Define a multiplexer and its basic function. Show how a higher-order MUX (e.g., 8-to-1) can be constructed using lower-order MUXes (e.g., 2-to-1).	12	2	3
	OR				
	(b)	(i) Compare SR, JK, D, and T flip-flops. Provide their truth tables, characteristic equations, and excitation tables. (ii) Explain the “race-around” condition in JK flip-flops and how it is resolved using Master-Slave configurations.	6 6	3	2
24.	(a)	Define addressing modes and explain at least five different types with suitable examples and their impact on instruction length.	12	3	4
	OR				
	(b)	Explain the fundamental concept of instruction pipelining. Illustrate a standard five-stage pipeline using a detailed timing diagram for a sequence of instructions.	12	3	3
25.	(a)	Explain about different types of ROM and compare HDD and SSD.	12	4	4
	OR				
	(b)	Discuss about various types of interrupts and brief about how priorities are handled by processors.	12	4	4