Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 90991

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2025.

Fifth Semester

Electronics and Communication Engineering

EC 3552 — VLSI AND CHIP DESIGN

(Common to: Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is channel length modulation?
2. List the components of power consumption in CMOS circuits.
3. State any two advantages of dynamic logic over static logic.
4. What is propagation delay? How it affects the circuit performance?
5. Differentiate static and dynamic latches.
6. What are the differences between synchronous and asynchronous circuits?
7. List the parasitic parameters of interconnects.
8. State the significance of FPGA in VLSI design.
9. What is the role of scan chains in testing?
10. Name the phases in ASIC design flow.

PART B — (5 × 13 = 65 marks)

11. (a) Elucidate the dynamic characteristics of a MOSFET. (13)

Or

(b) (i) Obtain the drain current for the three regions of operation of a MOS transistor. (6)

(ii) What is the need for technology scaling? Discuss the effects of technology scaling on device. (7)

12. (a) (i) Write the effect of Elmore delay model and estimate the Elmore delay for 4–input NAND gate realized using CMOS logic. (6)

(ii) Design and draw the layout diagram of a 2-input NAND gate using CMOS. (7)

Or

(b) (i) Explain the importance of transistor sizing in propagation delay reduction with examples. (6)

(ii) Discuss the sources of power dissipation in CMOS circuits and suggest the low power design strategies. (7)

13. (a) (i) What is metastability in sequential circuits? Show how to handle metastability problem by providing solutions? (6)

(ii) Describe the operation of a dynamic latch with the help of a timing diagram. (7)

Or

(b) (i) Elucidate the timing classification of digital systems with examples. (6)

(ii) Discuss the synchronous design methodology with a case study. (7)

14. (a) (i) Model an interconnect wire using RC parameters and derive the delay expressions. (6)

(ii) Discuss the role of FPGA in prototyping VLSI systems and its internal structure. (7)

Or

(b) (i) Explain the memory peripheral circuitry and its impact on read/write performance. (6)

(ii) Describe different memory building block with a suitable diagram. (7)

15. (a) (i) Describe wafer to chip fabrication process flow. (6)

(ii) Discuss various fault models used in VLSI testing with examples. (7)

Or

(b) (i) Compare the test strategies for embedded cores and SOCs. (6)

(ii) Illustrate the process of Automatic Test Pattern Generation (ATPG) for a combinational circuit. (7)

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a 2-to-1 multiplexer using pass transistor logic, dynamic CMOS logic and static CMOs logic. (7)

(ii) Design a pipelined architecture for the logic: $\log|a_n - b_n|$, where n = 1 2,3,4,5. Find the total clock period to get all the outputs for the given n. (8)

Or

(b) (i) Design a full-adder circuit using PLA. (8)

(ii) Write a test bench in Verilog HDL for a 4-bit adder circuit. (7)