Reg. No. : E N G G T R E E . C O M

Question Paper Code : 90985

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2025.

Fourth Semester

Electronics and Communication Engineering

EC 3451 – LINEAR INTEGRATED CIRCUITS

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the basic structure of a BJT differential amplifier with active load.

2. Define an active load. Why are current sources used as active loads?

3. List any two characteristics of an ideal instrumentation amplifier.

4. Calculate the output voltage of an op-amp based scale changer if the input is 1V and gain is –4.

5. Define transconductance and highlight its role in analog multiplier design.

6. If an analog multiplier IC provides an output of 3V for two inputs V_1 = 1.5V and V_2 = 2V, find the multiplication factor K.

7. Define resolution in a DAC and give its unit.

8. Identify the digital output of a 3-bit flash ADC for analog input of 3.5 V in (0-7 V) range.

9. Mention any two features of the ICL8038 function generator.

10. State the advantages of Low Drop-Out (LDO) regulators.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the internal circuit diagram of the IC 741 and mention the significances of each section. (7)

(ii) Compare and contrast open-loop and closed-loop configurations of operational amplifiers. (6)

Or

(b) With relevant sketches, discuss the working principle of MOSFET-based operational amplifier LF155.

12. (a) (i) Draw the circuit diagram of a Schmitt trigger using op-amp and explain its hysteresis characteristics. (7)

(ii) Design an adder circuit using op-amp for three input voltages $V_1 = 2V$, $V_2 = 1V$ and $V_3 = 1V$. All input resistors are $10k\Omega$ and feedback resistor is $10k\Omega$. Determine the output voltage. (6)

Or

(b) With neat circuit diagram, describe the working of

(i) Peak detector using op-amp. (6)

(ii) Clipper (positive and negative) using op-amp. (7)

13. (a) (i) Design a frequency synthesizer using PLL IC 565 to generate an output of 100 kHz from a reference frequency of 10 kHz. (7)

(ii) Discuss in detail the structure and working of the Gilbert multiplier cell. How does it improve linearity in multiplication? (6)

Or

(b) Elucidate the internal blocks and operation of the basic Phase Locked Loop (PLL) with necessary diagrams.

14. (a) Discuss in detail the working of successive approximation ADC. Draw its internal block diagram and explain each stage of conversion.

Or

(b) With relevant diagram, explain the working of a weighted resistor type DAC. Derive the expression for output voltage and discuss the limitations.

15. (a) (i) Design and explain the working of an astable multivibrator using 555 Timer. (7)

(ii) Discuss the architecture and working principle of the IC723 voltage regulator. (6)

Or

(b) Illustrate the working of a video amplifier and audio power amplifier IC. Compare their bandwidth and typical use cases in electronic systems.

PART C — (1 × 15 = 15 marks)

16. (a) A biomedical application requires signal conditioning of a 10 μV ECG signal. Propose a complete op-amp-based signal conditioning system. Justify each block with reasonable component values, and show how the output becomes suitable for ADC interfacing.

Or

(b) Design a 4-bit DAC using R-2R ladder logic to convert a digital input to analog voltage in a 0 to 5V range. Illustrate the operation for the input '1101'.
