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Reg. No. : E N G G T R E E . C O M

Question Paper Code : 90981

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2025.

Third Semester

Electronics and Communication Engineering

EC 3352 – DIGITAL SYSTEMS DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

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Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. State De Morgan's law.
2. List the disadvantages of K-map.
3. Draw the logic diagram for full adder.
4. Distinguish between encoder and decoder.
5. Differentiate Moore and Mealy machine models.
6. What is the significance counters?
7. What do you mean by unstable state.
8. Define asynchronous sequential circuits?
9. What is the propagation delay of a circuit?
10. For the 4-input NAND gate, what is the fan-in of gate? If the NAND gate output is connected to two combinational function equation, then what is the fan-out of the NAND gate?

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PART B — (5 × 13 = 65 marks)

11. (a) (i) Convert the following Boolean function into Canonical and Standard SoP form. $f = (p+q+r)\cdot(p+q+r')\cdot(p+q'+r)\cdot(p'+q+r)$. (6)

(ii) Simplify the function $F(a, b, c, d) = \sum m(2, 3, 4, 8, 9, 10, 13, 14, 15)$ using K-map and implement the function using NAND gates only. (7)

Or

(b) Simplify using tabulation method for the function $F(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 8, 9, 11, 13, 15)$ and implement using NOR gates only. (13)

12. (a) (i) Design a binary to BCD converter and draw the logic diagram. (7)

(ii) Design a carry look ahead adder and explain the operation. (6)

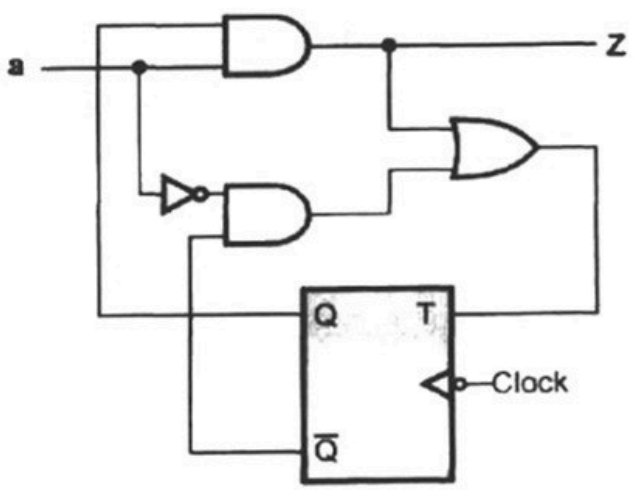
Or

(b) (i) Design a 2-bit magnitude comparator. (6)

(ii) Explain the operation of 4 : 2 encoder and 2 : 4 decoder with illustration. (7)

13. (a) (i) Describe the operation of master/slave flip-flop. (6)

(ii) Analyze the given synchronous sequential circuit. (7)



Or

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(b) (i) Design a 4-bit synchronous ring counter. (6)

(ii) Explain the operation of 4-bit universal shift register. (7)

14. (a) (i) Show how state reduction is performed in asynchronous sequential circuits. (6)

(ii) Define race condition. Provide solution to overcome the race condition. (7)

Or

(b) What are hazards? What are the types of hazards? Design a hazard free circuits. (13)

15. (a) Describe the TTL and CMOS logic families with necessary circuit diagram. (13)

Or

(b) (i) Elucidate the PLA architecture suitable for digital system design. (6)

(ii) Differentiate ROM and RAM? Explain the different types of ROM used in digital systems. (7)

PART C — (1 × 15 = 15 marks)

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16. (a) (i) Design the 8-bit arithmetic and logic unit. (7)

(ii) Realize the following expressions using PROM (8)

$F1(a, b, c) = \sum m(0, 1, 2, 3, 5, 7)$, $F2(a, b, c) = \sum m(1, 4, 5, 6)$.

Or

(b) (i) Implement the following Boolean functions using the PAL device for the following function :

$W(A, B, C, D) = \sum m(1, 12, 13)$

$X(A, B, C, D) = \sum m(2, 7, 8, 11, 12, 13, 14, 15)$

$Y(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 8, 10, 12, 14)$

$Z(A, B, C, D) = \sum m(2, 3, 4, 8, 12, 13)$ (7)

(ii) Design a rolling display using synchronous sequential circuits. (8)

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