EC 3451/ LINEAR INTEGRATED CIRCUITS

UNIT I

BASICS OF OPERATIONAL AMPLIFIERS

Syllabus:

Current mirror and current sources, Current sources as active loads, Voltage sources, Voltage References, BJT Differential amplifier with active loads, Basic information about op-amps – Ideal Operational Amplifier - General operational amplifier stages -and internal circuit diagrams of IC 741, DC and AC performance characteristics, slew rate, Open and closed loop configurations, JFET operational amplifiers-LF 155 and TL082.

1.1. CURRENT MIRROR (CONSTANT CURRENT SOURCE)

Q1. Draw and explain the circuit diagram of a basic current mirror. [Nov 003]

Q2. Explain the working of constant current source with a circuit diagram. [May 2005, Nov 006]

Q3. Draw the circuit of simple bipolar transistor current source and show that its output current is dependent on the β of the transistor. [May 2007, Nov 2009]

Definition:

A circuit in which the output current is equal to input current is called **current mirror.**

In current mirror circuit, the output current is the mirror image of the input current.

Circuit Diagram:

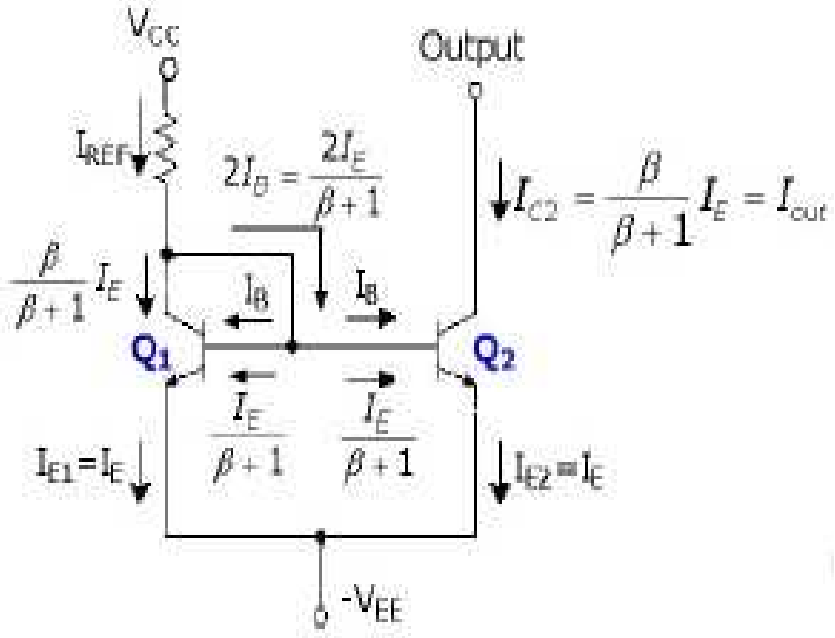


Fig. Current mirror circuit

Explanation:

- ✓ A constant current source uses the transistor in the active mode of operation.
- ✓ The collector current is independent of the collector voltage.
- ✓ Transistors Q_1&Q_2 are matched.
- ✓ The circuit is fabricated using IC technology.
- ✓ Base and emitter of Q_1& Q_2 are tied together and have the same V_{BE}.
- ✓ Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}.
- ✓ As long as Q_2 is maintained in the active region, its collector current $I_{C2}=I_{out}$ will be approximately equal to I_{ref}.
- ✓ Since the output current Io is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

Analysis:

- ✓ If the effect of finite β is considered, this may lead to an output current not equal to the input reference current, since

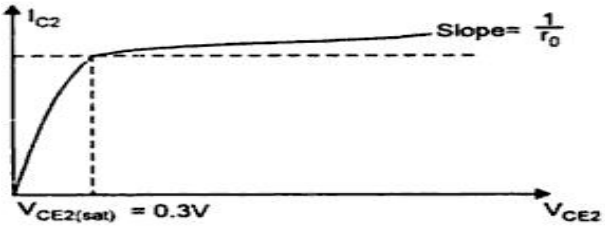
where the expression for I_{REF} is found by using KCL at the collector of Q1.

- ✓ The current gain of the current mirror is

$$\frac{I_{out}}{I_{REF}} = \frac{\beta}{\beta + 2},$$

which approaches unity for β very large.

Current source output current characteristics



Disadvantage:

The output resistance of the current mirror is limited by the r_o of Q_2,

$$r_o = \frac{V_A}{I_{out}} \approx \frac{V_A}{I_{REF}}.$$

1.2 CURRENT SOURCES

Current Source:

Definition:

A circuit which generates current is known as **current source.**

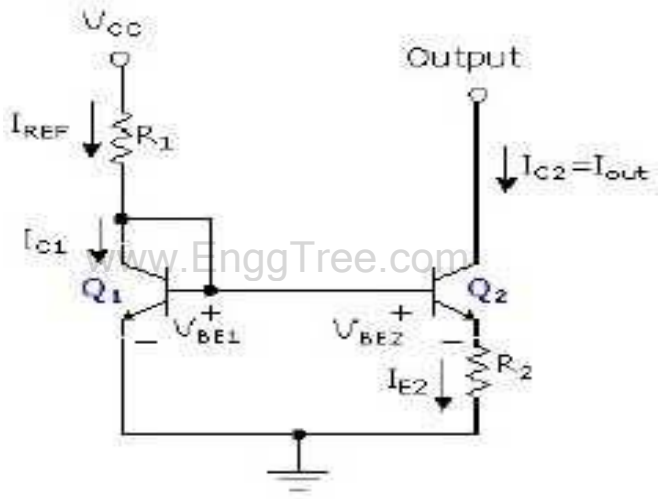
Types of current sources:

1. Widlar current source
2. Wilson current source

1. Widlar Current Source

Q. Draw the circuit of widlar current source and derive an expression for its output current. [May 2006, Nov 2007, May 2008, Nov 2008]

Circuit Diagram:



Explanation:

- ✓ In the Widlar current source, resistor (R_2) is added to the emitter circuit of transistor Q_2.
- ✓ Since multistage amplifier systems have high gain, bias currents must be small.
- ✓ The Widlar current source generates small constant currents using relatively small resistors.

Analysis:

$$I_C = I_0 e^{\left(\frac{V_{BE}}{V_T}\right)},$$

- ➢ Where, Io is the reverse saturation current,
- ➢ VT is the thermal voltage (kT/q≈26mV at room temperature)

Solving Equation for VBE, we get

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_O}\right).$$

✓ We can express VBE1 and VBE2 in the circuit as,

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_O}\right) \cong V_T \ln\left(\frac{I_{REF}}{I_O}\right); \quad V_{BE2} = V_T \ln\left(\frac{I_{C2}}{I_O}\right) = V_T \ln\left(\frac{I_{out}}{I_O}\right).$$

✓ Assuming we have matched devices, V_T and I_O are the same for Q_1 and Q_2.

✓ Subtracting VBE2 from VBE1, and using the appropriate property of logarithms (i.e., lnA-lnB=ln(A/B)),

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{REF}}{I_{out}}\right).$$

✓ Writing a KVL around the base loop of the two transistors,

$$V_{BE1} = V_{BE2} + I_{E2}R_2; \text{ or } V_{BE1} - V_{BE2} = I_{E2}R_2$$

✓ Assuming that $IC_2=IE_2=Iout$, and using our expression for V_{BE1}-V_{BE2},

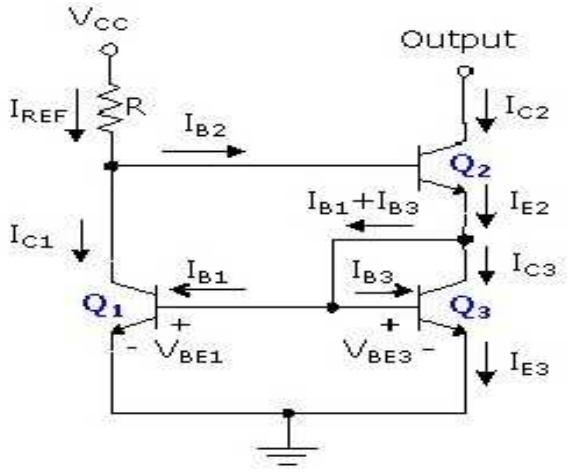
$$I_{out}R_2 = V_T \ln\left(\frac{I_{REF}}{I_{out}}\right).$$

✓ Since I_{REF} (=IC_1) is usually defined in design can be solved for the required value of R_2.

2. <u>Wilson Current Source</u>

Q. With neat diagram explain Wilson current source. [Nov 2009]

<u>Circuit Diagram</u>



Explanation:

- ✓ Another current source configuration that possesses increased output resistance is the Wilson current source.
- ✓ The increased r_o of the Wilson current source is due to the negative feedback provided by Q_3.
- ✓ It provides an output current Io which is very nearly equal to V_{ref} and also exhibits a very high output resistance.

Analysis:

- ✓ Writing a KCL equation at the emitter of Q2

$$I_{E2} = I_{C3} + I_{B1} + I_{B3}.$$

- ✓ If all three transistors are matched $V_{BE1}=V_{BE2}=V_{BE3}$, $\beta_1=\beta_2=\beta_3$, $I_{B1}=I_{B3}$, and $I_{C1}=I_{C3}$.
- ✓ Tthe relationship between base and collector currents ($I_B=I_C/\beta$).
- ✓ We can rewrite the expression for I_{E2} as

$$I_{E2} = I_{C3}\left(1+\frac{2}{\beta}\right).$$

- ✓ Using $I_{C2}=\alpha I_{E2}=\beta I_{E2}/(\beta+1)$ and simplifying,

$$I_{C2} = \frac{I_{C3}(1+2/\beta)\beta}{\beta+1} = \frac{I_{C3}(\beta+2)}{(\beta+1)}.$$

- ✓ Now, if we sum the currents at the base of Q_2,

$$I_{C1} = I_{C3} = I_{REF} - I_{B2} = I_{REF} - I_{C2}/\beta.$$

- ✓ Solving for I_{C2}, we get an expression for the output current (I_{C2}) in terms of the transistor parameter β and the input current, I_{REF}

$$I_{C2} = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} I_{REF} = \left(1-\frac{2}{\beta^2+2\beta+2}\right) I_{REF}$$

- ✓ For reasonable values of β, the second term will be negligible and $I_{C2}=I_{out}=I_{REF}$.
- ✓ Therefore, in addition to the increased output resistance, the Wilson configuration provides an output that is almost independent of the internal transistor characteristics.

1.3. CURRENT SOURCES AS ACTIVE LOADS

- ✓ The current source can be used as an active load in both analog and digital IC's.
- ✓ The active load realized using current source in place of the passive load (i.e. a resistor) in the collector arm of differential amplifier.
- ✓ The active load used to achieve high voltage gain without requiring large power supply voltage.

1.4. VOLTAGE SOURCES

Q. Explain the voltage sources with neat circuit diagram.

Definition:

A **voltage source** is a circuit that produces an output voltage V_0, which is independent of the load.

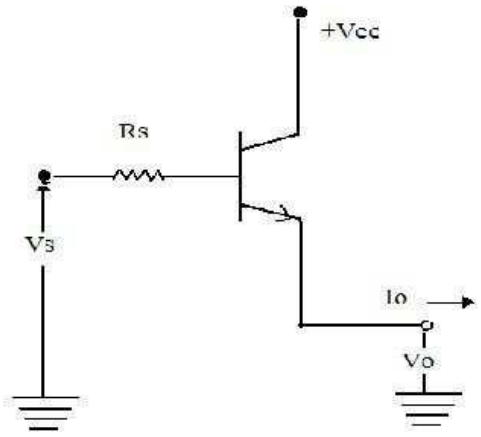
Methods:

There are four methods used to produce a voltage source, namely,

1. Voltage source circuit using Impedance transformation:
2. Emitter– follower or Common Collector Type Voltage source:
3. Voltage source using breakdown voltage of the base- emitter junction
4. Voltage Source using VBE as a reference:

1. Voltage source circuit using Impedance transformation:

Circuit Diagram:



Explanation:

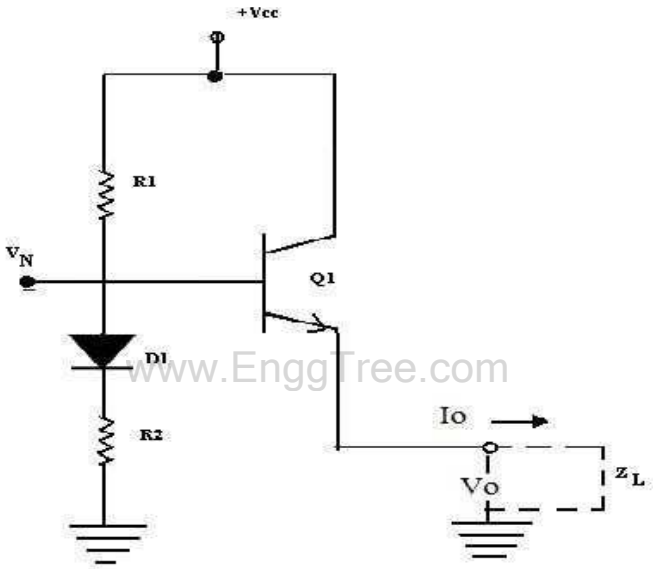
- ✓ The voltage source circuit using the impedance transforming property of the transistor is shown in figure.
- ✓ The source voltage Vs drives the base of the transistor through a series resistance R_S.
- ✓ The output is taken across the emitter.
- ✓ From the circuit, the output ac resistance looking into emitter is given by

$$R_0 = \frac{R_s}{\beta+1} + r_{eb} \; ; \quad \text{With } \beta >> 100, \quad R_0 = \frac{R_s}{\beta+1}$$

- ✓ Equation is applicable only for small changes in the output current.
- ✓ The load regulation parameter indicates the changes in V_o resulting from large changes in output current I_o.
- ✓ Reduction in V_o occurs as Io goes from no-load current to full-load current and this factor determines the output impedance of the voltage sources.

2.Emitter– follower or Common Collector Type Voltage source:

Circuit Diagram:



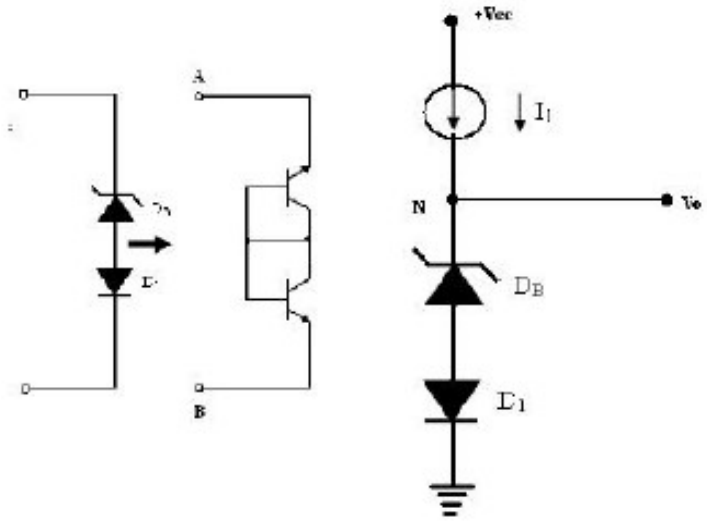
Explanation:

- ✓ The figure shows an emitter follower or common collector type voltage source.
- ✓ Thisvoltage source is suitable for the differential gain stage used in op-amps.
- ✓ The low output impedance of the common-collector stage simulates a low impedance voltage source with an output voltage level of Vo represented by

$$V_0 = V_{CC} \frac{R_2}{R_1 + R_2}$$

- ✓ The diode D_1 is used for offsetting the effect of dc value V_{BE} , across the E-B junction of the transistor.
- ✓ For compensating the temperature dependence of V_{BE} drop of Q1.
- ✓ The load Z_L shown in dotted line represents the circuit biased by the current through Q_1.

- ✓ The impedance R_0 looking into the emitter of Q_1 derived from the hybrid π model is given by



- ✓ The voltage source using common collector stage has the limitations of its weakness for changes in bias voltage V_N.
- ✓ The output voltage V_o with respect to changes in supply voltage Vcc.
- ✓ This is overcome in the voltage source circuit using the breakdown voltage of the base- emitter junction.
- ✓ The emitter – follower stage of common – collector is eliminated in this circuit, since the impedance seen looking into the bias terminal N is very low.
- ✓ The current source I_1 is normally simulated by a resistor connected between Vcc and node n.
- ✓ Then, the output voltage level V_0 at node N is given by $V0 = V_B + V_{BE}$ Where V_B is the breakdown voltage of diode D_B and V_{BE} is the diode drop across D_1.
- ✓ The breakdown diode D_B is normally realized using the base-emitter junction of the transistor.
- ✓ The diode D_1 provides partial compensation for the positive temperature coefficient effect of V_B.
- ✓ In a monolithic IC structure, D_B and D_1 can be conveniently realized as a single transistor with two individual emitters as shown in figure.

Advantages:

1. Producing low ac impedance and
2. Resulting in effective decoupling of adjacent gain stages.

3.Voltage source using breakdown voltage of the base- emitter junction

- ✓ The structure consists of composite connection of two transistors which are diode connected back-to back.
- ✓ Since the transistors have their base to collector terminals common, they can be designed as a single transistor with two emitters.

- ✓ The output resistance R_0 looking into the output terminal in figure is given by

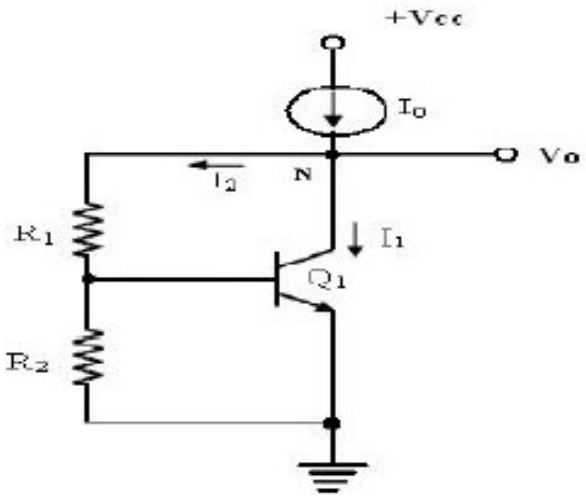
$$Ro=R_B+V_T/ I_1$$

- ✓ where R_B and V_T / I_1 are the ac resistances of the base–emitter resistance of diode D_B and D_1 respectively.
- ✓ Typically, R_B is in the range of 40Ω to 100Ω, and V_0 in the range of 6.5V to 9V.

4.Voltage Source using VBE as a reference:

- ✓ The output stage of op-amp requires stabilized bias voltage source, which can be obtained using a forward-biased diode connected transistor.
- ✓ The forward voltage drop for such a connection is approximately 0.7V, and it changes slightly with current.
- ✓ When a voltage level greater than 0.7V, is needed, several diodes can be connected in series, which can offer integral multiples of 0.7V.
- ✓ Alternatively, the figure shows a multiplier circuit, which can offer voltage levels that need not be integral multiplied of 0.7V.
- ✓ The drop across R2 equals VBE drop of Q1. Considering negligible base current for Q1, current through R2 is the same as that flowing through R1.
- ✓ Therefore, the output voltage V_0 can be expressed as

$$V_0 = I_2(R_1 + R_2) \approx \frac{V_{BE}}{R_2}(R_1 + R_2) \approx V_{BE}(\frac{R_1}{R_2} + 1)$$



- ✓ Hence, the voltage V_0 can be any multiple of V_{BE} by properly selecting the resistors R_1 and R_2.
- ✓ Due to the shunt feedback provided by R_1, the transistor current I_1 automatically adjusts itself, towards maintaining I_2 and V_0 relatively independent of the changes in supply voltage.

- ✓ The ac output resistance of the circuit R_0 is given by,

$$R_O = \frac{dV_0}{dI_0} = \frac{R_1+R_2}{1+g_m R_2} \approx \frac{(R_1+R_2)}{R_2 g_m} \quad \text{When } g_m R_2 >> 1$$

$$R_O = \frac{V_0}{V_{BE}} \frac{1}{g_m} = \frac{V_O}{V_{BE}} \frac{V_1}{I_C} \quad \text{as } \frac{V_O}{V_{BE}} = \frac{(R_1+R_2)}{R_2}$$

1.5. Voltage References

Q. Explain the voltage references with neat circuit diagram.

Definition:

- ✓ The circuit that is designed for providing a constant voltage independent of changes in temperature is called a **voltage reference**.

Concepts:

- ✓ The most important characteristic of a voltage reference is the temperature coefficient reference voltage TCR, and it is expressed as

$$T_{CR} = \frac{dV_R}{dT}$$

- ✓ Reference voltage must be independent of any temperature change.
- ✓ Reference voltage must have good power supply rejection which is as independent of the supply voltage.
- ✓ Output voltage must be as independent of the loading of output current.
- ✓ The circuit should have low output impedance.
- ✓ The voltage reference circuit is used to bias the voltage source circuit, and the combination can be called as the voltage regulator.
- ✓ The basic design strategy is producing a zero TCR at a given temperature, and thereby achieving good thermal ability.
- ✓ Temperature stability of the order of 100ppm/^{0}C is typically expected.

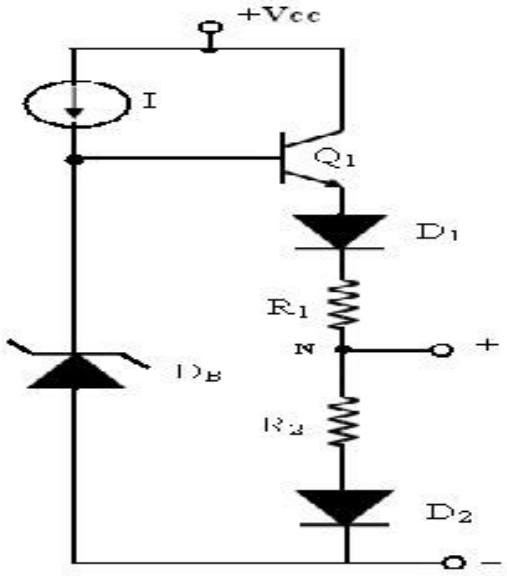
Methods:

There are two methods.

1. Voltage Reference circuit using Avalanche Diode Reference:
2. Voltage Reference circuit using temperature compensation scheme

1. Voltage Reference circuit using temperature compensation scheme:

Circuit Diagram:



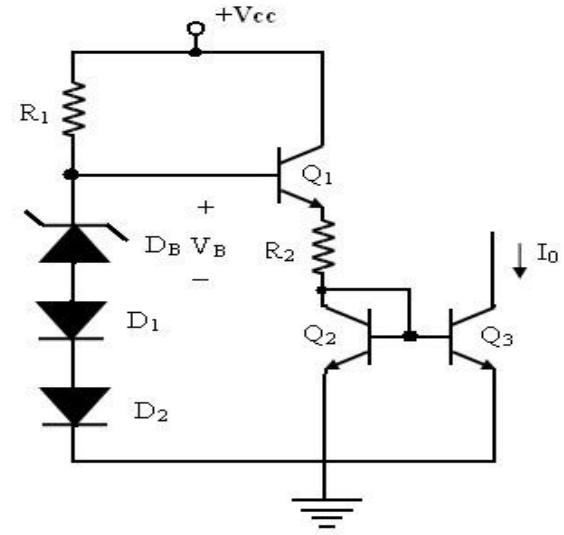
Explanation:

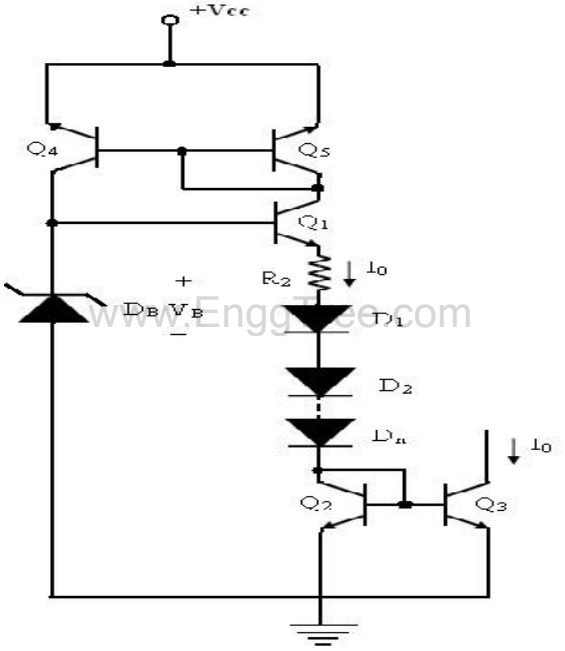
- ✓ This design utilizes the close thermal coupling achievable among the monolithic components.
- ✓ This technique compensates the known thermal drifts by introducing an opposing and compensating drift source of equal magnitude.

- ✓ A constant current I is supplied to the avalanche diode D_B and it provides a bias voltage of $V_{B\,to}$ the base of Q_1.
- ✓ The temperature dependence of the V_{BE} drop across Q_1 and those across $D_{1\,and}$ D_2 results in respective temperature coefficients.
- ✓ Hence, with the use of resistors R_1 and R_2 with tapping across them at point N compensates for the temperature drifts in the base- emitter loop of Q_1.
- ✓ This results in generating a voltage reference V_R with normally zero temperature coefficient.

2. Voltage Reference circuit using Avalanche Diode Reference:

Circuit Diagram





Explanation:

- ✓ A voltage reference can be implemented using the breakdown phenomenon condition of a heavily doped PN junction.
- ✓ The Zener breakdown is the main mechanism for junctions, which breakdown at a voltage of 5V or less.
- ✓ For integrated transistors, the base-emitter breakdown voltage falls in the range of 6 to 8V.
- ✓ Therefore, the breakdown in the junctions of the integrated transistor is primarily due to avalanche multiplication.
- ✓ The avalanche breakdown voltage V_B of a transistor incurs a positive temperature coefficient, typically in the range of 2mV/0 C to 5mV/^{0}C.

- ✓ The base bias for transistor Q1 is provided through register R1 and it also provides the dc current needed to bias DB, D1 and D2.
- ✓ The voltage at the base of Q_1 is equal to the Zener voltage V_B added with two diode drops due to D_1 and D_2.
- ✓ The voltage across R_2 is equal to the voltage at the base of Q_1 less the sum of the base – emitter voltages of Q_1 and Q_2.
- ✓ Hence, the voltage across R2 is approximately equal to that across DB = VB. Since Q2 and Q3 act as a current mirror circuit, current I_0 equals the current through R2.

$$I_O = \frac{V_B}{R_2}$$

- ✓ It shows that, the output current Io has low temperature coefficient, if the temperature coefficient of R2 is low, such as that produced by a diffused resistor in IC fabrication.
- ✓ The zero temperature coefficients for output current can be achieved, if diodes are added in series with R2, so that they can compensate for the temperature variation of R2 and V_B.
- ✓ The temperature compensated avalanche diode reference source circuit is shown in figure.
- ✓ The transistor Q4 and Q5 form an active load current mirror circuit. The base voltage of Q1 is the voltage VB across Zener DB.
- ✓ Then, VB = (VBE * n) +VBE across Q1 + VBE across Q2 + drop across R2. Here, n is the number of diodes.
- ✓ It can be expressed as

$$V_B = (n+2)\, V_{BE} + I_0 * R_2$$

- ✓ Differentiating for V_B, I_0, R2 and VBE partially, with respect to temperature T, we get

$$\frac{\partial V_B}{\partial T} = n + 2\frac{\partial V_{BE}}{\partial T} + R_2\frac{\partial I_0}{\partial T} + I_0\frac{\partial R_2}{\partial T}$$

- ✓ Dividing throughout by I0 R2, we get

$$\frac{I}{I_0}\frac{\partial I_O}{\partial T} = 0 = \frac{1}{R_2 I_0}\left[\frac{\partial V_B}{\partial T} - (n+2)\frac{\partial V_{BE}}{\partial T} - \frac{1}{R_2}\frac{\partial R_2}{\partial T}\right.$$

- ✓ Therefore, zero temperature coefficient of I0 can be obtained, if the above condition is satisfied.

1.6. DIFFERENTIAL AMPLIFIER

Q.Explain the operation of basic differential amplifier. [May 2005]

Definition:

An amplifier that is used to amplify the difference between two signals is known as **differential amplifier.**

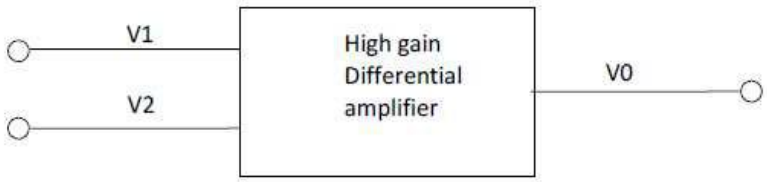
- ✓ This forms the basic input stage of an integrated amplifier.
- ✓ The basic differential amplifier has the following important properties.

1. Excellent stability
2. High versatility and
3. High immunity to interference signals

Advantages

1. Lower cost
2. Easier fabrication as IC component and closely matched components.

Block Diagram:



- ✓ The above figure shows the basic block diagram of a differential amplifier, with two input terminals and one output terminal.
- ✓ The output signal of the differential amplifier is proportional to the difference between the two input signals. V0 = Adm (V1 – V2)
- ✓ If V1 = V2, then the output voltage is zero.
- ✓ A non-zero output voltage V0 is obtained when V1 and V2 are not equal.
- ✓ The difference mode input voltage is defined as Vm = V1 – V2
- ✓ The common mode input voltage is defined as

$$V_{CM} = \frac{V1+V2}{2}$$

- ✓ If V1 = V2, then the differential mode input signal is zero and common mode input signal is Vcm = V1 =V2.

1.6.1. DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD:

Q.Draw the circuit of a differential amplifier with current mirror load. Drive an expression for its gain. (May 2007, Dec 2018, May 2018) [Nov/Dec 2022]

- ✓ Differential amplifier is designed with active loads to increase the differential mode voltage gain.
- ✓ The open circuit voltage gain of an op-amp is needed to be as large as possible.
- ✓ This is got by cascading the gain stages which increase the phase shift.
- ✓ The gain can be increased by using large values of collector resistance.
- ✓ For such a circuit, the voltage gain is given by Adm = gm Rc
- ✓ To increase the gain the Ic Rc product must be made very large.

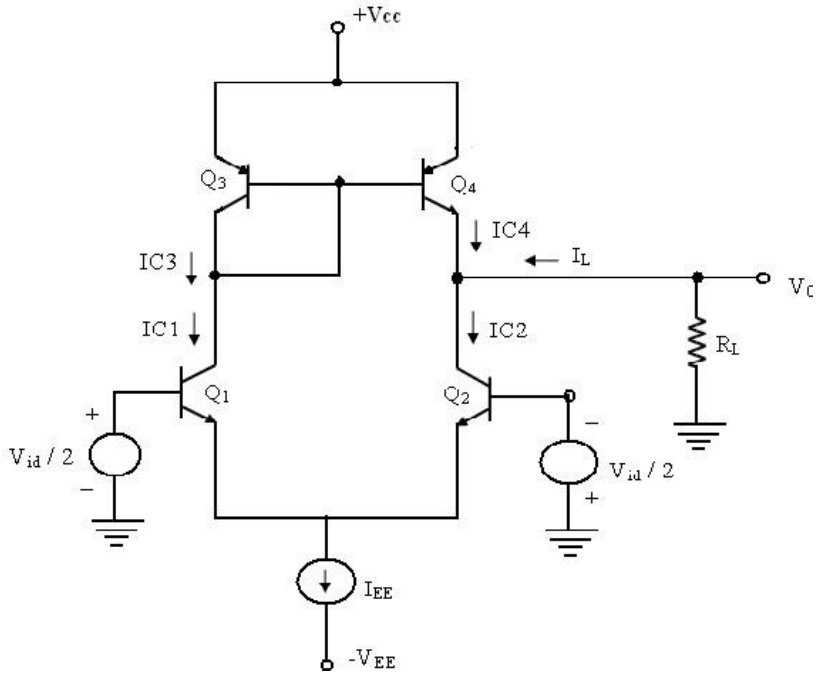
Limitations in IC fabrication

1. A large value of resistance needs a large chip area.
2. For large RC, the quiescent drop across the resistor increased.
3. A large power supply will be required to maintain a given operating current.
4. Large monolithic resistor introduces large parasitic capacitances which limits the frequency response of the amplifier.
5. For linear operation of the differential pair, the devices should not be allowed to enter into saturation.

- ✓ This limits the max input voltage that can be applied to the bases of transistors Q1 and Q2 the base-collector junction must be allowed to become forward-biased by more than 0.5V.
- ✓ The large value of load resistance produces a large dc voltage drop (IEE / 2) Rc, so that the collector voltage will be VC=Vcc - (IEE/2) RC and it will be substantially less than the supply voltage Vcc.
- ✓ This will reduce the input voltage range of the differential amplifier.
- ✓ Due to the reasons cited above, an active load is preferred in the differential amplifier configurations.

BJT Differential Amplifier using active loads:

- ✓ A simple active load circuit for a differential amplifier is the current mirror active load as shown in figure.



- ✓ The active load comprises of transistors Q3 and Q4 with the transistor Q3 connected as a Diode with its base and collector shorted. The circuit is shown to drive a load RL.
- ✓ When an ac input voltage is applied to the differential amplifier, the various currents of the circuit are given by IC4 = IC3 = IC1 = gmVid/2, where IC4 = IC3 due to current mirror action. IC2 = - gmVid/2 .
- ✓ We know that the load current IL entering the next stage is

  IL= IC2-IC4 = - gmVid/2 - gmVid/2 = - gmVid
- ✓ Then, the output voltage from the differential amplifier is given by V0= - ILRL = $g_m R_L V_{id}$.
- ✓ The ac voltage gain of the circuit is given by

$$A_V = \frac{V_0}{V_{id}} = g_{mR_L}$$

- ✓ The amplifier can amplify the differential input signals
- ✓ It provides single-ended output with a ground reference since the load RL is connected to only one output terminal.
- ✓ This is made possible by the use of the current mirror active load.
- ✓ The output resistance Ro of the circuit is that offered by the parallel combination of transistors Q2 (NPN) and Q4 (PNP). It is given by Rr = ro2 || ro4

Analysis of BJT differential amplifier with active load:

- ✓ The collector currents of all the transistors are equal. IC1 = IC2 = IC3 =IC4 = IEE/2 .

- ✓ The Collector -emitter voltages of Q1 and Q2 are given by

  VCE1-VCE2 =VC-VE=V CC - VEB-(-VEB)= VCC

- ✓ Equation shows that, the offset is higher than that of a resistive loaded differential amplifier A.
- ✓ This can be reduced by the use of emitter resistors for Q 3 and Q 4 , and a transistor Q5 in the current mirror load.

Common Mode Rejection Ratio (CMRR)

- ✓ **CMRR** is defined as the ratio of differential mode gain to the common mode gain.
- ✓ The common mode rejection ratio is a measure of the differential amplifier's ability to reject the common mode signal and amplify the differential mode signal.

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{v_{o1}/v_{id}}{v_{o1}/v_{ic}}\right| = \frac{\frac{g_{m1}R_C}{2}}{\frac{\beta_{o1}R_C}{r_{\pi 1}+(1+\beta_{o1})2R_{EE}}} \approx g_{m1}R_{EE} = \frac{I_{EE}R_{EE}}{2V_t}$$

- ✓ Thus, the larger the input trans conductance or REE, the larger the common mode rejection ratio.

Input common-mode range (ICMR)

The **input common-mode range** is the range of common-mode voltages over which the differential amplifier continues to sense and amplify the difference signal with the same gain.

Typically, the ICMR is defined by the common-mode voltage range over which all MOSFETs remain in the saturation region and all BJTs remain in the active region.

Output offset voltage (VOS(out))

The **output offset voltage** is the voltage which appears at the output of the differential amplifier when the input terminals are connected together.

Input offset voltage (VOS(in) = VOS)

The input offset voltage is equal to the output offset voltage divided by the differential voltage gain.

$$V_{OS} = \frac{V_{OS}(\text{out})}{A_{VD}}$$

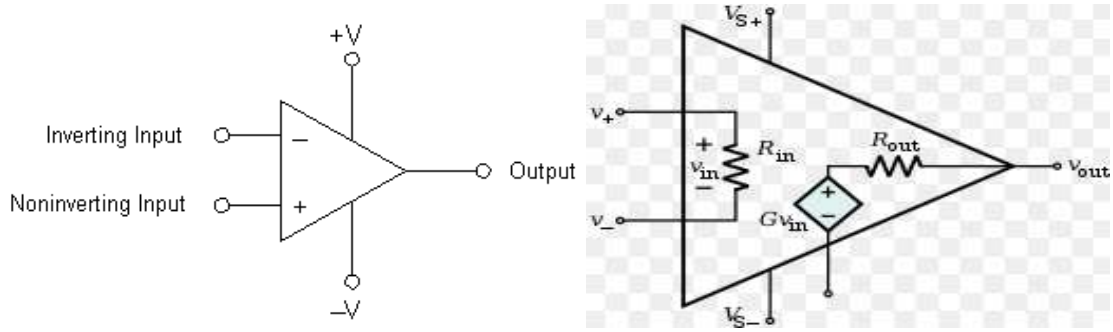
1.7.BASIC INFORMATION ABOUT OPERATIONAL AMPLIFIERS

Q. Explain about Ideal Op-amp in detail. [May 2018)

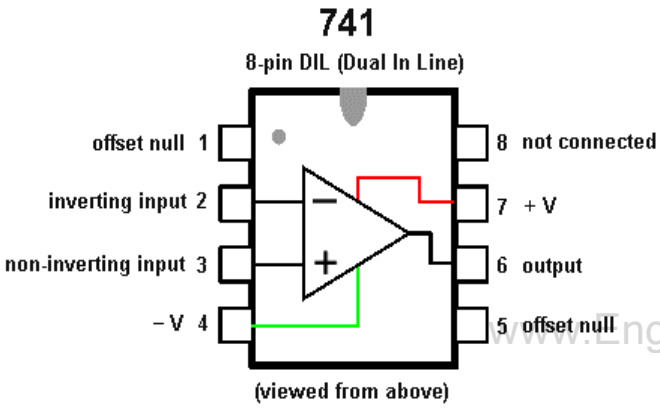
- ✓ An operational amplifier is a direct coupled high gain amplifier.
- ✓ It consists of one or more dfferential amplifiers, followed by a level translator and an output stage.
- ✓ It is a versatile device.

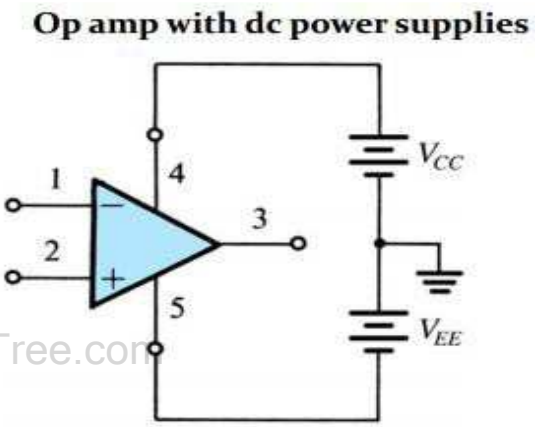
✓ It is used to amplify ac as well as dc input signals & designed for computing mathematical functions such as addition, subtraction, multiplication, integration & differentiation.

Symbol:



Pin Configuration:





Ideal characteristics of O P A M P

1. Open loop gain infinite
2. Input impedance infinite
3. Output impedance zero
4. Bandwidth infinite
5. Zero offset, ie, Vo=0 when V1=V2=0

Ideal Vs Practical Op-Amp

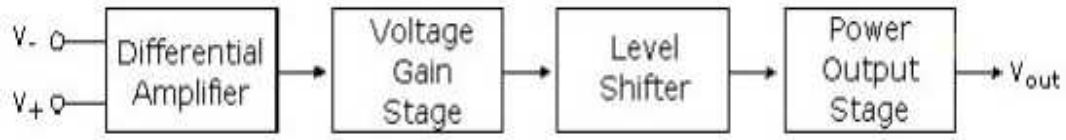
Parameter	Ideal	Practical
Open Loop gain *A*	$\propto$	10^5
Bandwidth *BW*	$\propto$	10-100Hz
Input Impedance Z_{in}	$\propto$	>1MΩ

Output Impedance Z_{out}	0 Ω	10-100 Ω
Output Voltage V_{out}	Depends only on $V_d = (V_+ - V_-)$ Differential mode signal	Depends slightly on average input $V_c = (V_+ + V_-)/2$ Common- Mode signal
CMRR	∝	10-100dB

1.8. GENERAL OPERATIONAL AMPLIFIER STAGES

Q1. Explain the general stages of op-amp with block diagram.

Q2. Draw and explain the block diagram of an op amp. Discuss the functions of each stage in detail.[Nov/Dec 2021] [Nov/Dec 2022]



1. **Input stage:**

- ✓ The input stage, or **differential amplifier**, provides the common-mode rejection to op-amp operation.
- ✓ It also supplies the large input impedance.
- ✓ It allows coupling to a high impedance source without loss of signal level.
- ✓ The differential amplifier may also provide voltage gain if the output of the differential amplifier is connected to an emitter follower with a large emitter resistor.
- ✓ The Emitter Follower amplifier will provide a high impedance load to the differential amplifier to obtain a high voltage gain.

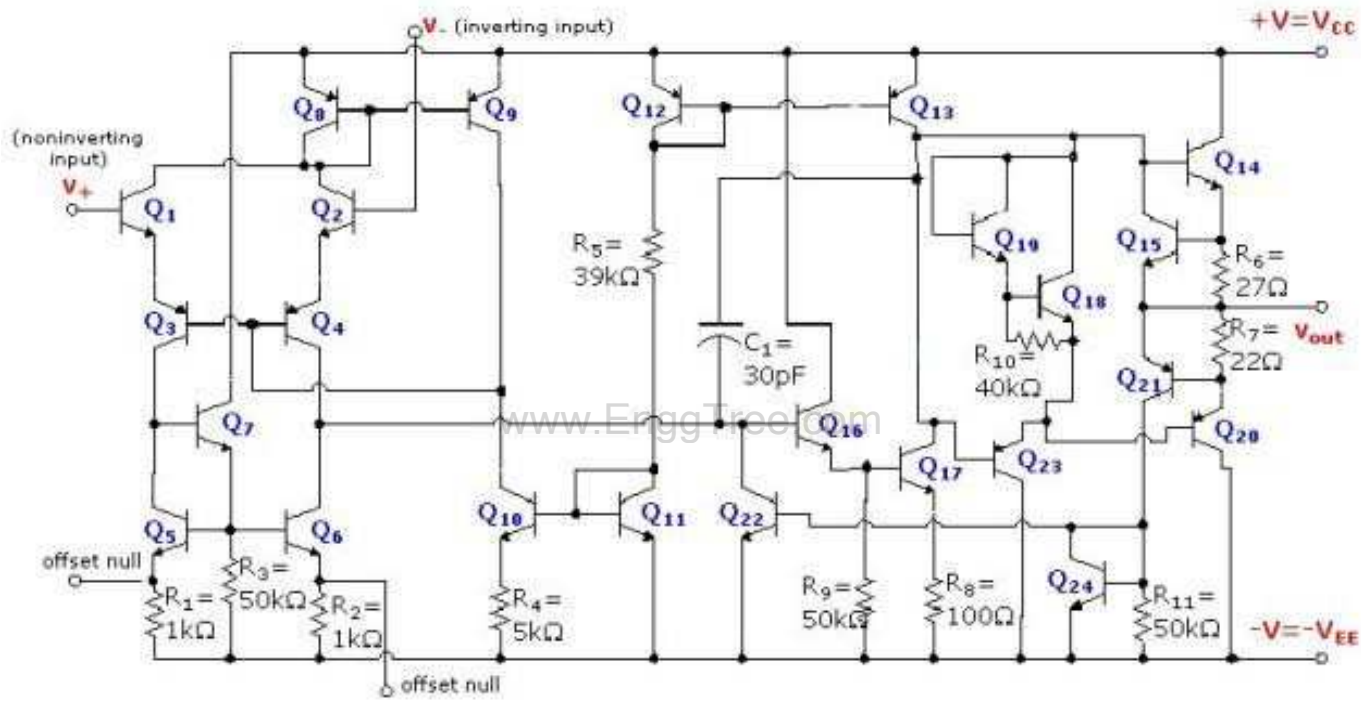
2. **Intermediate stage:**

- ✓ The intermediate stages are shown as the **voltage gain stage and the level shifter** in the figure above.
- ✓ The **voltage gain stage** usually consists of one or more CE amplifiers to provide the bulk of the overall voltage gain.
- ✓ Linear operational amplifiers are direct coupled to eliminate the need for coupling capacitors that are too large to be placed on an IC chip.
- ✓ The **level shifter** stage may be one or more level shifters that are included to ensure that there is no dc offset in the output signal.
- ✓ In addition, these intermediate stages may be used to convert the signal from differential (double-ended) mode to single-ended mode.

3. Output stage:

- ✓ The output stage, or **power output stage**, also serves a dual purpose.
- ✓ It must supply the current required by the load without dissipating too much power in the output transistors.
- ✓ The output stage should provide a low output impedance to allow coupling to a low impedance load without loss of gain.

1.9. INTERNAL CIRCUIT DIAGRAMS OF IC 741



1.10.AC CHARACTERISTICS OF AN OP-AMP

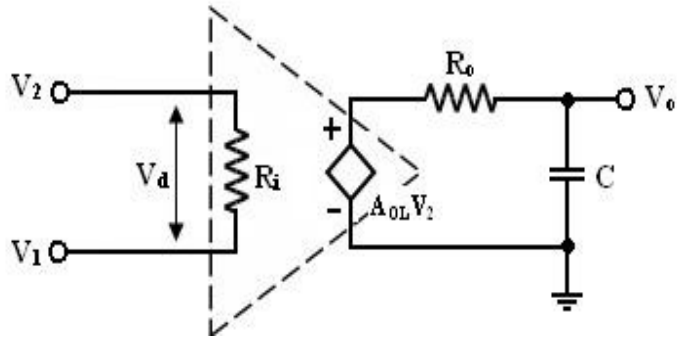
Q. Explain the AC characteristics of op-amp.[Nov/Dec 2021] [Nov/Dec 2022]

1. Frequency Response
2. Circuit Stability
3. Slew Rate
4. Frequency Compensation

1. Frequency Response:

- ✓ The variation in operating frequency will cause variations in gain magnitude and its phase angle.
- ✓ The gain of the op-amp responds to different frequencies is called the frequency response.

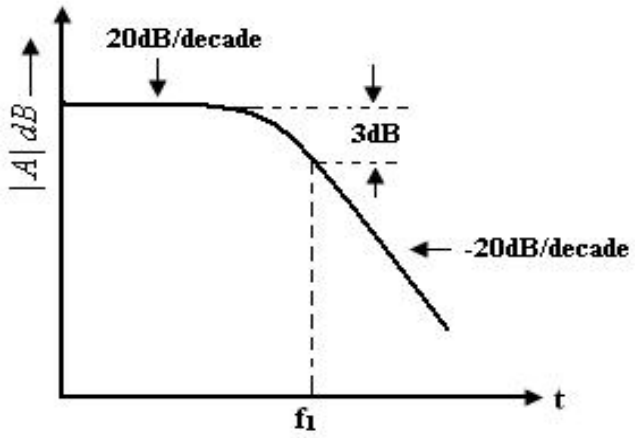
- ✓ Op-amp should have an infinite bandwidth BW =∞.
- ✓ If its open loop gain in 90dB with dc signal, its gain should remain the same 90 dB through audio and onto high radio frequency.
- ✓ The op-amp gain decreases (roll-off) at higher frequency.
- ✓ There is a capacitive component in the equivalent circuit of the op-amp, decrease gain after a certain frequency reached.
- ✓ For an op-amp with only one break (corner) frequency, all the capacitors effects can be represented by a single capacitor C.
- ✓ Variation of the low frequency model with capacitor C at the output is shown in fig.



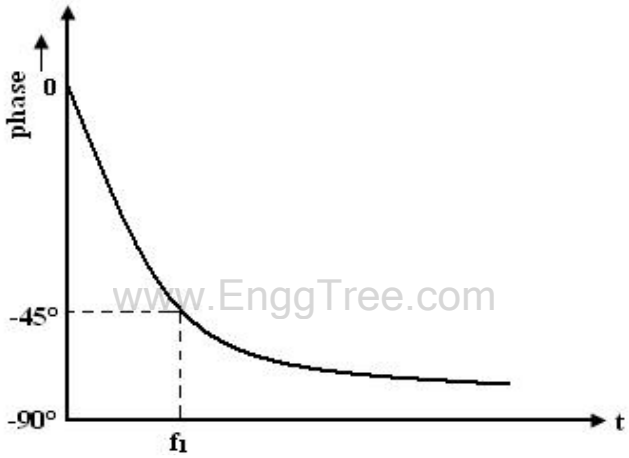
Equivalent circuit of practical circuit

- ✓ There is one pole due to R_oC and one -20dB/decade.
- ✓ The open loop voltage gain of an op-amp with only one corner frequency is obtained from above fig.
- ✓ f_1 is the corner frequency or the upper 3 dB frequency of the op-amp.
- ✓ **The magnitude and phase angle characteristics**:

1. For frequency f<< f1, the magnitude of the gain is 20 log AOL in db.
2. At frequency f = f1, the gain in 3 dB down from the dc value of AOL in db.
   This frequency f1 is called corner frequency.
3. For f>> f1, the fain roll-off at the rate off -20dB/decade or -6dB/decade.



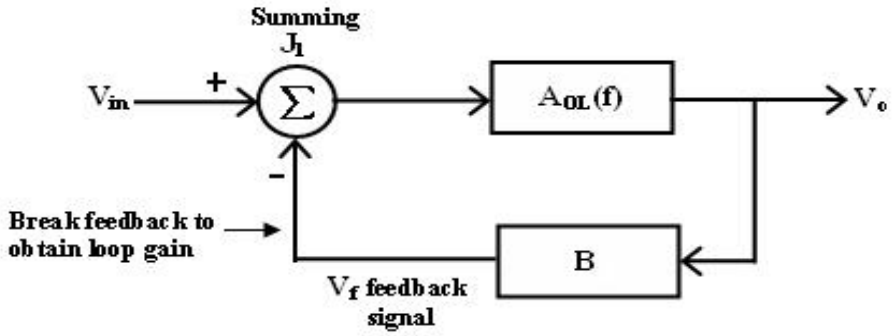
Frequency response of op amp



2. Circuit Stability:

Q. Explain various stability criteria of op-amp. [Nov 2006]

- ✓ A circuit or a group of circuit connected together as a system is said to be stable, if its output reaches a fixed value in a finite time.
- ✓ A system is said to be unstable, if its output increases with time instead of achieving a fixed value.
- ✓ Bode plots are compared of magnitude Vs Frequency and phase angle Vs frequency.
- ✓ Any system whose stability is to be determined can represented by the block diagram.



Feedback loop system

- ✓ The block between the output and input is referred to as forward block.
- ✓ The block between the output signal and feedback signal is referred to as feedback block.
- ✓ The content of each block is referred as transfer frequency.

  AOL (f) = V0 /Vin if Vf = 0 ----- (1)

  where AOL (f) = open loop volt gain.

- ✓ The closed loop gain Af is given by AF = V0 /Vin = AOL / (1+(AOL) (B) ----(2)
- ✓ B = gain of feedback circuit.
- ✓ B is a constant if the feedback circuit uses only resistive components.

- ✓ Once the magnitude Vs frequency and phase angle Vs frequency plots are drawn, system stability may be determined as follows

Method 1:

- ✓ Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.
- ✓ If phase angle is >-180, the system is stable.
- ✓ However, some systems the magnitude may never be 0, in that cases method 2, must be used.

Method 2:

- ✓ Determine the phase angle when the magnitude of (AOL) (B) is 0dB (or) 1.
- ✓ If phase angle is > - 180, the magnitude is –ve decibels then the system is stable.
- ✓ However, some systems the phase angle of a system may reach -1800, under such conditions method 1 must be used to determine the system stability.

3.Slew Rate:

Q. Define slew rate and describe the methods to improve slew rate. [Nov 2005, 08, 2009, May 2009, Dec 2018]

- ✓ **The slew rate** is defined as the maximum rate of change of output voltage caused by a step input voltage.
- ✓ An ideal slew rate is infinite.
- ✓ Slew rate is the maximum rate of change of output voltage with respect to time.
- ✓ It is specified in V/μs.

Reason for Slew rate:

- ✓ The rate at which the volt across the capacitor increases is given by

$$dVc/dt = I/C \text{ --------(1)}$$

- ✓ I -> Maximum amount furnished by the op-amp to capacitor C.
- ✓ Op-amp should have the either a higher current or small compensating capacitors.

4. **Frequency Compensation:**

- ✓ Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.
- ✓ Compensating networks are used to control the phase shift and hence to improve the stability.

Frequency compensation methods:

1. External compensation
   a. Dominant- pole compensation
   b. Pole- zero compensation

2. Internal compensation

1.11.DC CHARACTERISTICS OF AN OP-AMP

Q. Explain the DC characteristics of op-amp.

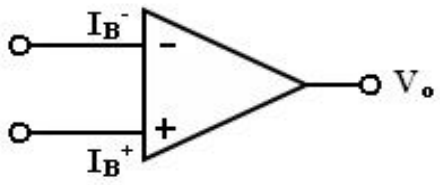
DC characteristics of op amp are,

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

1. Input bias current:

Input bias current I_B is defined as the average value of the base currents entering into terminal of an op-amp.

$$I_B = (I_B^+ + I_B^-) / 2$$



Input Bias Current

2.Input offset current

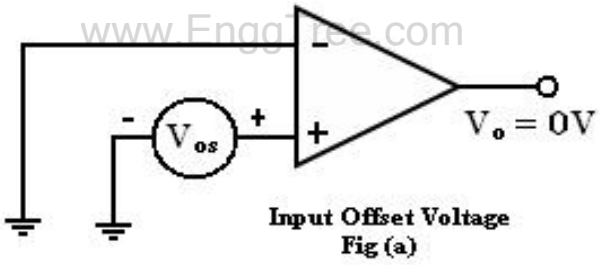
The difference between the bias currents at the input terminals of the op- amp is called as **input offset current.**

$$I_{OS} = I_B^+ - I_B^-$$

The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents

3. Input offset voltage

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called **input offset voltage**



Input Offset Voltage
Fig (a)

4. Thermal drift

Bias current, offset current and offset voltage change with temperature.

A circuit carefully nulled at 25°c may not remain so when the temperature rises to 35°c. This is called **drift.**

1.12. OPEN LOOP OP-AMP CONFIGURATION

Q. Explain the open loop configuration of op-amp with example circuits. (Nov 2016)

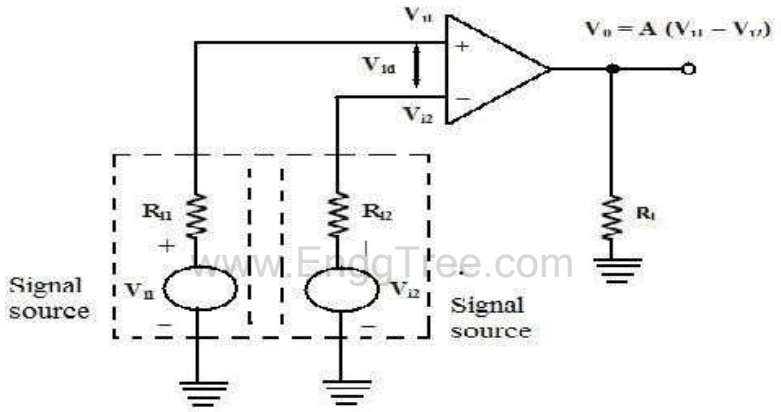
- ✓ The term open-loop indicates that no feedback in any form is fed to the input from the output.
- ✓ When connected in open – loop, the op-amp functions as a very high gain amplifier.
- ✓ There are three open – loop configurations of op-amp namely,

1. Differential amplifier
2. Inverting amplifier
3. Non-inverting amplifier

- ✓ The above classification is made based on the number of inputs used and the terminal to which the input is applied.
- ✓ The op-amp amplifies both ac and dc input signals.
- ✓ Thus, the input signals can be either ac or dc voltage.

1. <u>Differential Amplifier:</u>

- ✓ In this configuration, the inputs are applied to both the inverting and the non-inverting input terminals of the op-amp.
- ✓ It amplifies the difference between the two input voltages.



Open - loop Differential Amplifier

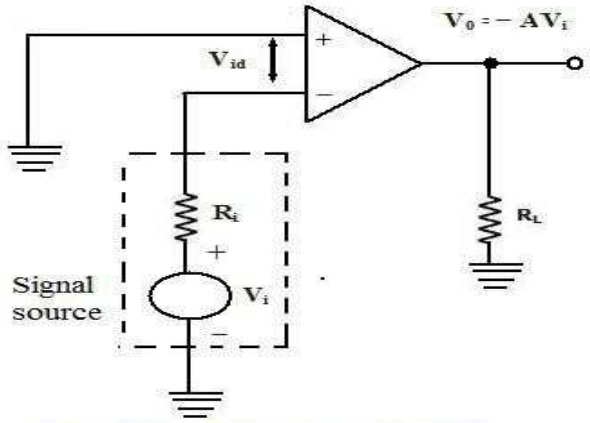
- ✓ Figure shows the open-loop differential amplifier configuration.
- ✓ The input voltages are represented by V_{i1} and V_{i2}.
- ✓ The source resistance R_{i1} and R_{i2} are negligibly small in comparison with the very high input resistance offered by the op-amp.
- ✓ Thus the voltage drop across these source resistances is assumed to be zero.
- ✓ The output voltage V_0 is given by

$$V_0 = A\,(V_{i1} - V_{i2})$$

where A is the large signal voltage gain.

- ✓ Thus the output voltage is equal to the voltage gain A times the difference between the two input voltages.
- ✓ This is the reason why this configuration is called a differential amplifier.
- ✓ In open – loop configurations, the large signal voltage gain A is also called open-loop gain A.

2. Inverting amplifier:



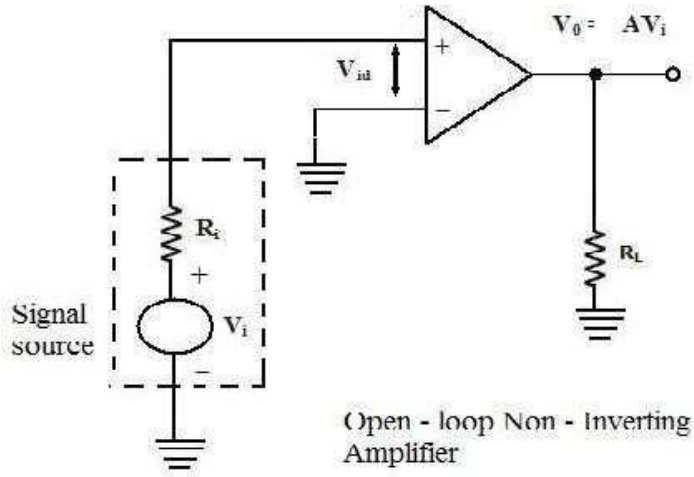
Open - loop Inverting Amplifier

- ✓ In this configuration, the input signal is applied to the inverting input terminal of the op - amp and the non-inverting input terminal is connected to the ground.
- ✓ Figure shows the circuit of an open loop inverting amplifier.
- ✓ The output voltage is 180 out of phase with respect to the input.
- ✓ Hence, the output voltage V0 is given by,

$$V0 = -AVi.$$

- ✓ Thus, in an inverting amplifier, the input signal is amplified by the open-loop gain A and in phase shifted by 180^0.

3.Non-inverting Amplifier:



Open - loop Non - Inverting Amplifier

- ✓ Figure shows the open – loop non- inverting amplifier.
- ✓ The input signal is applied to the non-inverting input terminal of the op-amp and the inverting input terminal is connected to the ground.
- ✓ The input signal is amplified by the open – loop gain A and the output is in-phase with input signal.

$V_0 = AVi$

Limitations of Open – loop Op – amp configuration:

- ✓ In the open – loop configurations, clipping of the output waveform can occur when the output voltage exceeds the saturation level of op-amp.
- ✓ This is due to the very high open – loop gain of the op-amp.
- ✓ The open – loop gain of the op – amp is not a constant.
- ✓ It varies with changing temperature and variations in power supply.
- ✓ Also, the bandwidth of most of the open- loop op amps is negligibly small.
- ✓ This makes the open – loop configuration of op-amp unsuitable for ac applications.

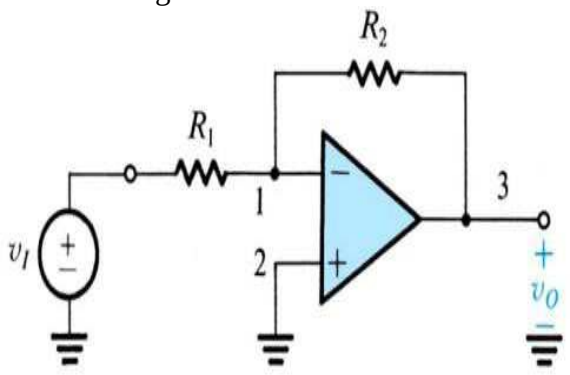
1.13. CLOSED LOOP OP-AMP CONFIGURATION

Q. Explain the inverting and Non-inverting amplifier of closed loop configurations. [Dec 2018]

- ✓ The op-amp can be effectively utilized in linear applications by providing a feedback from the output to the input, either directly or through another network.
- ✓ If the feedback signal is out - of- phase by 1800 with respect to the input, then the feedback is referred to as negative feedback or degenerative feedback.
- ✓ If the feedback signal is in phase with respect to the input, then the feedback is referred to as positive feedback or regenerative feedback.
- ✓ An op amp that uses feedback is called a closed – loop amplifier.
- ✓ The most commonly used closed loop amplifier configurations are
  1. Inverting amplifier (Voltage shunt amplifier)
  2. Non- Inverting amplifier (Voltage – series Amplifier)

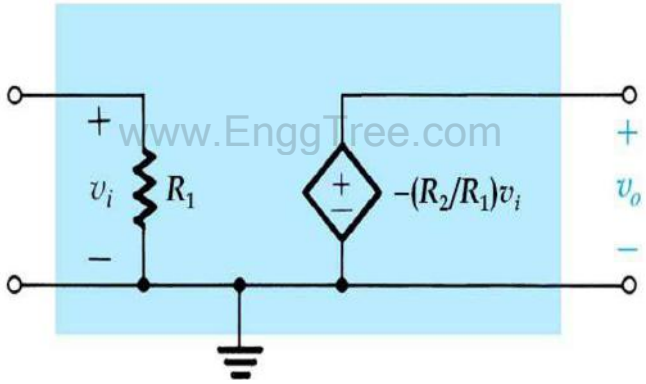
The inverting close-loop configuration

- ✓ External components R1 and R2 form a close loop
- ✓ Output is fed back to the inverting input terminal
- ✓ Input signal is applied from the inverting terminal



- ✓ The required conditions to apply virtual short for op-amp circuit:
  - ➢ Negative feedback configuration
  - ➢ Infinite open- loop gain
- ✓ Closed loop gain: G ≡ V_O /V_I = -R2 /R1
- ✓ Infinite differential gain: V2 - V1 = V_O /A = 0
- ✓ Infinite input impedance: i2 = i1 = 0
- ✓ Zero output impedance: V_O = V_1 - i1R2 = - vI R2 /R1
- ✓ Voltage gain is negative: Input and output signals are out of phase
- ✓ Closed loop gain depends entirely on external passive components (independent of op-amp gain)
- ✓ Close loop amplifier trades gain (high open loop gain) for accuracy (finite but accurate closed loop gain)

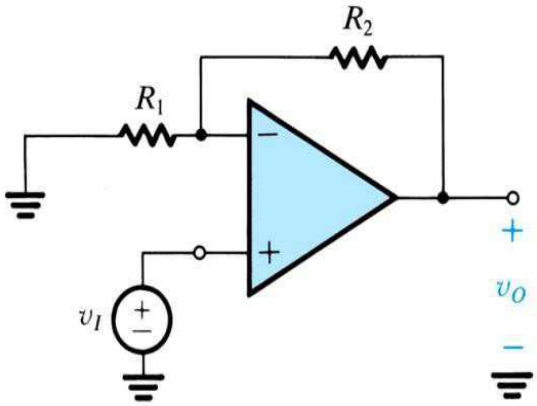
Equivalent circuit model for the inverting configuration



- ✓ Input impedance: Ri ≡vI /iI = vI / (vI /R1) = R1
- ✓ For high input closed loop impedance, R1 should be large, but is limited to provide sufficient G
- ✓ In general, the inverting configuration suffers from a low input impedance
- ✓ Output impedance: Ro = 0
- ✓ Voltage gain: Avo = - R2/R1

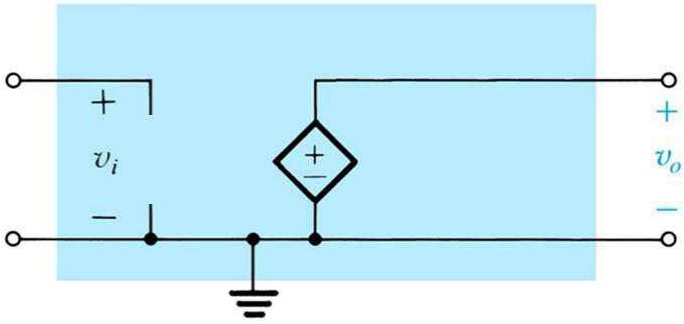
2.<u>Non inverting closed loop Configuration:</u>

- ✓ External components R1 and R2 form a close loop
- ✓ Output is fed back to the inverting input terminal Input signal is applied from the noninverting terminal.



- ✓ The required conditions to apply virtual short for op- amp circuit:
  - ➢ Negative feedback configuration
  - ➢ Infinite open loop gain
- ✓ Closed loop gain: G ≡ V_O /V_I = 1 + R2 /R1
- ✓ Infinite differential gain: V_+ - V- = V_O /A = 0
- ✓ Infinite input impedance: i2 = i1 = V- /R1
- ✓ Zero output impedance: V_O = V- + i_1R2 = V_I (1 + R2 /R1)
- ✓ Closed loop gain depends entirely on external passive components (independent of op amp gain)
- ✓ Close loop amplifier trades gain (high open loop gain) for accuracy (finite but accurate closed loop gain)

Equivalent circuit model for the noninverting configuration



- ✓ Input impedance: Ri = Infinite
- ✓ Output impedance: Ro = 0

1.14. JFET OPERATIONAL AMPLIFIERS

1.15. LF 155

1.16. TL082

TWO MARKS

1. Define an integrated circuit. (or) what is an integrated circuit? [May 2010]

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

2. Mention the advantages of integrated circuits.

The advantages of integrated circuits are,

- ✓ Miniaturization and hence increased equipment density.
- ✓ Cost reduction due to batch processing.
- ✓ Increased system reliability due to the elimination of soldered joints.
- ✓ Improved functional performance.
- ✓ Matched devices.
- ✓ Increased operating speeds. Reduction in power consumption

3. Define Current mirror circuit & List out its advantages. (or) What is current mirror? [April/May 2010, Nov/Dec 2011]

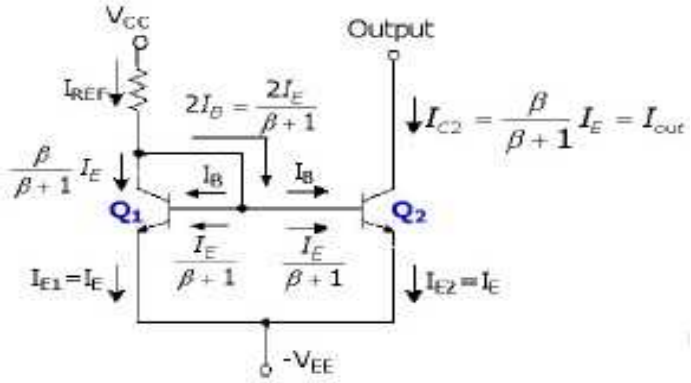
A circuit in which the output current is equal to input current is called current mirror circuit. In current mirror circuit, the output current is the mirror image of the input current.

Advantages:

a. High CMRR

b. Easy to design

4. Draw the current mirror circuit.



5. Give the basic concept of current source.

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of collector voltage.

6. What are the applications of current sources?

The applications of current sources are:

i. The emitter resistance in differential amplifier to increase CMRR.

ii. As an active load to provide high a.c.resistance without disturbing the d.c conditions.

7. Give the limitation of current mirror circuit.

The limitation of current mirror circuit is whenever we need low value of current, the value of resistance is high and it cannot be fabricated economically in IC circuits

8. Justify the reasons for using current sources in integrated circuits.

1. Superior insensitivity of circuit performance to power supply variations and temperature.
2. More economical than resistors in terms of die area required providing bias currents of small value.
3. When used as load element, the high incremental resistance of current source results in high voltage gains at low supply voltages.

9. What is the advantage of widlar current source over constant current source?

Using constant current source, the output current of small magnitude (microamp range) is not attainable due to the limitations in chip area. Widlar current source is useful for obtaining small output currents. Sensitivity of widlar current source is less compared to constant current source.

10. Mention the advantages of Wilson current source.

The advantages of Wilson current sources are:

- ✓ Provides high output resistance.
- ✓ Offers low sensitivity to transistor base currents.

11. What is voltage source?

A voltage source is a circuit that produces an output voltage (V_0), which is independent of the load driven by the voltage source or the output current supplied to the load.

12. Give advantages of emitter follower voltage source.

The advantages of emitter follower are:

a. It produces low ac impedance

b. Gives effective decoupling of adjacent gain stages.

13. Write the limitation of emitter follower or common collector voltage source.

Emitter follower voltage source is weak and without protection for changes in bias voltage and the output voltage with respect to changes in supply voltage.

14. What is voltage reference? [Nov/Dec 2021]

The circuit that is designed for providing a constant voltage independent of changes in temperature is called a voltage references.

15. Define temperature coefficient.

Temperature coefficient is the measure of the ability of the circuit to maintain the standard output voltage under varying temperature conditions.

$$TC(V_O) = dV_O / dT \text{ in } mV/^{O} C$$

16. What are the properties of voltage reference?

The Properties of voltage reference are:

i. Reference voltage must be independent any temperature change.

ii. It must have good power supply rejection which is independent of the supply voltage.

iii. The circuit should have low output impedance.

17. What are the parameters of voltage reference circuits?

The Parameters of voltage reference are:

i. Line regulation

ii. Load regulation

iii. Long term stability

iv. Ripple rejection ratio.

18. Define line regulation.

Line regulation is defined as the ratio of change in output voltage to the change in input voltage.

Line regulation = $\Delta V_O/\Delta V_i$

Where ΔV_O – changes in the output line voltage

ΔV_i - changes in the input line voltage It is expressed in mV/V

19. Define load regulation.

Load regulation is defined as the ratio of change in output voltage to the change in load current. Load regulation = $\Delta V_O/\Delta I_L$

Where ΔV_O – changes in the output line voltage

ΔI_L - changes in the load current It is expressed in mV/mA

20. What is long term stability?

The ability of the circuit to maintain the output voltage constant with respect to time is given by the parameter long term stability. It is measured in ppm/1000 hours.

21. Define Ripple Rejection Ratio (RRR).

The ability of the circuit to reject input ripples and an indication of how much ripples are present at the output due to input is given by the factor RRR.It is defined as RRR = $20 \log_{10}[V_{ri}/V_{ro}]$ Where V_{ri} - Input ripple and V_{ro} –Output ripple

22. What are the limitations in a temperature compensated zener-reference source?

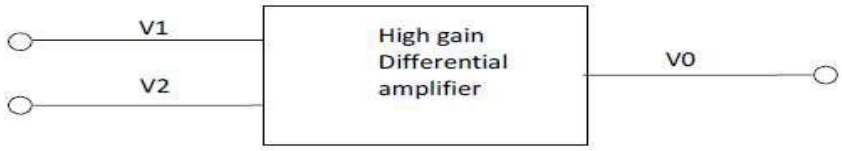
Limitations of zero reference source:

A power supply voltage of at least 7 to 10 V is required to place the diode in the breakdown region and that substantial noise is introduced in the circuit by the avalanching diode.

23. What is differential amplifier? Need for differential amplifier. [Nov/Dec 2022]

A circuit which amplifies the difference between two input voltage signals. Hence it is also called as difference amplifier.

24. Draw the block diagram for differential amplifier.



25. What are the properties of differential amplifier?

The Properties of differential amplifier are:

i. Excellent stability

ii. High versatility

iii. High immunity to interference signals.

26. Give the advantages of differential amplifier.

The advantages of differential amplifier are:

1. Lower cost
2. IC fabrication is easy
3. Closely matched components

27. Define differential gain.

Differential gain is defined as the ratio of the output voltage to the difference voltage.

$$A_d = V_o / V_d ,$$

In decibel $20 \log_{10} A_d = 20 \log_{10} V_o / V_d$

28. Why are active loads preferred than passive loads in the input stage of an operational amplifier? [Nov /Dec 2010] [Nov/Dec 2022]

Differential amplifier designed with active load to increase the CMRR. The gain increased by using large value of collector resistances. If the collector resistance is large then limitation in IC fabrications are large chip area and large bias voltage need.

29. Define CMRR. [May/June 2004, Nov/Dec 2005, Nov/Dec 2009, Nov/Dec 2010]

The common Mode Rejection ratio (CMRR) is defined as the ration of difference modegain to the common mode gain

$$CMRR = |A_{DM}/A_{CM}|$$

It is expressed in decibel (dB)

30. What are the draw backs of using large RC in differential amplifier?

The main draw backs are: It requires large chip area. For larger RC quiescent drop, a large power supply will be required to maintain a given quiescent collector current.

31. What is active load? Where it is used and why?

The requirement to increase the gain is same that the collector resistance (RC) should not disturb d.c conditions while it must provide large resistance for a.c purposes. The current mirror which has very low d.c resistance (dV/dI) and higher a.c resistance (dv/di) can be used as a collector load instead of RC. Such a load is called as active load.

32. What is an operational amplifier? [Nov/Dec 2005]

An operational amplifier is a direct-coupled, high gain amplifier consisting of one or more differential amplifier. By properly selecting the external components, it can be used to perform a variety of mathematical operations.

33. What are the popular IC packages available?

The IC packages available are:

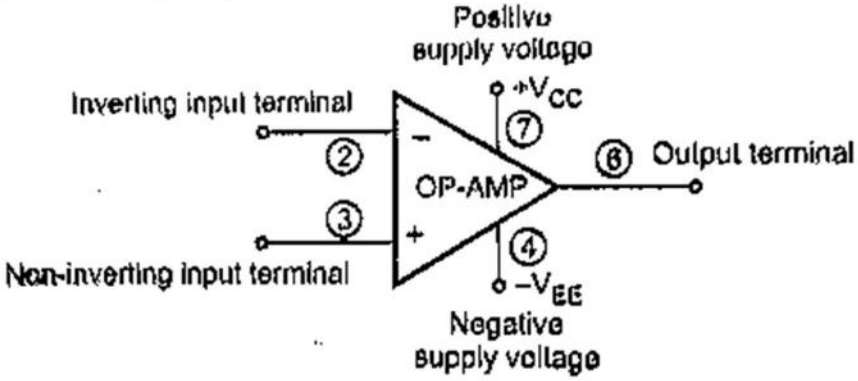
- Metal can package.
- Dual-in-line package.
- Ceramic flat package.

34. List out the ideal characteristics, and draw the equivalent diagram of an OP-AMP Mention any four important characteristics of ideal operational amplifier. [May/June2003, May/June2009, Nov/Dec2010]

The Ideal characteristics of op-amp are:

- Open loop voltage gain is infinity.
- Input impedance is infinity.
- Output impedance is zero.
- Bandwidth is infinity.
- Zero offset
- Infinite CMRR
- Infinite slew rate
- PSRR = 0

35. Draw the circuit symbol for op-amp.

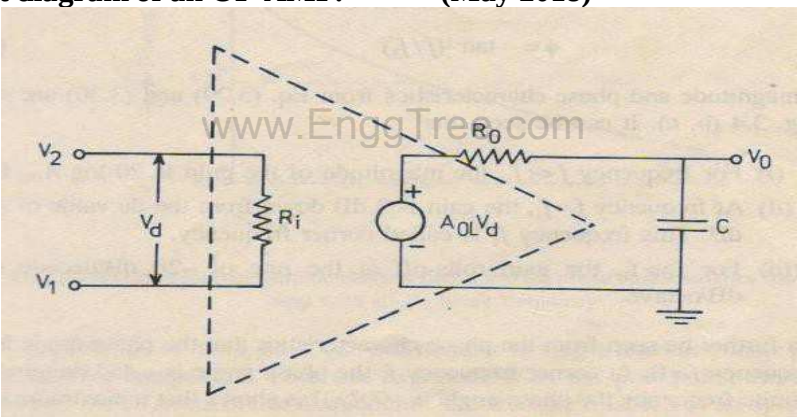


Op-amp symbol

36. Define Virtual ground property of an OP-AMP.

A virtual ground is a ground which acts like a ground. It may not have physical connection to ground. This property of an ideal op-amp indicates that the inverting and non-inverting terminals of op-amp are at the same potentials. The non-inverting input is grounded for the inverting amplifier circuit. This means that the inverting input of the op-amp is also at ground potential.

37. Draw the equivalent diagram of an OP-AMP. (May 2018)



38. What are the stages in op-amp?

The stages of op-amp are:

a. Input stage

b. Gain stage

c. Output stage

39. What are the requirements of the input stage of an op-amp?[May/June 2010]

The differential amplifier eliminates the need for an emitter bye-pass capacitor. So, differential amplifier is used as an input stage in op-amp ICs

40. In what way 741S is better than 741? [Nov/Dec2003]

741S is a military grade op-amp with higher slew rate

41. Why is IC741 op-amp not used for high frequency applications?

Op-amp IC741 has very low slew rate and therefore cannot be used for high frequency applications

42. Define Input bias current. [May/June 2009]

Input bias current IB is the average of the currents that flow into the inverting and non- inverting input terminals of the op-amp.

i.e. IB = (IB1+IB2)/2

43. Define Input offset current. [May/June 2009]

The algebraic difference between the current into the inverting and non-inverting terminals is referred to as input offset current Iio. Mathematically it is represented as Iios= |IB+ - IB- |

Where I B+ is the current into the non-inverting input terminals.

IB- is the current into the inverting input terminals.

44. What is Input offset voltage?

Input offset voltage is the voltage required to be amplified at the input for making output voltage to zero volts.

45. Determine the slew rate of the op-amp. Or Define slew rate. (May/June2003, Nov/Dec2010, Nov/Dec2011, May/June 2008]

Slew rate can be defined as the maximum rate of change of output voltage of op-amp with respect to time. It is expressed as S = (dVo / dt) max in V/Sec.Where slew rate S = 2Π f Vm in V/Sec.

46. What is a compensating network?

The networks formed by components such as resistors and capacitors for modifying the rate of change of gain and the phase shift is called as compensating network

47. When are the internally compensating systems used?

In applications where the op-0amp is required to amplify relatively slow changing signals and does not require good high frequency response, internally compensating systems are used.

48. In response to a square wave input, the output of an op-amp changed from -3V to +3V over a time interval of 0.25µs, find slew rate. (May '06)

Slew rate= $\Delta Vo/\Delta t = 6/0.25=24$ V/µs.

49. List the types of frequency compensation.

a. External frequency compensation

1. Dominant pole freq. compensation
2. Pole zero freq. compensation

b. Internal frequency compensation.

50. List the DC characteristics of op amp.

DC characteristics of op-amp are:

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift.

51. List the AC characteristics of opamp. (Dec 2018)

AC characteristics of op-amp are:

1. Frequency response
2. Stability of an op-amp,
3. Frequency compensation
4. Slew rate.

52. What is the need for frequency compensation in practical op-amps?

Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability.

53. What are the merits of Dominant-pole compensation?

The merits of Dominant-pole compensation are:

1.Noise immunity of the system is improved.

2. Open-loop bandwidth is reduced.

54. What is the maximum undistorted amplitude, that a sine wave input of 10 KHz, can produce, at the output of an op-amp whose slew rate is 0.5V/μs? (Nov '12)

Given F=10KHZ and slew rate (S) = **0.5V**/μs

Solution: Slew rate (S) = 2πfVm V/ μs.

Maximum amplitude (Vm) = S/2πf =7.92V

55. The op-amp has a gain of 12 million. Express the gain in dB.(Nov '03)

Gain in dB=20log(gain)

20 log($20*10^6$)= 141.6dB

56. What is the need for frequency compensation in practical op-amps?

Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability.

57. Why open loop op-amp configurations are not used in linear applications?

a. The open loop gain of the op-amp is very high. Therefore, only the smaller signals having low frequency may be amplified accurately without distortion.

b. Open loop Voltage gain of the op-amp is not a constant voltage gain varies with changes in temperature and power supply as well as mass production techniques. This makes op-amp unsuitable for many linear applications

c. Bandwidth of most open loop op-amps is negligibly small or almost zero therefore op-amp is impractical in ac applications.

58. In practical op-amps, what is the effect of high frequency on its performance?

The open-loop gain of op-amp decreases at higher frequencies due to the presence of parasitic capacitance. The closed-loop gain increases at higher frequencies and leads to instability.

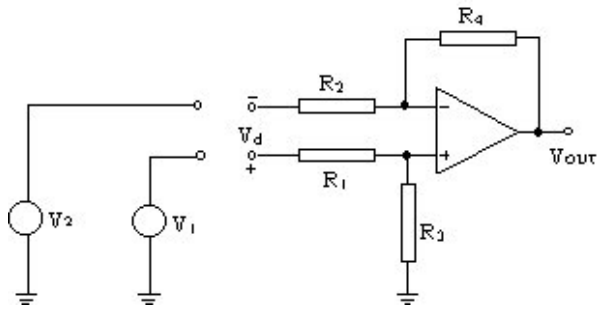
59. What are the advantages of negative feedback?

Advantages of negative feedback are:

1. It reduces the gain and makes it controllable
2. It reduces the possibility of distortion
3. It increases the bandwidth
4. It increases the input resistance of the op-amp
5. It decreases the output resistance of the op-amp
6. It reduces the effect of temperature, power supply on the gain of the circuit.

60. Define Differential Mode gain. (Dec 2018)

Gain of an amplifier is defined as V_{OUT}/V_{IN}. For the special case of a differential amplifier, the input V_{IN} is the difference between its two input terminals, which is equal to (V_1-V_2) as shown in the following diagram.



61. What are the two methods can be used to produce voltage sources? (May 2018)

There are two methods used to produce a voltage source, namely,

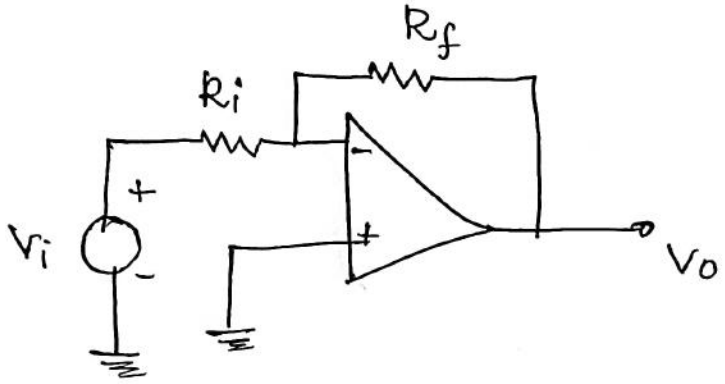
1. Using the impedance transforming properties of the transistor,
2. Using an amplifier with negative feedback.

62. Why is slew rate is infinite in an ideal op-amp? [N0v/Dec 2021]

For an ideal operational amplifier, time delay is negligible. Hence it has an infinite slew rate. That means it can provide output voltage simultaneously with the input voltage changes.

PART B

1) A 741 op-amp is used as an inverting amplifier with a closed loop gain of 50. Find the maximum input signal that can be applied to get undistorted output if frequency response is constant upto 20KHz. [Nov/Dec 2022].



$$A_{CL} = \frac{-R_f}{R_1} = 50$$

$$50R_1 = -R_f$$

$$\frac{V_o}{V_{in}} = 50$$

$$V_o = 50 V_{in}$$

$$V_{in} = \frac{V_o}{50}$$

Assume S = 2

$$V_o = V_m = \frac{S \times 10^6}{2\pi \times f} = \frac{2 \times 10^6}{2\pi \times \frac{20}{10} \times 10^3} = \frac{100}{2\pi}$$

$$V_o = \frac{100}{6.28} = 15.92V$$

$V_o = 15.92$ V. $V_{in} = \frac{15.92}{50}$

$V_{in} = 30 \times 10^{-2}$ V.

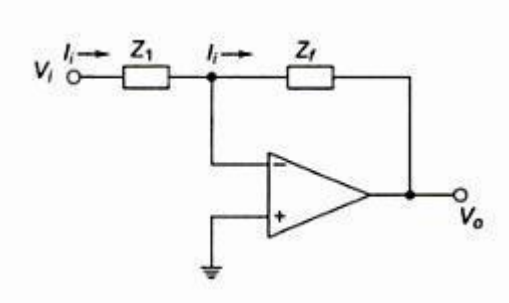
UNIT II

APPLICATIONS OF OPERATIONAL AMPLIFIERS

Sign Changer, Scale Changer, Phase Shift Circuits, Voltage Follower, V-to-I and I-to-V converters, adder, subtractor, Instrumentation amplifier, Integrator, Differentiator, Logarithmic amplifier, Antilogarithmic amplifier, Comparators, Schmitt trigger, Precision rectifier, peak detector, clipper and clamper, Low-pass, high-pass and band-pass Butterworth filters.

Sign Changer (Phase Inverter)

Explain sign changer and scale changer using op-amp.



- ✓ The basic inverting amplifier configuration using an op-amp with input impedance Z1 and feedback impedance Zf .
- ✓ If the impedance Z1 and Z f are equal in magnitude and phase, then the closed loop voltage gain is -1, and the input signal will undergo a 180° phase shift at the output.
- ✓ Hence, such circuit is also called phase inverter.
- ✓ If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign.
- ✓ Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

Scale Changer:

- ✓ Referring the above diagram, if the ratio $Z_f / Z_1 = k$, a real constant, then the closed loop gain is – k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output.
- ✓ Usually, in such applications, Z_f and Z_1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

Phase Shift Circuits

Explain the phase shift circuits using op-amp.

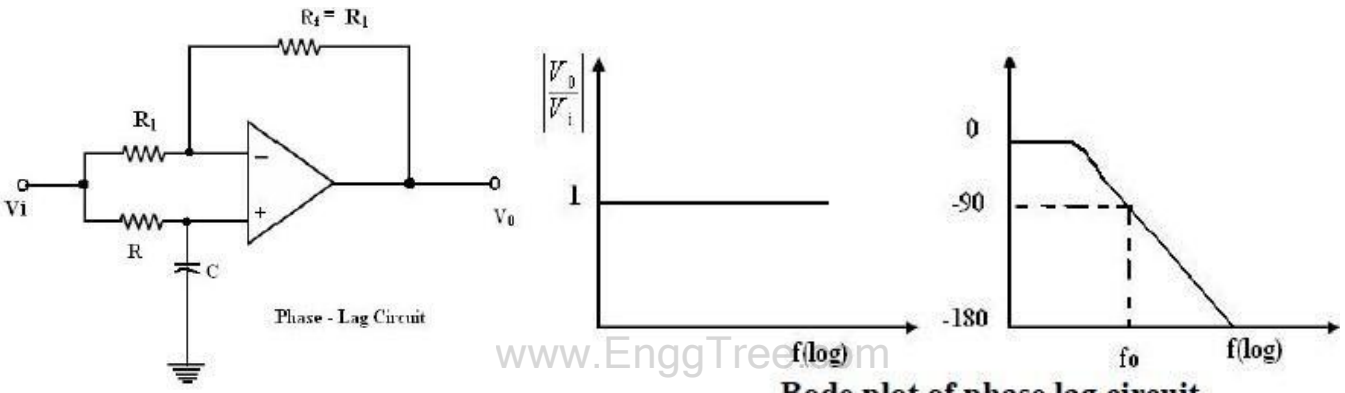
- ✓ The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain.
- ✓ These circuits are also called constant-delay filters or all-pass filters.
- ✓ That constant delay refers to time difference between input and output remains constant when frequency is changed over a range of operating frequencies.
- ✓ This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range.

- ✓ The two types of circuits, for lagging phase angles and leading phase angles.

Phase-lag circuit:

- ✓ Phase lag circuit is constructed using an op-amp, connected in both inverting and non-inverting modes.
- ✓ To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non-inverting amplifier with a low-pass filter.
- ✓ It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit is

$$1+\frac{R_f}{R_1} \approx 1+1=2 \quad \text{Since R f=R1.}$$



Bode plot of phase lag circuit

$$V_O(jw) = -V_i(jw)\left(-1+\frac{2}{1+jwRC}\right)$$

and the relationship between output and input can be expressed by

$$\frac{V_O(jw)}{V_i(jw)} = \frac{(1-jwRC)}{(1+jwRC)}$$

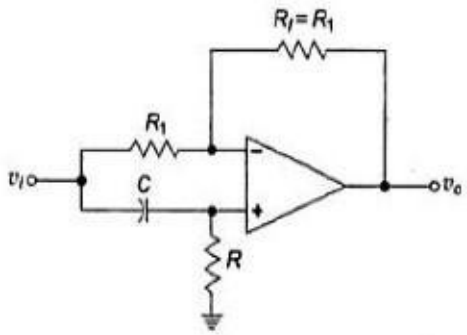
The relationship is complex as defined above equation and it shows that it has both magnitude and phase. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

$$\theta = -2\ \tan^{-1} RC\omega$$

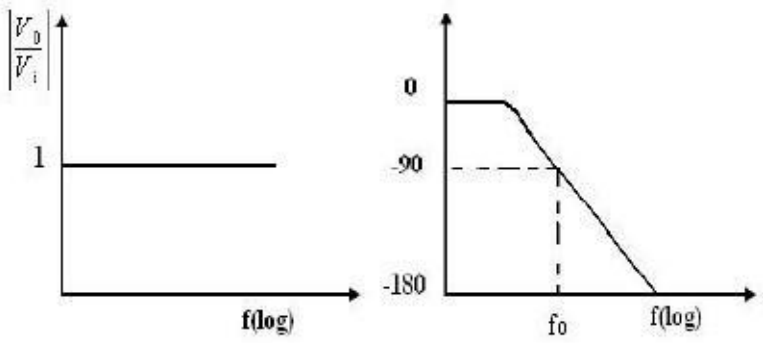
Phases-lead circuit

$$\frac{V_O(jw)}{V_i(jw)} = -\frac{(1-jwRC)}{(1+jwRC)}$$

$$\theta = 180° - 2\ \tan^{-1} RC\omega$$



Phase lead circuit

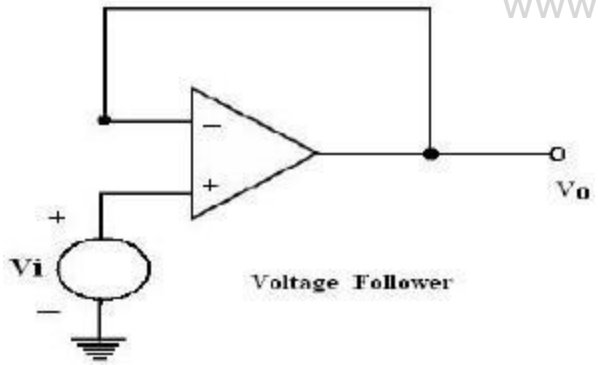


Bode plot of Phase lead circuit

- ✓ Phase lead circuit is constructed using an op-amp, connected in both inverting and non-inverting modes.
- ✓ To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non-inverting amplifier with a High-pass filter.

Voltage follower:

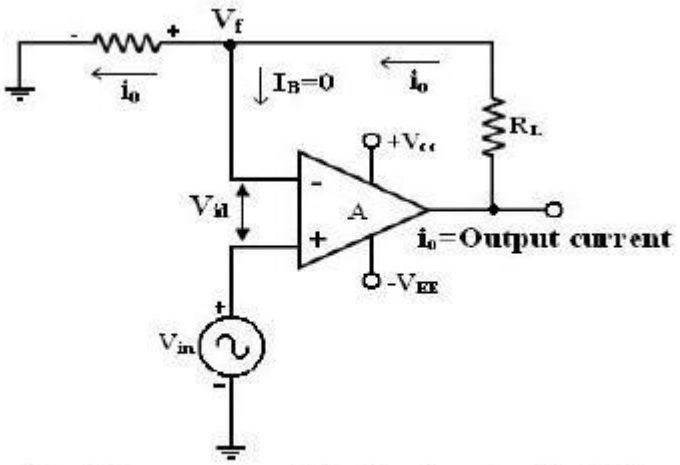
Draw the voltage follower circuit and explain. (May 2018)



- ✓ If R1=∞ and Rf =0 in the non-inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower.
- ✓ The circuit consists of an op-amp and the output voltage is equal to the input voltage, both in magnitude and phase. V0=Vi.
- ✓ Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower.
- ✓ It offers very high input impedance of the order of MΩ and very low output impedance.
- ✓ Therefore, this circuit draws negligible current from the source.
- ✓ Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

Voltage to Current Converter with floating loads (V/I) [Nov/Dec 2022]

Explain voltage to current converter using op-amp. (Nov 2006, 2016, May 2018) [Nov/Dec 2021]



V to I Converter with floating loads (V/I)

- ✓ Voltage to current converter in which load resistor RL is floating (not connected to ground).
- ✓ Vin is applied to the non- inverting input terminal, and the feedback voltage across R1 devices the inverting input terminal.
- ✓ This circuit is also called as a current – series negative feedback amplifier.

✓ Because the feedback voltage across R1 (applied Non-inverting terminal) depends on the output current i0 and is in series with the input difference voltage Vid.

Writing KVL for the input loop,

Voltage $V_{id} = V_f$ and $I_B = 0$, $V_i = R_L i_o$ where $i_o = \frac{V_i}{R_L}$

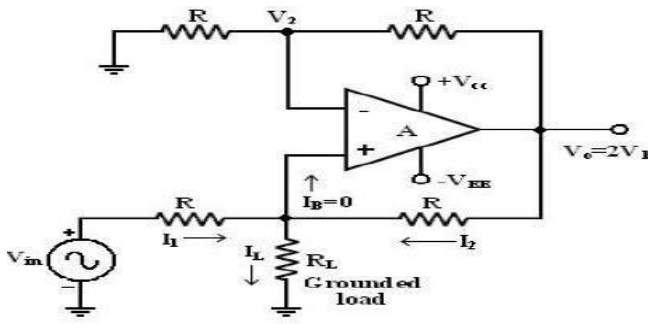
✓ From the fig input voltage Vin is converted into output current of Vin/RL [Vin -> i0].

✓ In other words, input volt appears across R1. If RL is a precision resistor, the output current (i0 = Vin/R1) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

Voltage – to current converter with Grounded load



V – I converter with grounded load

- ✓ This is the other type V – I converter, in which one terminal of the load is connected to ground.

Analysis of the circuit:

- ✓ The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V1 at the non-inverting (+) terminals and
2. To establish relationship between V1 and the load current IL. Applying KCL at node a,

R= Rf

I1 +I2=IL

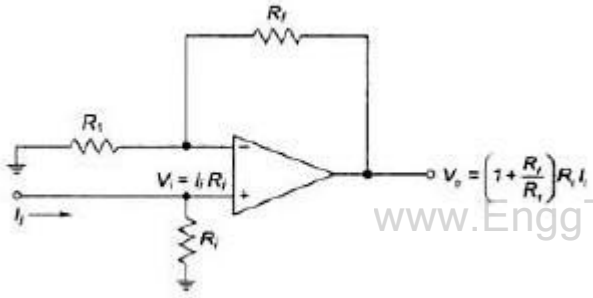
(Vi+Va)/R + (Vo –Va)/R= IL

Vo = (Vi +Vo - IL R)/2 and gain =1+ R/R= 2.

$$\therefore V_i = I_L R \; ; I_L = V_i/R$$

Current to Voltage Converter (I –V):

Explain current to voltage converter using op-amp. (Nov 2016)[Nov/Dec2021]



Open – loop gain A of the op-amp is very large. Input impedance of the op amp is very high.

Sensitivity of the I – V converter:

1. The output voltage V0 = -RF Iin.
2. Hence the gain of this converter is equal to -RF. The magnitude of the gain (i.e.) is called as sensitivity of I to V converter.
3. The amount of change in output volt ΔV0 for a given change in the input current ΔIin is decide by the sensitivity of I-V converter.
4. By keeping RF variable, it is possible to vary the sensitivity as per the requirements.

Applications of I – V Converter:

One of the most common uses of the current to voltage converter is

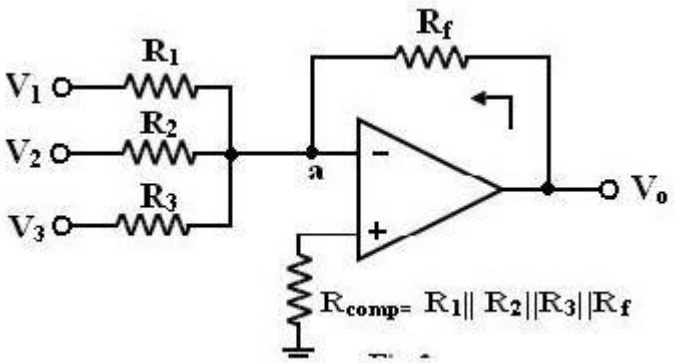
1. Digital to analog Converter (DAC)
2. Sensing current through Photo detector. Such as photo cell, photo diodes and photovoltaic cells.

Photoconductive devices produce a current that is proportional to an incident energy or light (i.e). It can be used to detect the light.

Adder:

- ✓ Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer or adder.

Inverting Summing Amplifier:



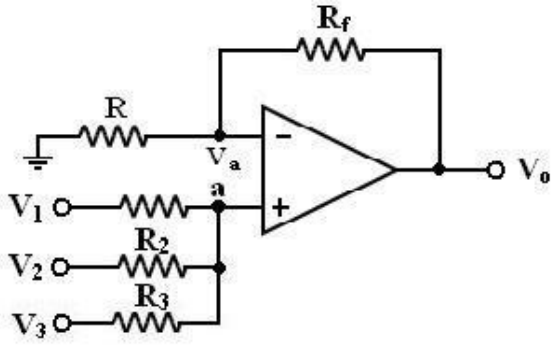
- ✓ A typical summing amplifier with three input voltages V1, V2 and V3 three input resistors R1, R2, R3 and a feedback resistor Rf is shown in figure.
- ✓ The op-amp is an ideal one, AOL= ∞.
- ✓ Since the input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non-inverting input terminal is at ground potential.

I= V1/R1+V2/R2…..+Vn/Rn;

Vo= - Rf I=Rf/R(V1+V2+….Vn).

- ✓ To find Rcomp, make all inputs V1 = V2 = V3 = 0.
- ✓ So the effective input resistance Ri = R1 || R2 || R3.
- ✓ Therefore, Rcomp = Ri || Rf = R1 || R2 || R3 || R,f.

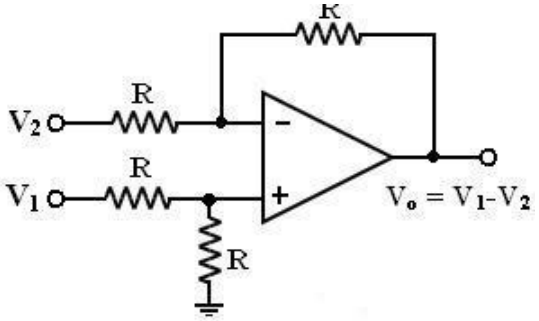
Non-Inverting Summing Amplifier:



- ✓ A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure
- ✓ Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs.
- ✓ Let R1 = R2 = R3 = R = Rf/2, then Vo = V1+V2+V3

Subtractor:

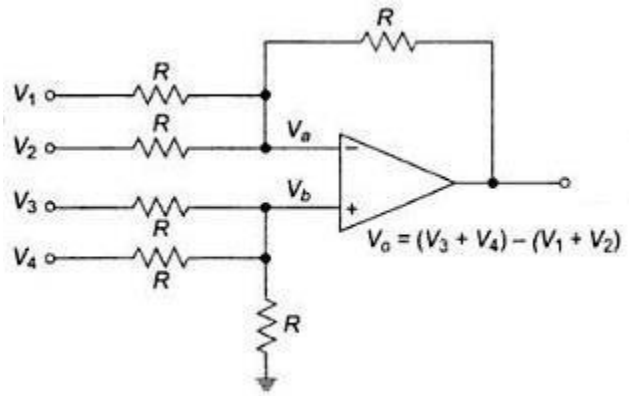
(Write short notes on subtractor.) (May 2018)



- ✓ A basic differential amplifier can be used as a subtractor as shown in the above figure.
- ✓ If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

- ✓ To find the output V01 due to V1 alone, make V2 = 0.
- ✓ Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage V1/2 at the non-inverting input terminal and the output becomes
  V01 = V1/2(1+R/R) = V1 when all resistances are R in the circuit.
- ✓ Similarly the output V02 due to V2 alone (with V1 grounded) can be written simply for an inverting amplifier as V02 = -V2
- ✓ Thus the output voltage Vo due to both the inputs can be written as V0 =V01 - V02 =V1 - V2

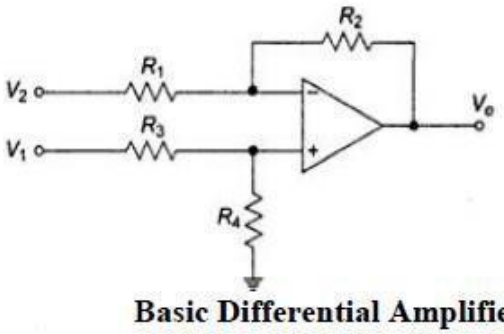
Adder/Subtractor:



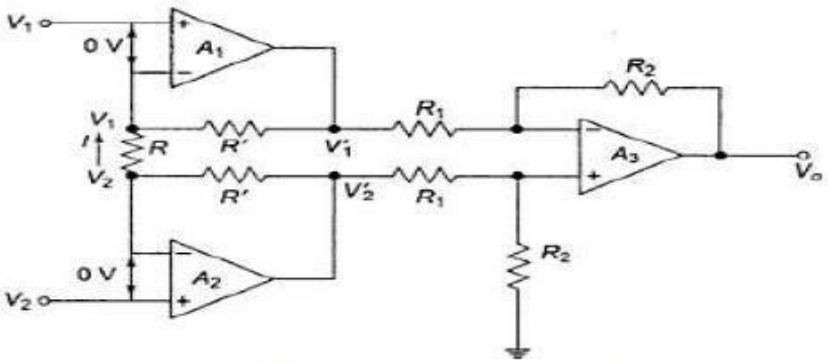
- ✓ It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure
- ✓ The output voltage Vo can be obtained by using superposition theorem.
- ✓ To find output voltage V01 due to V1 alone, make all other input voltages V2, V3 and V4 equal to zero.

Instrumentation Amplifier:

Explain operation of instrumentation amplifier. Name two applications of the same. (Nov 2003, May 2005, 2008, Dec 2018)



Basic Differential Amplifier



Instrumentation Amplifier

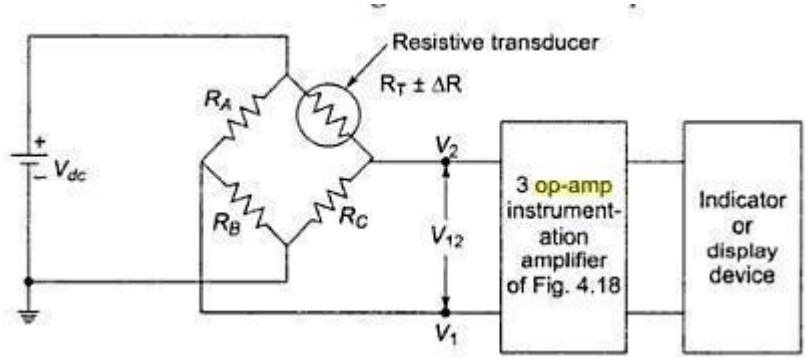
- ✓ Current flowing in resistor R is I= (V1-V2)/R and it flow through R' in the direction shown, Voltage at non-inverting terminal op-amp A3 is R2V1'/(R1+R2).
- ✓ By superposition theorem,
  Vo= (R2/R1)V1+(1+R2/R1)(R2V2/(R1+R2)=R2/R1(V1'-V2');
  V1'= R'I+V1=R'/R(V1-V2)+V1

V2'= R'I+V1=R'/R(V1-V2)+V2;

V0= (R2/R1)[(2R'/R(V2-V1)+ (V2-V1)]= (R2/R1)[(1+2R'/R)(V2-V1)

- ✓ In a number of industrial and consumer applications, one is required to measure and control physical quantities.
- ✓ Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers.
- ✓ The output of transducer has to be amplified so that it can drive the indicator or display system.
- ✓ This function is performed by an instrumentation amplifier.
- ✓ The important features of an instrumentation amplifier are

  1. High gain accuracy
  2. High CMRR
  3. High gain stability with low temperature coefficient
  4. Low output impedance
- ✓ There are specially designed op-amps such as μA725 to meet the above stated requirements of a good instrumentation amplifier.
- ✓ The op-amp A1 and A2 have differential input voltage as zero. For V1=V2, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifier.
- ✓ A1 acts as voltage follower, so its output V2'=V2. Similarly op-amp A2 acts as voltage follower having output V1'=V1. However, if V1≠V2, current flows in R and R', and (V2'-V1')> (V2- V1). Therefore, this circuit has differential gain and CMRR more compared to the single opamp circuit.
- ✓ The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity.
- ✓ To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.



- ✓ Figure shows a differential instrumentation amplifier using Transducer Bridge.

- ✓ The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to
- ✓ be measured.
- ✓ The bridge is initially balanced by a dc supply voltage Vdc so that V1=V2.
- ✓ As the physical quantity changes, the resistance RT of the transducer also changes, causing an unbalance in the bridge (V1≠V2).
- ✓ This differential voltage now gets amplified by the three opamp differential instrumentation amplifier.

$$R_B(V_{dc})/(R_B+R_A)= R_C V_{dc}/(R_C+R_T)$$

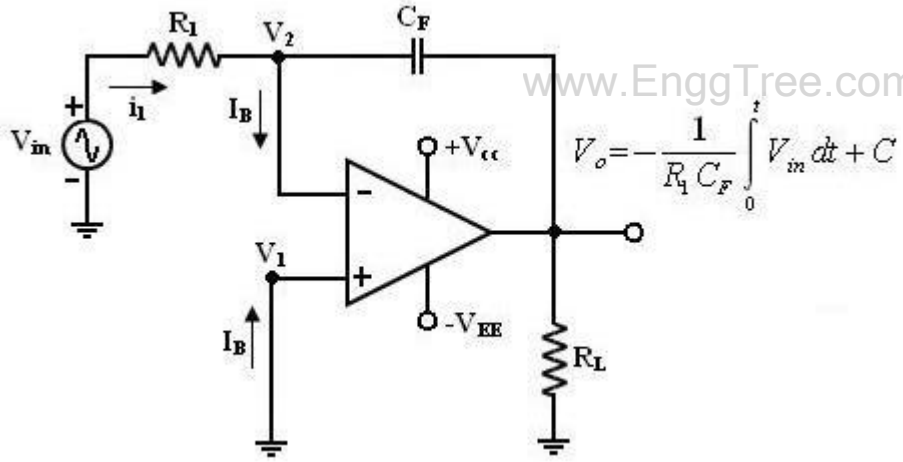
Applications of instrumentation amplifier with the transducer bridge:

- ✓ temperature indicator,
- ✓ temperature controller and
- ✓ light intensity meter

Integrator:

Q. Explain the circuit that provides an output voltage which is proportional to the time integral of the input. [Nov/Dec 2021][Nov/Dec 2022]

Draw the circuit of integrator using opamp. Explain the working. (Nov 2009)



- ✓ A circuit in which the output voltage is the integral of the input voltage is the integrator or Integration Amplifier.
- ✓ The expression for the output voltage V0 can be obtained by KVL eqn. at node V2.

$$i_1 = I_B + i_f$$

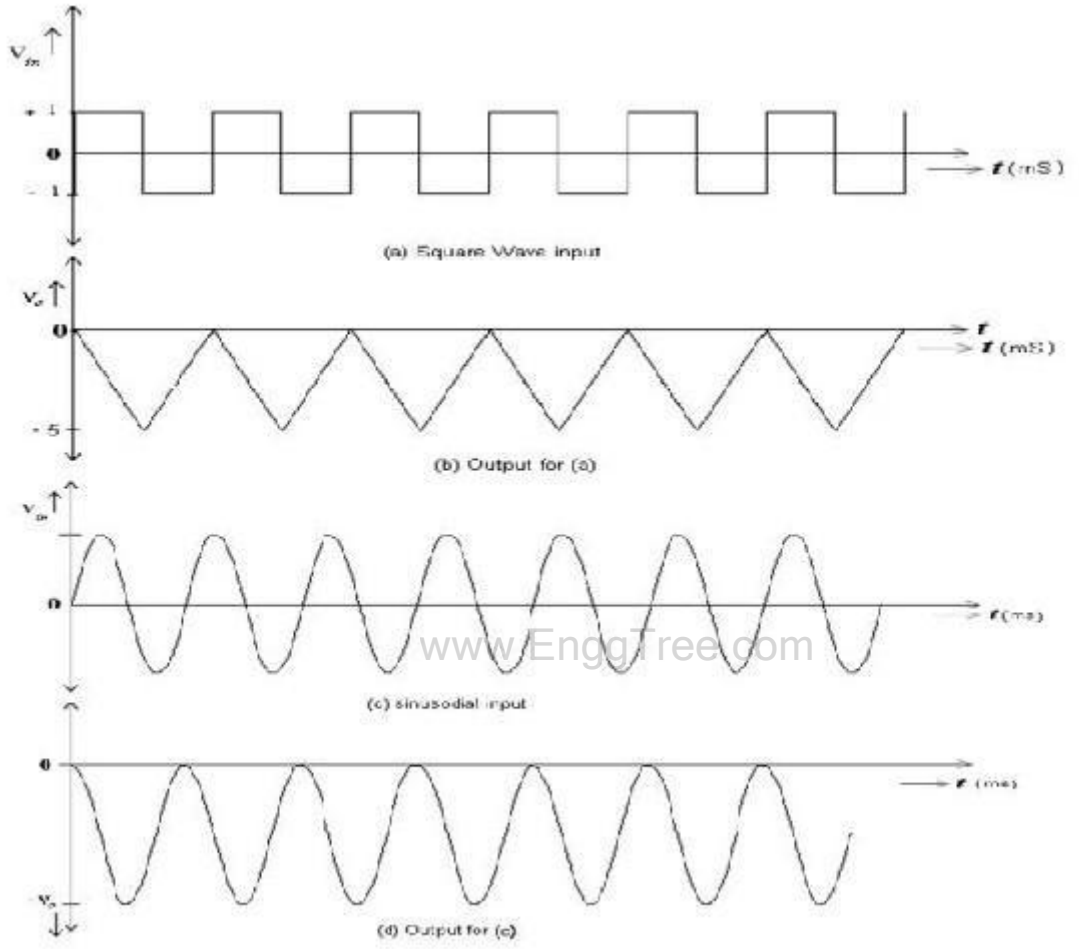
$$\text{Since } I_B \text{ is negligible small, } \quad i_1 = i_F$$

- ✓ Relation between current through and voltage across the capacitor is

$$i_{C(t)} = C dv_c(t)/dt$$

- ✓ The output voltage can be obtained by integrating both sides with respect to time

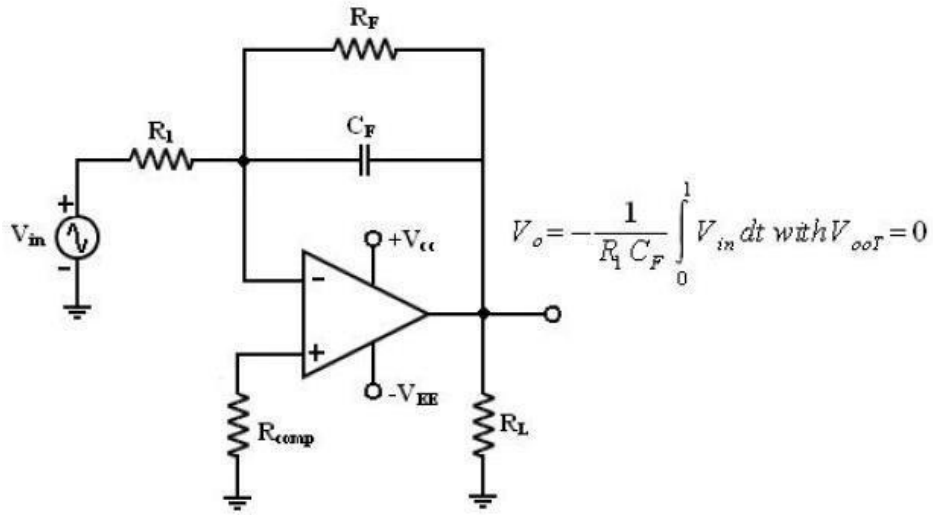
$$V_o = -\frac{1}{R_1 C_F}\int_0^t V_{in}\,dt + C$$



Practical Integrator:

- ✓ Practical Integrator reduce the error voltage at the output, a resistor RF is connected across the feedback capacitor CF.
- ✓ Thus RF limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$



$$V_o = -\frac{1}{R_1 C_F}\int_0^1 V_{in}\,dt \quad with V_{out} = 0$$

- ✓ Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor RF in the practical integrator.
  - Stability refers to a constant gain as frequency of an input signal is varied over a certain range.
  - Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.
- ✓ The gain limiting frequency fa is given by

$$f_a = \frac{1}{2\pi R_1 C_F}$$

- ✓ The value of fa and R1 CF and RF CF values should be selected such that fa<fb.
- ✓ The input signal will be integrated properly if the time period T of the signal is larger than or equal to RF CF,

$$f_b = \frac{1}{2\pi R_F C_F}$$

Uses:

Most commonly used in

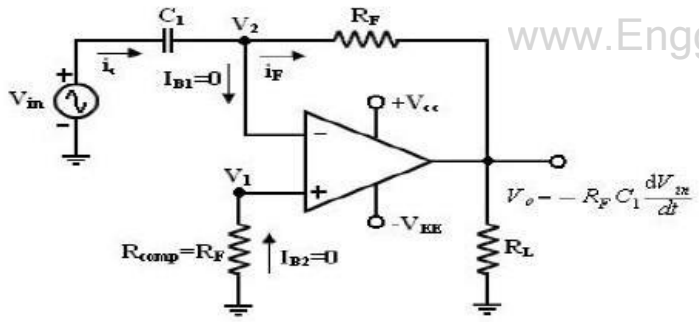
- Analog computers
- ADC
- Signal wave shaping circuits.

Differentiator:

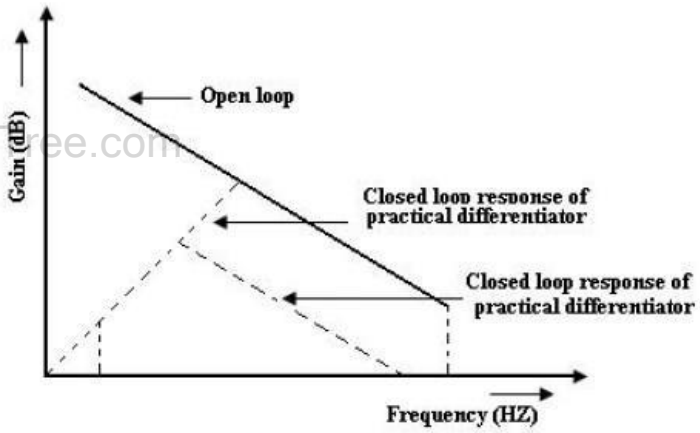
Draw the circuit of differentiator using op-amp. Explain the working. (Nov 2009)

Explain the circuit that performs the mathematical operation of differentiation. Draw its output wave form. [Nov/Dec 2021]

- ✓ The circuit performs the mathematical operation of differentiation (i.e.) the output waveform is the derivative of the input waveform.
- ✓ Since the differentiator performs the reverse of the integrator function. Thus the output V0 is equal to RF C1 times the negative rate of change of the input voltage Vin with time.
- ✓ The negative sign indicates a 180 phase shift of the output waveform V0 with respect to the input signal.
- ✓ The below circuit will not do this because it has some practical problems. The gain of the circuit (RF /XC1) R with R in frequency at a rate of 20dB/decade.
- ✓ This makes the circuit unstable. Also input impedance XC1s with R in frequency which makes the circuit very susceptible to high frequency noise.



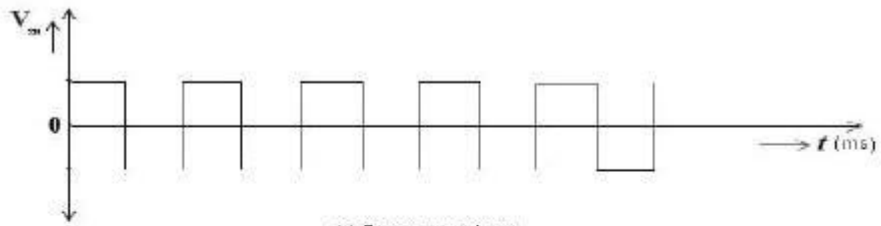
Basic Differentiator



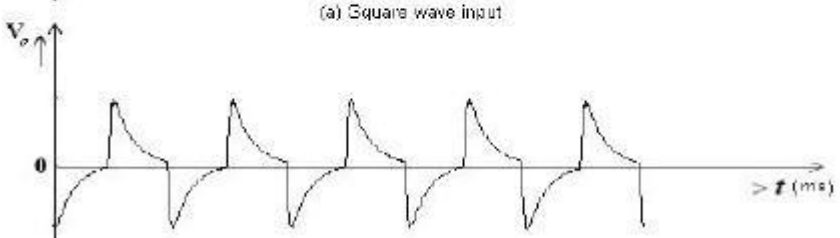
Frequency response of differentiator

- ✓ The output voltage can be obtained by differentiating input voltage with respect to time

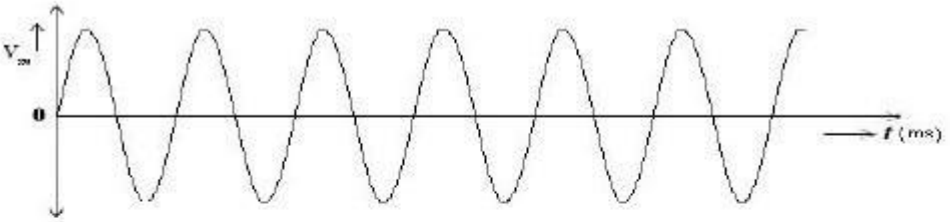
$$Vo_{(t)} = -RfC1\,dvin(t)/dt$$



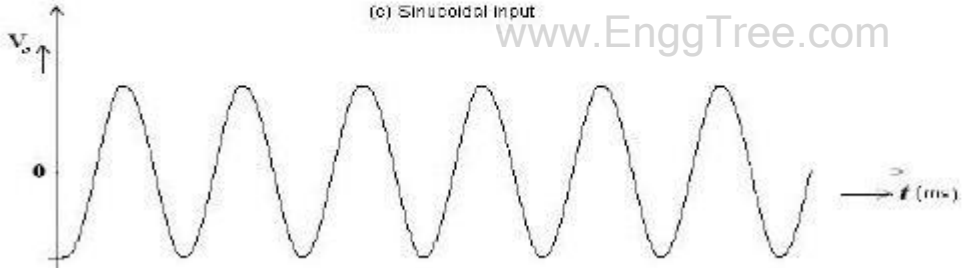
(a) Square wave input



(b) Output for (a)

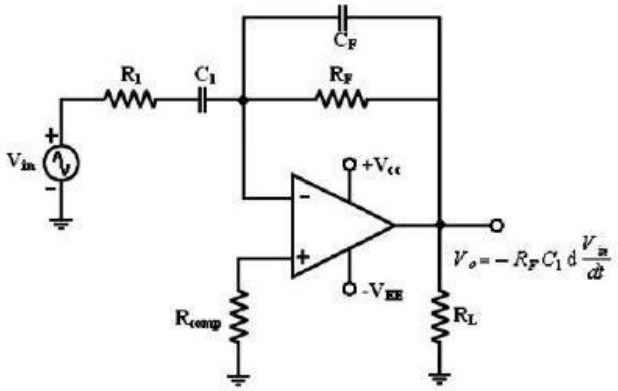


(c) Sinusoidal input



(d) Output for (c)

Practical Differentiator:



$$f_a = \frac{1}{2\pi R_f C_1}$$

$$f_b = \frac{1}{2\pi R_1 C_1}$$

A workable differentiator can be designed by implementing the following steps.

1. Select f_a equal to the highest frequency of the input signal to be differentiated then assuming a value of $C_1 < 1\mu f$. Calculate the value of RF.

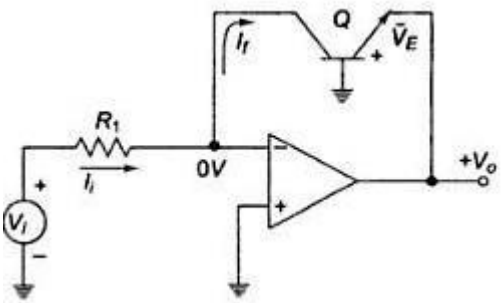
2. Choose $f_b = 20f_a$ and calculate the values of R_1 and C_F so that $R_1 C_1 = R_F C_F$.

Uses:

It is used in wave shaping circuits to detect high frequency components in an input signal and also as a rate of change and detector in FM modulators.

Log Amplifier:

Explain the working of log amplifier. (May 2008)



- ✓ A grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path.
- ✓ Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_S[e^{\frac{qV_{BE}}{kT}} - 1]$$

since $I_C = I_E$ for a grounded base transistor $I_C = Is\ e^{kT}$

Is=emitter saturation current ≈10-13A

k=Boltzmann's constant

T=absolute temperature (in o K)

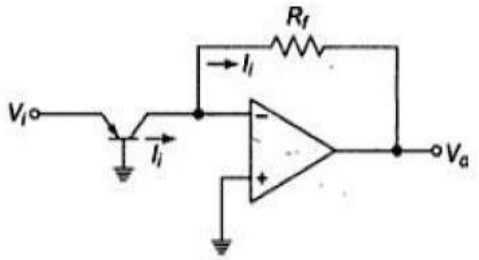
$$V_o = -\frac{kT}{q} ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

where Vref =R1Is

The output voltage is thus proportional to the logarithm of input voltage.

Antilog Amplifier

Explain the working of anti-log amplifier. (May 2005, Dec 2018)



$I_i = I_c = I_s(e^{\frac{\eta V_{BE}}{kT}})$ and $V_0 = R_f I_s(e^{\frac{\eta V_{BE}}{kT}})$

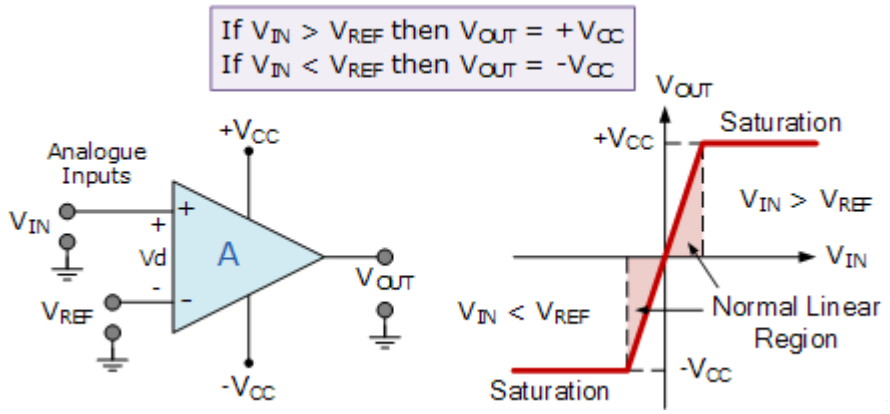
- A circuit to convert logarithmically encoded signal to real signals.
- Transistor in inverting input converts input voltage into logarithmically varying currents.

Comparator

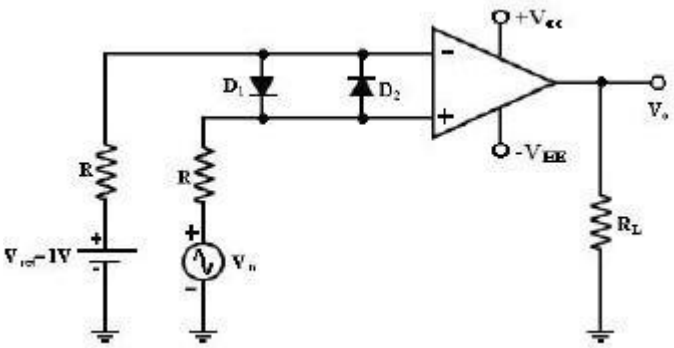
Explain the working of inverting and non-inverting comparator using op-amp.[Nov/Dec 2021]

A comparator compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

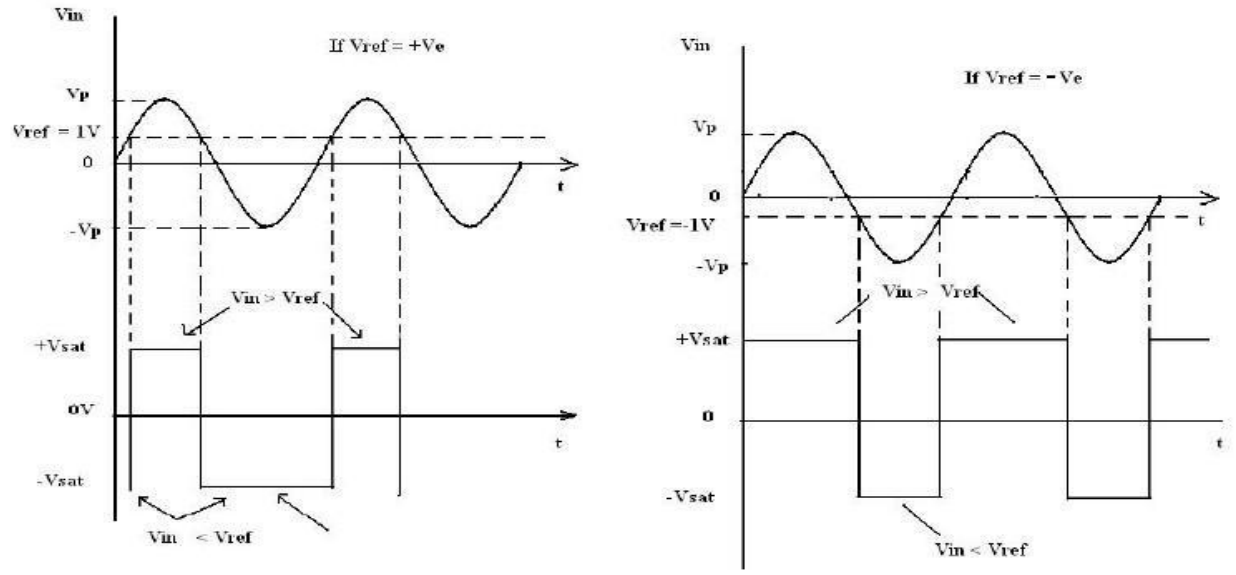
- Digital Interfacing
- Schmitt Trigger
- Discriminator
- Voltage level detector and oscillators



Non-inverting Comparator:



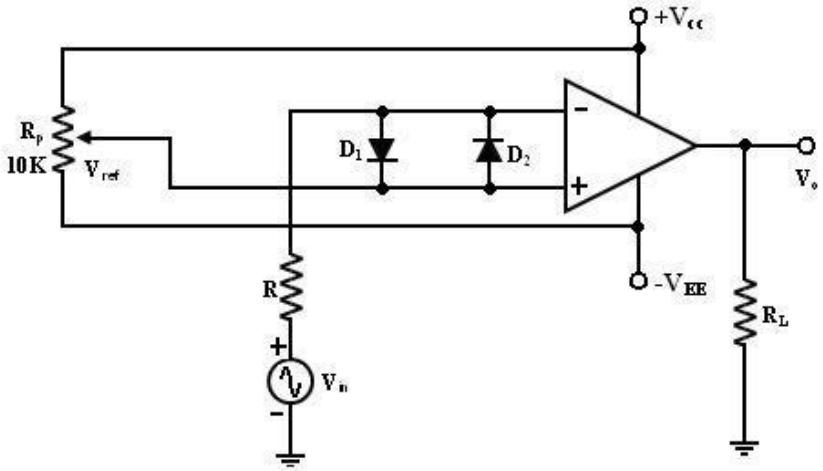
- ✓ A fixed reference voltage Vref of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied to the positive terminal.
- ✓ When Vin is less than Vref the output becomes V0 at –Vsat [Vin < Vref => V0 (-Vsat)].
- ✓ When Vin is greater than Vref, the (+) input becomes positive, V0 = +Vsat. [Vin > Vref => V0 (+Vsat)]. Thus the V0 changes from one saturation level to another.



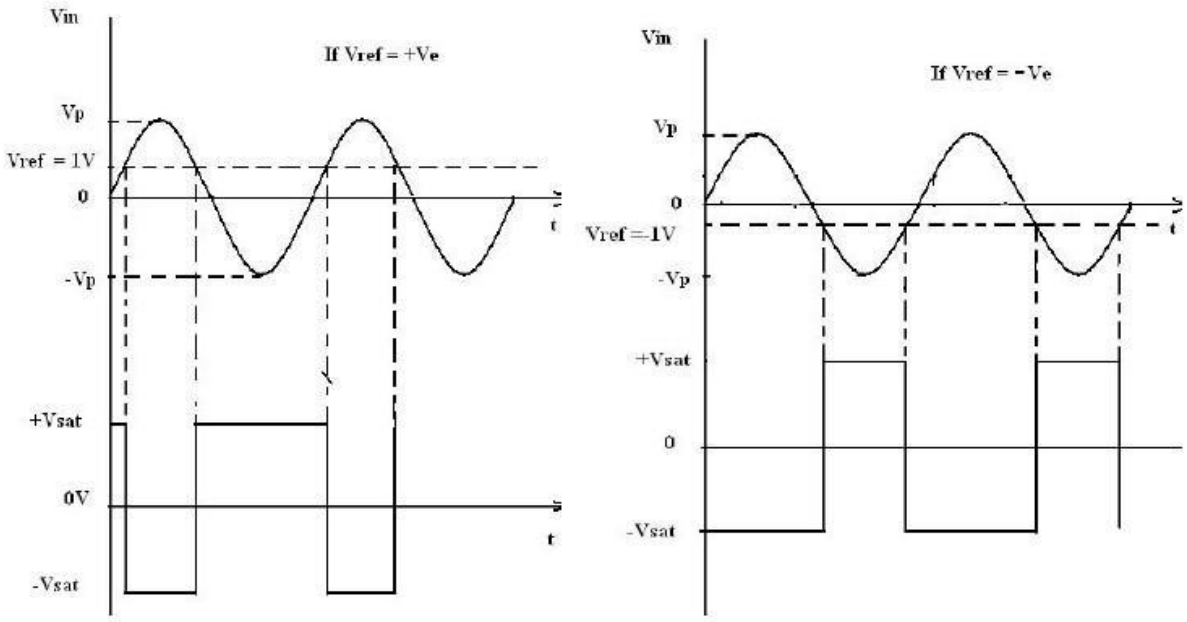
- ✓ The diodes D1 and D2 protect the op-amp from damage due to the excessive input voltage Vin. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes.
- ✓ The resistance R in series with Vin is used to limit the current through D1 and D2. To reduce offset problems, a resistance Rcomp = R is connected between the (-ve) input and Vref.

Inverting Comparator:

- ✓ This fig shows an inverting comparator in which the reference voltage Vref is applied to the (+) input terminal and Vin is applied to the (-) input terminal.



- ✓ In this circuit Vref is obtained by using a 10K potentiometer that forms a voltage divider with DC supply volt +Vcc and -1 and the wiper connected to the input.

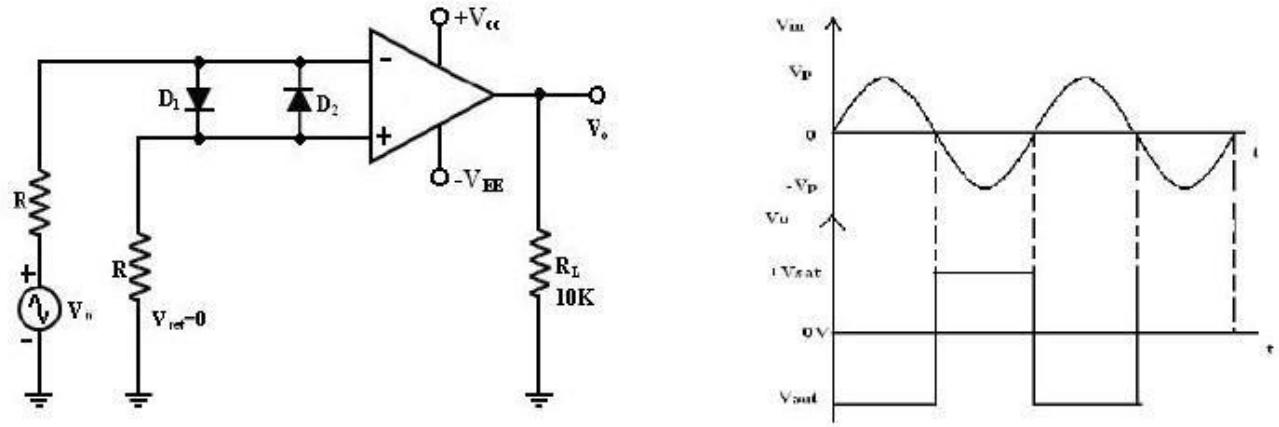


Applications:

Zero Crossing Detector: [Sine wave to Square wave converter]

Explain how comparator work as a zero crossing detector. (May 2004)

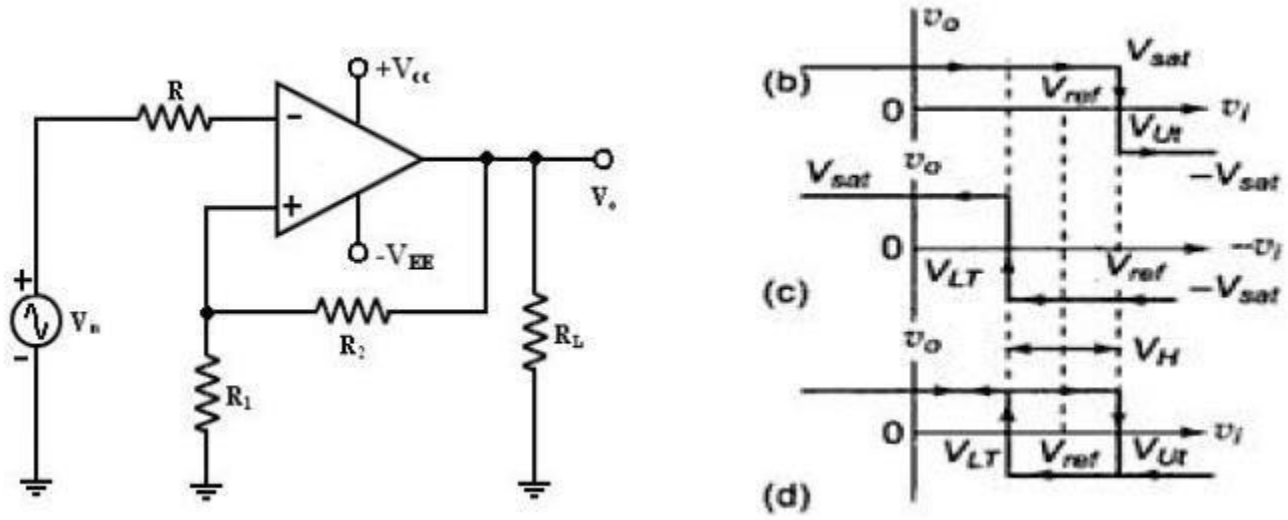
- ✓ The basic comparator can be used as a zero crossing detector by setting Vref is set to Zero.
- ✓ This Fig shows when in what direction an input signal Vin crosses zero volts. (i.e.) the output V0 is driven into negative saturation when the input the signal Vin passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V0 switches and saturates positively.



Schmitt Trigger: [Square Circuit]

Explain the operation of schmitt trigger. (Nov 2008, Dec 2018)
Describe the circuit and working of a square-wave generator. [Nov/Dec 2021] [Nov/Dec 2022]

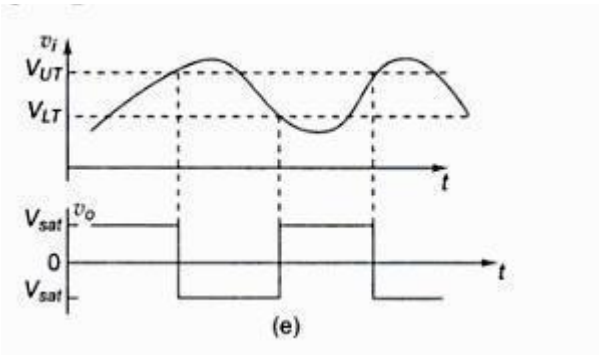
This circuit converts an irregular shaped waveform to a square wave or pulse. The input voltage Vin triggers (changes the state of) the output Vo every time it exceeds certain voltage levels called the upper threshold Vut and lower threshold Vlt voltage.



- ✓ These threshold voltages are obtained by using the voltage divider R1– R2, where the voltage across R_1 is feedback to the (+) input.
- ✓ The voltage across $R_1$is variable reference threshold voltage that depends on the value of the output voltage. When V0 = +Vsat, the voltage across R1 is called upper threshold voltage Vut.
- ✓ The input voltage Vin must be more positive than Vut in order to cause the output V0 to switch from +Vsat to -Vsat using voltage divider rule, Voltage at (+) input terminal is

$$V_{UT}=V_{ref}+ R_2 (V_{sat}-V_{ref})/(R_1+R_2) \text{ when } V_0= +v_{sat.}$$

- ✓ When v0= -vsat. Hysteris width $V_H= V_{UT} - V_{LT} = 2 R_2 (V_{sat})/ (R_1+R_2)$
- ✓ When V0 = -Vsat, the voltage across R1 is called lower threshold voltage Vlt .the Vin must be more negative than Vlt in order to cause V0 to switch from –Vsat to +Vsat. for Vin > Vlt , V0 is at –Vsat.
- ✓ Voltage at (+) terminal is $V_{LT}=V_{ref} - R_2 (V_{sat}+V_{ref})/(R_1+R_2)$.
  - If the threshold voltages Vut and Vlt are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions.
  - Also the positive feedback, because of its regenerative action, will make V0 switch faster between +Vsat and –Vsat.
  - Resistance Rcomp=R1 || R2 is used to minimize the offset problems.



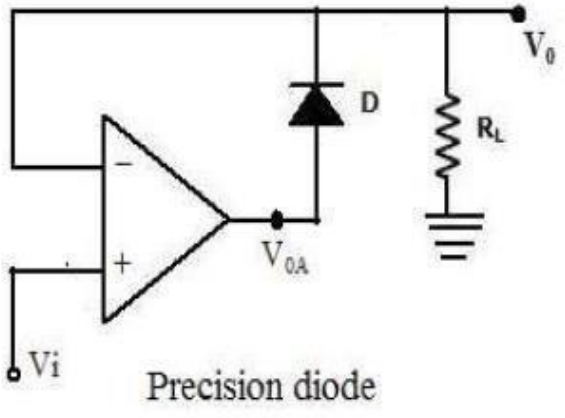
- The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) hen the input of the comparator exceeds Vut its output switches from +Vsat to –Vsat and reverts to its original state, +Vsat when the input goes below VLT.

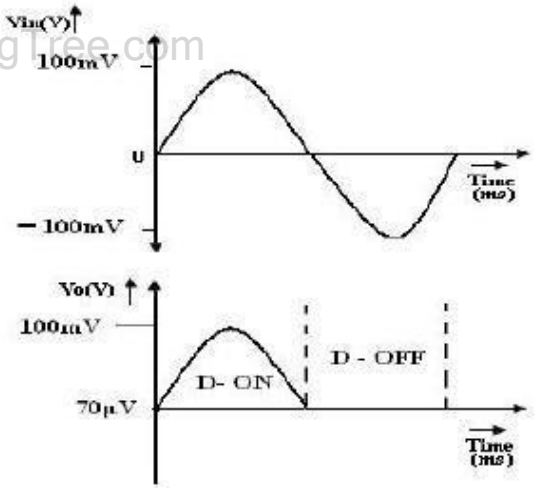
- The hysteresis voltage is equal to the difference between Vut and Vlt. Therefore VH= Vut – Vlt.
- If Vref=0, Vut= -VLT =2 R2(Vsat)/(R1+R2)

Precision Rectifier:

The ordinary diodes cannot rectify voltages below the cut-in-voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

Precision diodes:





- ✓ Figure shows the arrangement of a precision diode. It is a single diode arrangement and functions as a non-inverting precision half– wave rectifier circuit.
- ✓ If V1 in the circuit of figure is positive, the op-amp output VOA also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage V0 = Vi . When Vi < 0, the voltage V0A becomes negative and the diode is reverse biased. The loop is then broken and the output V0 = 0.

- ✓ Consider the open loop gain AOL of the op-amp is approximately 10^4 and the cut-in voltage Vγ for silicon diode is ≈ 0.7V. When the input voltage Vi > Vγ / AOL, the output of the op-amp VOA exceeds Vγ and the diode D conducts.

Applications: The precision diodes are used in

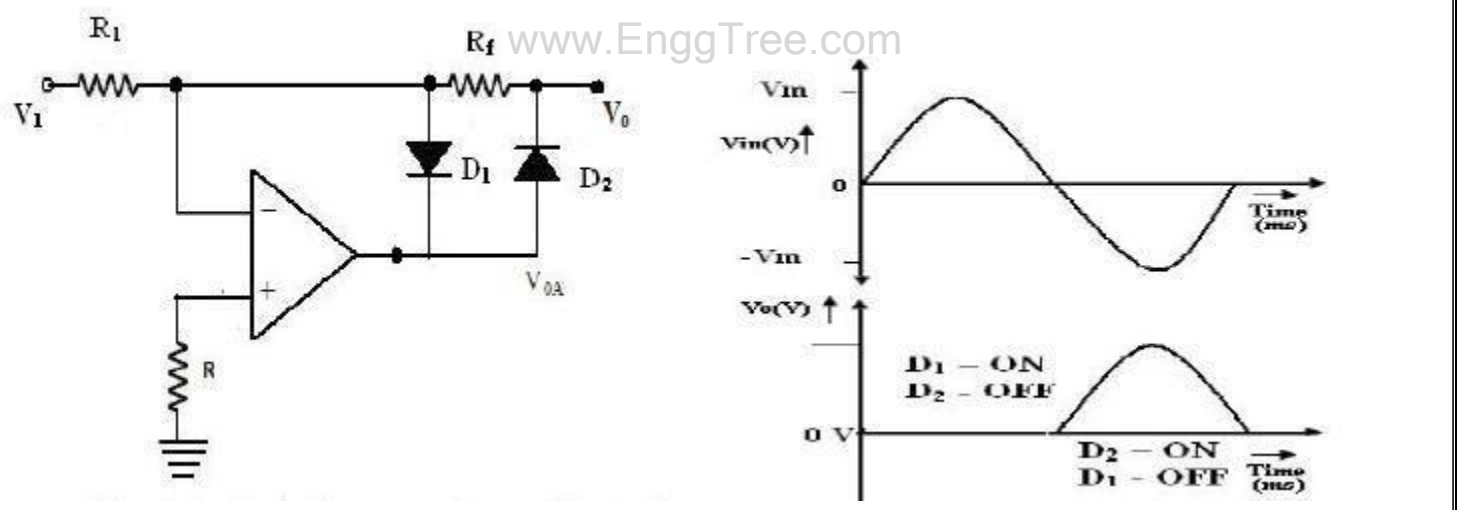
- ✓ half wave rectifier,
- ✓ Full-wave rectifier,
- ✓ peak value detector,
- ✓ Clipper and clamper circuits.

Disadvantage:

It can be observed that the precision diode as shown in figure operated in the first quadrant with Vi > 0 and V0 > 0. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

Half – wave Rectifier:

What is precision rectifier? With circuit schematic explain the working principles of half wave rectifier. (Nov 2007)



- ✓ A non-saturating half wave precision rectifier circuit is shown in figure.
- ✓ When Vi > 0V, the voltage at the inverting input becomes positive, forcing the output VOA to go negative.
- ✓ This results in forward biasing the diode D1 and the op-amp output drops only by ≈ 0.7V below the inverting input voltage. Diode D2 becomes reverse biased. The output voltage V0 is zero when the input is positive.

- ✓ When Vi > 0, the op-amp output VOA becomes positive, forward biasing the diode D2 and reverse biasing the diode D1. The circuit then acts like an inverting amplifier circuit with a nonlinear diode in the forward path. The gain of the circuit is unity when Rf = Ri
- ✓ The circuit operation can mathematically be expressed as

  $V_0 = 0$ when $V_i > 0$ and

  $V_0 = R_f/R_i V_1$ for $V_i < 0$
- ✓ The voltage V_{OA} at the op amp output is $V_{OA} = -0.7V$ for $V_i > 0$

  $V_{OA} = R_f/R_i V_1 + 0.7V$ for $V_i < 0$

Advantages:

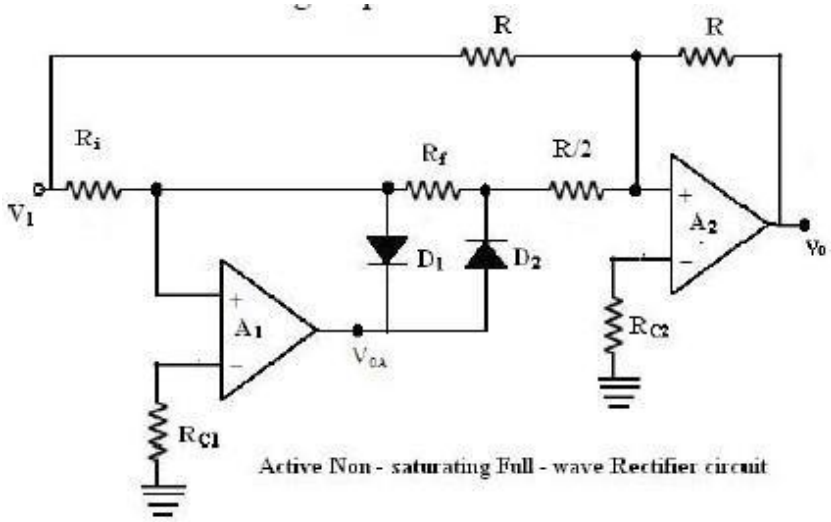
- ✓ It is a precision half wave rectifier and
- ✓ Iit is a non-saturating one.

The inverting characteristics of the output V0 can be circumvented by the use of an additional inversion for achieving a positive output.

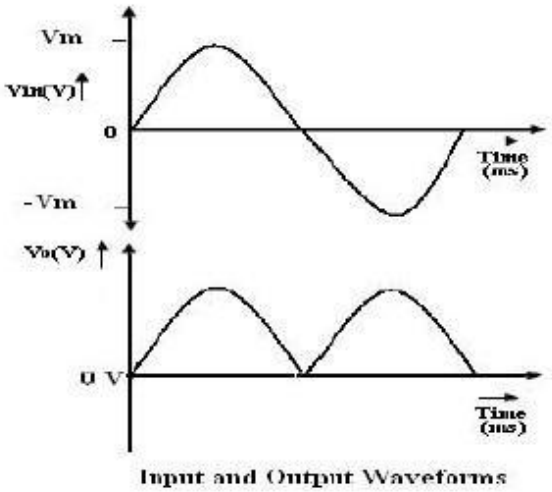
Full wave Rectifier:

What is precision rectifier? With circuit schematic explain the working principles of Full wave rectifier. (Nov 2008)

The first part of the Full wave circuit is a half wave rectifier circuit. The second part of the circuit is an inverting amplifier.



Active Non - saturating Full - wave Rectifier circuit



Input and Output Waveforms

- ✓ For positive input voltage Vi > 0V and assuming that RF =Ri = R, the output voltage VOA = Vi. The voltage V0 appears as (-) input to the summing op-amp circuit formed by A2, The gain for the input V‘0 is R/(R/2), as shown in figure.
- ✓ The input Vi also appears as an input to the summing amplifier.

- ✓ Then, the net output is V0 =-Vi -2V0= -Vi -2(-Vi) = Vi. Since Vi > 0V, V0 will be positive, with its input output characteristics in first quadrant.
- ✓ For negative input Vi < 0V, the output V‘0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero.
- ✓ However, Vi is also applied as an input to the summer circuit formed by the op-amp A2.
- ✓ The gain for this input id (-R/R) = -1, and hence the output is V0 = -Vi. Since Vi is negative, V0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.
- ✓ To summarize the operation of the circuit,

V0 = Vi when Vi < 0V and

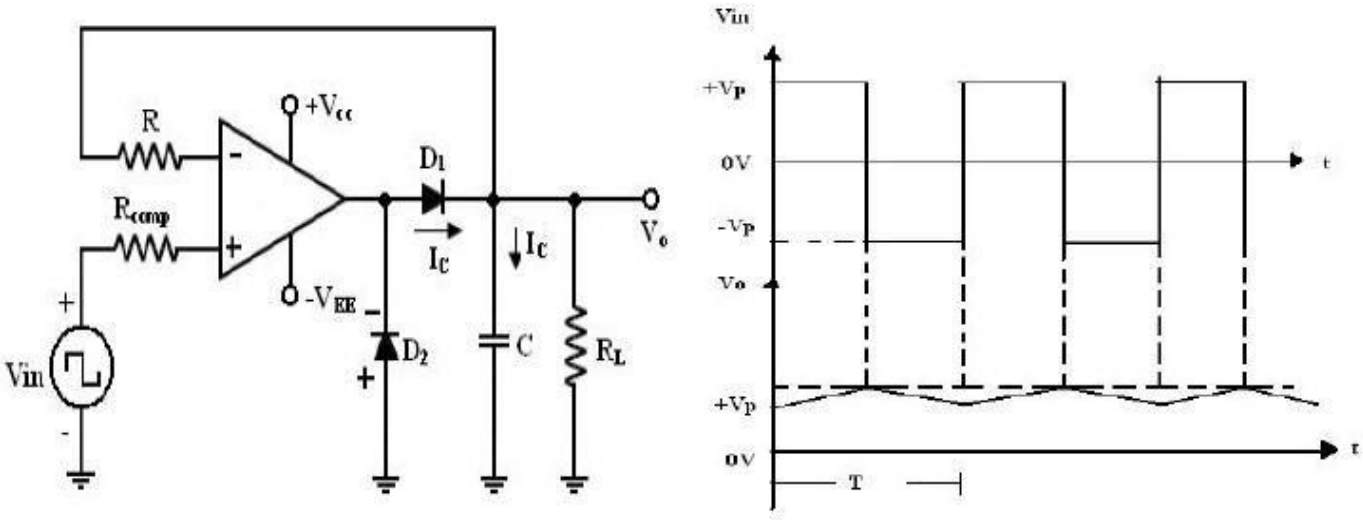
V0 = Vi for Vi > 0V, and hence

V0 = |Vi |

Peak Detector

What is peak detector? Draw the circuit using op-amp.

- ✓ Peak detector measures the +ve peak value of the square wave input.
- ✓ Square, Triangular, Saw tooth and pulse waves are typical examples of non-sinusoidal waveforms.
- ✓ A conventional AC voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the RMS value of the pure sine wave.



- ✓ One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms.

i) During the positive half cycle of Vin: the o/p of the op-amp drives D1 on. (Forward biased) Charging capacitor C to the positive peak value Vp of the input volt Vin.

ii) During the negative half cycle of Vin: D1 is reverse biased and voltage across C is retained. The only discharge path for C is through RL since the input bias IB is negligible.

For proper operation of the circuit, the charging time constant (CRd) and discharging time constant (CR_L) must satisfy the following condition.

CRd <= T/10

Where Rd = Resistance of the forward-biased diode.

T = time period of the input waveform.

CRL >= 10T

Where R_L = load resistor.

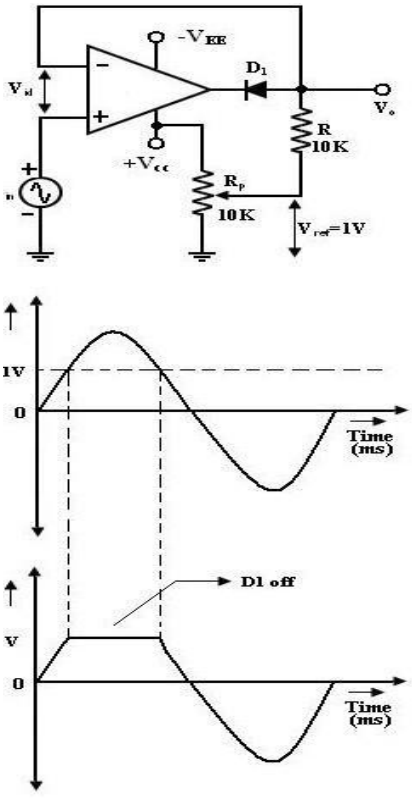
Note: Negative peak of the input signal can be detected simply by reversing diode D1 and D2.

Clipper:

What is clipper? With circuit schematic explain the working of positive and negative clipper.

A circuit that removes parts of the input signal is called clipper. It can be formed by using an op-amp with a rectifier diode.

Positive Clipper:

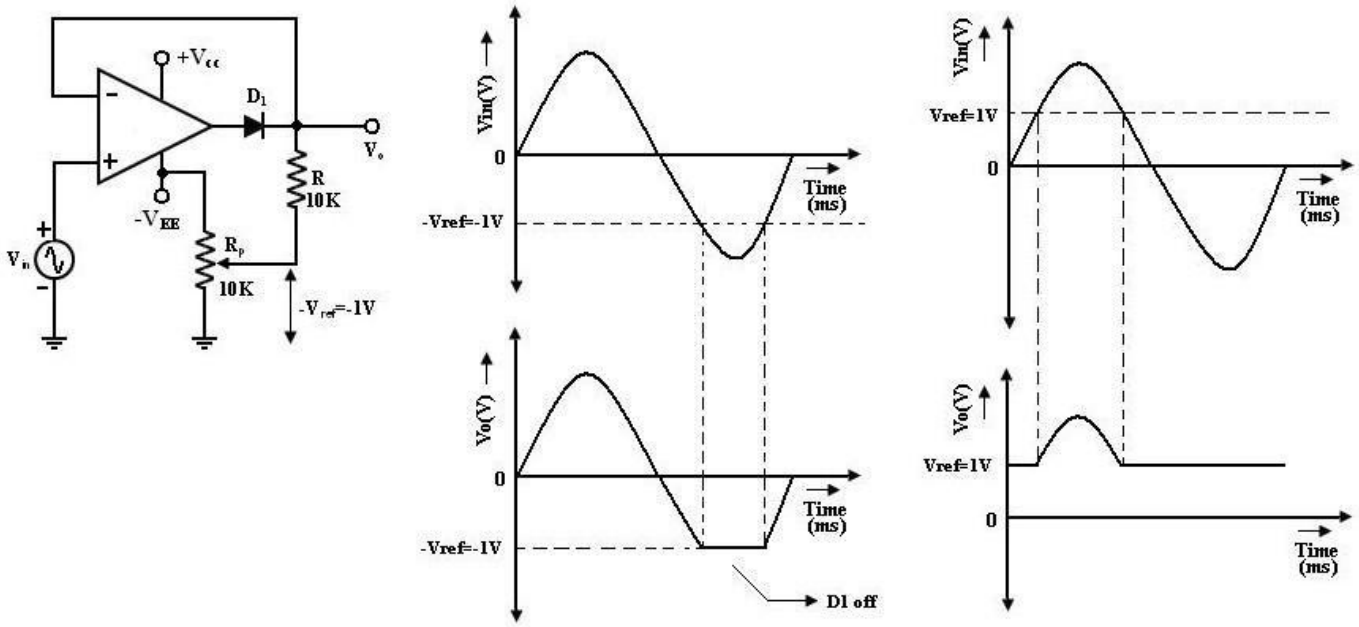


- ✓ A circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode.
- ✓ The clipping level is determined by the reference voltage Vref.
- ✓ if $V_{ref} < V_{in}$, The Output voltage has the portions of the positive half cycles above V_{ref} clipped off.

Operation:

- ✓ During the positive half cycle of the input, the diode D1 conducts only until Vin = Vref.
- ✓ Output V0 follows input until Vin = Vref.
- ✓ When Vin > Vref => the V0 becomes +ve to derive D1 into off. It opens the feedback loop and op-amp operates open loop.
- ✓ When Vin drops below Vref (Vin<Vref) the o/p of the op-amp V0 again becomes –ve to device D1 into conduction. It closes the feedback path. (o/p follows the i/p).
- ✓ Thus diode D1 is on for vin<Vref (o/p follows the i/p) and D1 is off for Vin>Vref.

Negative Clipper

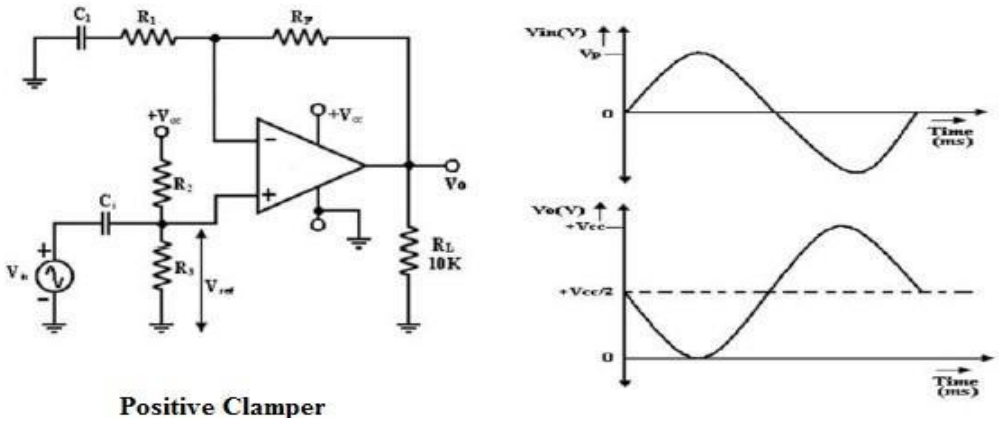


- ✓ The positive clipper is converted into a –ve clipper by simply reversing diode D1 and changing the polarity of Vref voltage.
- ✓ The negative clipper clips off the –ve parts of the input signal below the reference voltage.
- ✓ Diode D1 conducts -> when Vin > -Vref and therefore during this period o/p volt V0 follows the input volt Vin.
- ✓ The negative portion of the output volt below –Vref is clipped off because (D1 is off) Vin<-Vref.

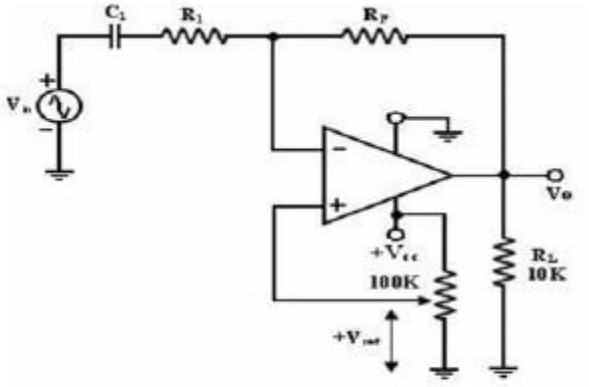
Positive and Negative Clampers:

In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

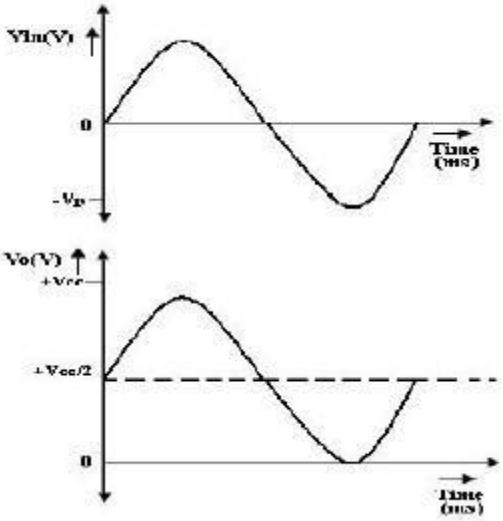
1. If the clamped dc level is +ve, the clamper is positive clamper
2. If the clamped dc level is –ve, the clamper is negative clamper.



Positive Clamper

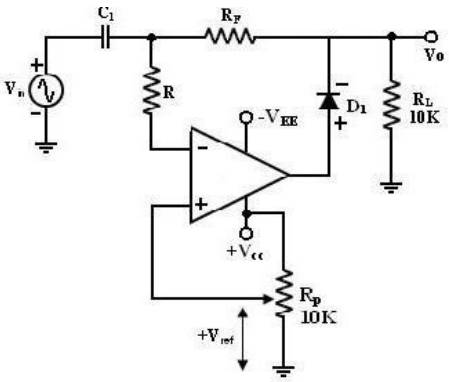


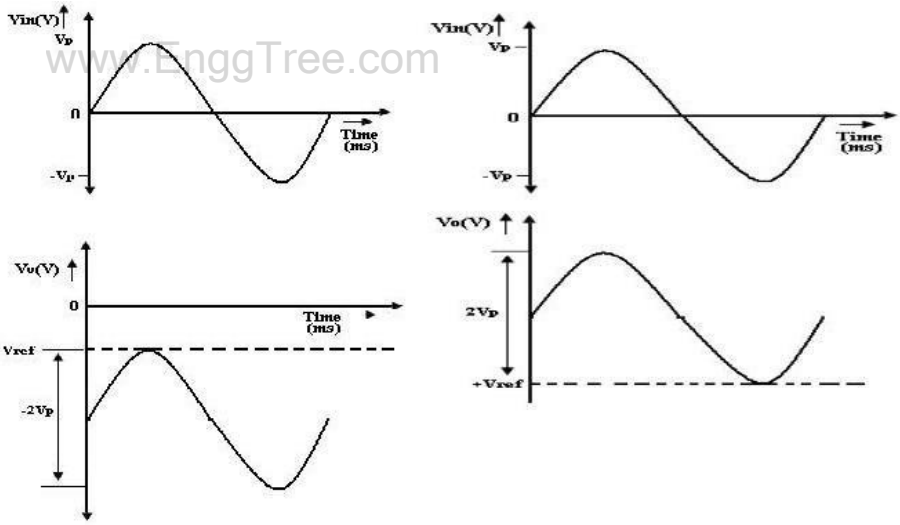
Negative Clamper



Peak clamper:

In this circuit, the input waveform peak is clamped at Vref. For this reason, the circuit is called the peak clamper.





- ✓ First consider the input voltage Vref at the (+) input: since this volt is +ve, V‘0 is also +ve which forward biases D1. This closed the feedback loop.
- ✓ Voltage Vin at the (-) input: During its –ve half cycle, diode D1 conducts, charging c; to the –ve peak value of Vp.
- ✓ During the +ve half cycle, diode D1 in reverse biased. Since this voltage Vp is in series with the +ve peak volt Vp the o/p volt V0 = 2 Vp. Thus the nett o/p is Vref plus 2 Vp. So the – ve peak of 2 Vp is at Vref. For precision clamping, CiRd << T/2.

Where Rd = resistance of diode D1 when it is forward biased.

T = time period of the input waveform.

- ✓ Resistor R is used to protect the op-amp against excessive discharge currents from capacitor Ci especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by reversing D1 and using –ve reference voltage (-Vref).

Note: Inv and Non-Inv clamper – Fixed dc level, Peak clamper – Variable dc level

Active filters:

An electric filter is circuit that passes a specified band of frequencies and blocks signal at frequencies outside this band.

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

Active filters offer the following advantages over passive filters:

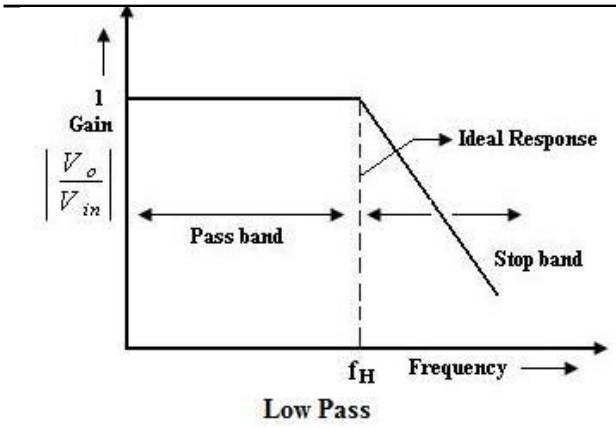
1. Gain and Frequency adjustment flexibility.
2. No loading problem:
3. Cost: Active filters are more economical than passive filter.

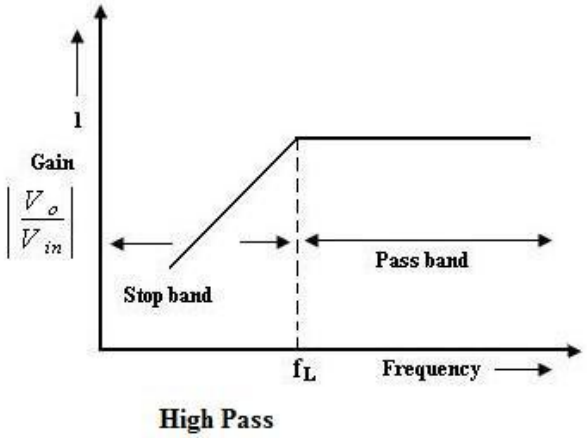
The most commonly used filters are these:

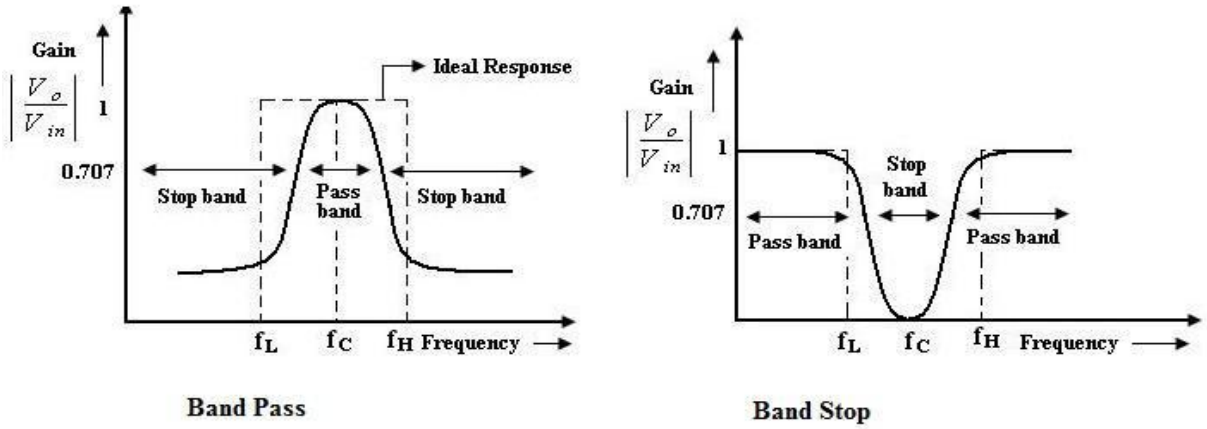
1. Low pass Filters
2. High pass Filters
3. Band pass filters
4. Band –reject filters
5. All pass filters.

Frequency response of the active filters:

Compare the frequency response of Active filters. (Nov 2016)

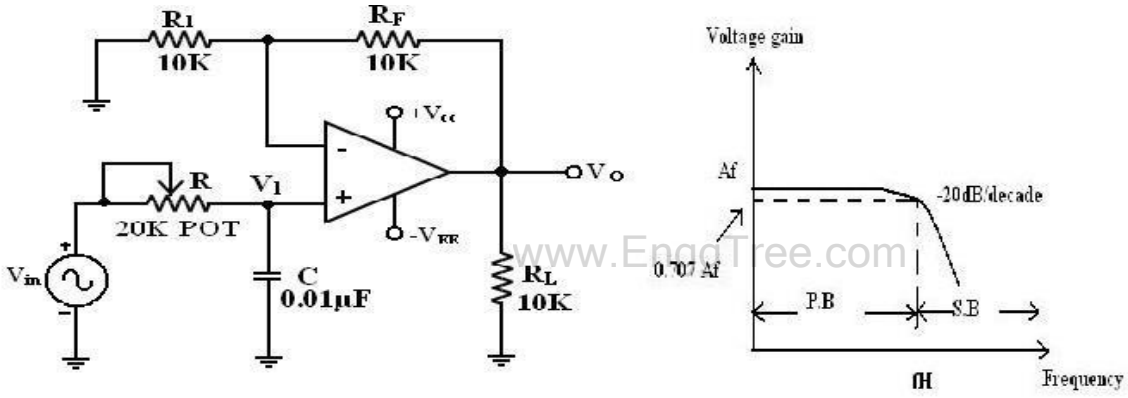






Design First order Low Pass Butterworth filter: **(Dec 2018)**

First order LPF that uses an RC for filtering op-amp is used in the non-inverting configuration. Resistor R1 & Rf determine the gain of the filter.



Gain A= $(1+R_f/R_1)$

Voltage across capacitor $V_1 = V_i / (1+j2\pi fRC)$

Output voltage V0 for non inverting amplifier $=AV_1 = (1+R_f/R_1)\, V_i/(1+j2\pi fRC)$

Overall gain $V0/Vi = (1+R_f/R_1)\, V_i/(1+j2\pi fRC$

Transfer function $H(s) = A/(jf/f_h+1)$ if $f_h = 1/2\pi RC$

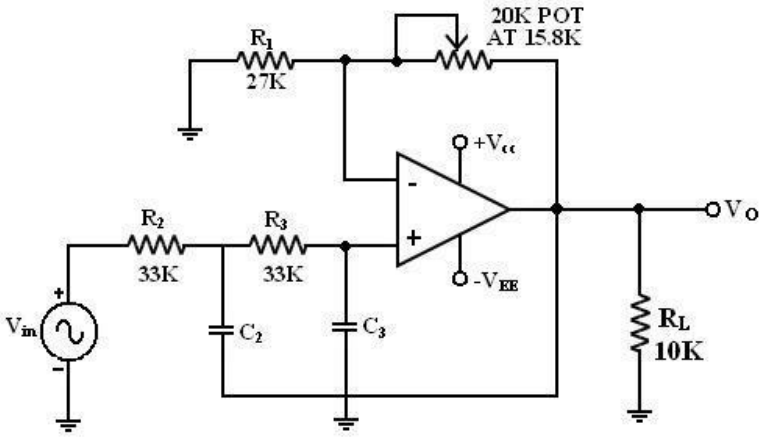
$H(j\omega) = A/(j RC+1) = A/(j RC+1)$.

Filter design:

A LPF can be designed by implementing the following steps.

1. Choose a value of high cut off frequency fH**.**
2. Select a value of C less than or equal to 1µf.
3. Choose the value of R using $f_h = 1/2\pi RC$
4. Finally select values of R1 and RF dependent on the desired pass band gain AF Using A= (1+Rf/R1)

Second order Low Pass Butterworth filter:



Filter Design:

1. Choose a value for a high cut off freq. (fH).

2. To simplify the design calculations, set R2 = R3 = R and C2 = C3 = C then choose a value of C<=1μf.

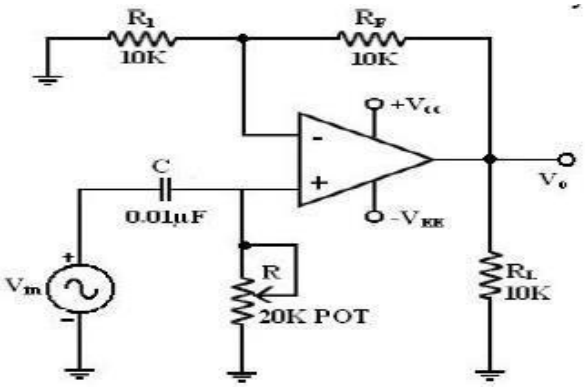
3. Calculate the value of R, $R = 1/2\pi f_h C$

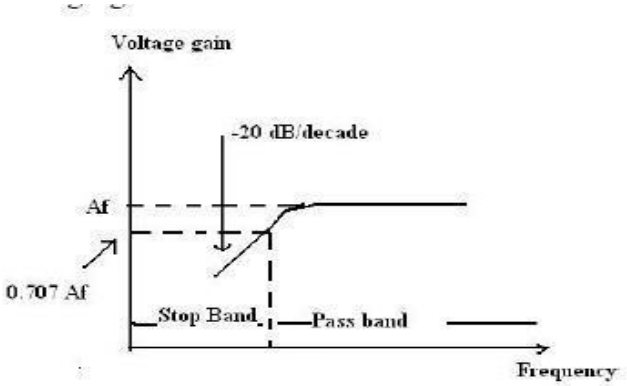
4. Finally, because of the equal resistor (R2 = R3) and capacitor (C2 = C3) values, the pass band volt gain AF = 1 + RF / R1 of the second order had to be = to 1.586. RF = 0.586 R1. Hence choose a value of R1<=100kΩ.

5. Calculate the value of RF.

First order High Pass Butterworth filter:

High pass filters are formed by interchanging frequency-determining resistors and capacitors in low-pass filters.



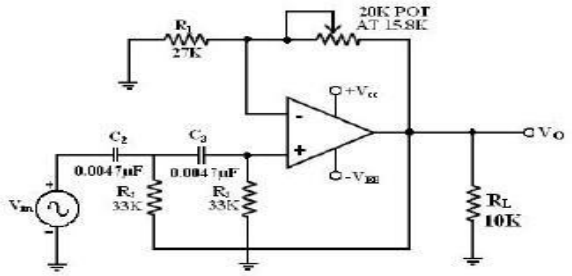


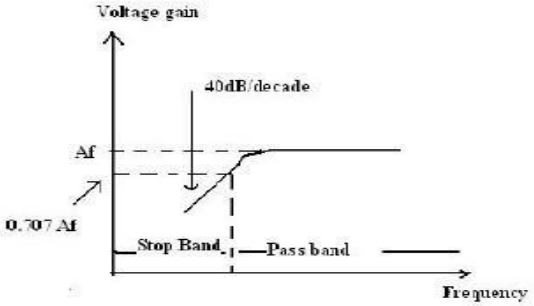
At high frequencies f>fL gain = A.

- ✓ At f= fL gain = 0.707 A.
- ✓ At f < fL the gain decreases at a rate of -20 db /decade.

The frequency below cutoff frequency is stop band.

Second – order High Pass Butterworth Filter:





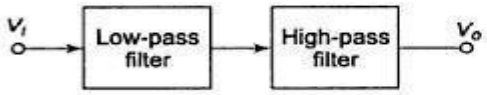
Band pass filters

Filters that pass band of frequencies and attenuates others. Its high cutoff frequency and low cutoff frequency are related as $f_H > f_L$ and maximum gain at resonant frequency $f_r = f_H f_L$

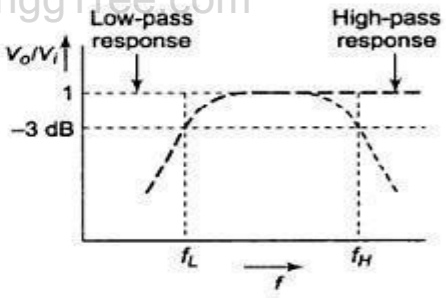
- ✓ Figure of merit $Q = f_r / (f_H - f_L) = f_r/B$ where B= bandwidth.
- ✓ Two types of filters are Narrow band pass and wide band pass filters

Wide band pass filter:

It is connection of a low pass filter and a high pass filter in cascade. The f_H of low pass filter and f_L of high pass filter are related as $f_H > f_L$.

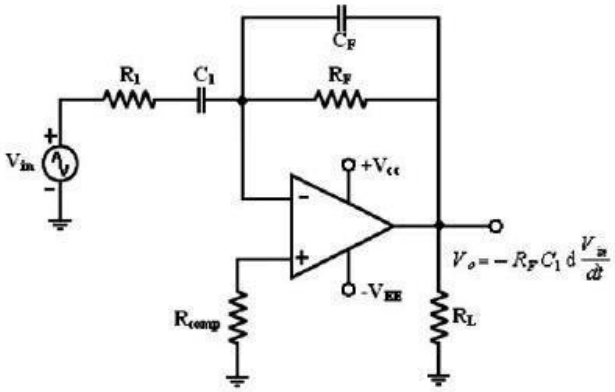


(a)



(b)

1. **Design an op amp differentiator that will differentiate an input signal with f_{max} = 100Hz.** **[Nov/Dec 2021]** [Nov/Dec 2022]



$$f_a = \frac{1}{2\pi R_f C_1}$$

$$f_b = \frac{1}{2\pi R_1 C_1}$$

100 = 1/(2*3.14*0.1*R)

R = 1/(0.628*100)

R= 0.015Ohm.

UNIT II

APPLICATIONS OF OP – AMPS

1. What do you meant by linear circuits?

Linear circuits are the circuits in which the output signal varies with the input signal in a linear manner.

2. What do you meant by non linear circuits?

Non linear circuits are the circuits in which the output signal does not vary with the input signal.

3. Mention some of the linear applications of op – amps.(Nov/Dec' 2005)

Adder, subtractor, voltage –to- current converter, current –to- voltage converters, instrumentation amplifier, analog computation, power amplifier, etc are some of the Linear op-amp circuits.

4. Mention some of the non – linear applications of op-amps. (Nov/Dec'2005)

Rectifier, peak detector, clipper, clamper, sample and hold circuit, log amplifier, anti –log amplifier, multiplier are some of the non – linear op-amp circuits.

5. What are the areas of application of non-linear op- amp circuits?

The applications of non-linear op-amp are:

- . Industrial instrumentation
- . Communication
- . Signal processing

6. What is an inverting amplifier?

Inverting amplifier is the one in which a signal is applied to the inverting input terminal. The output voltage is fed back to the inverting input terminal through feedback resistance (R_f) - input resistance (R_I) network. The output signal is the amplified form of input signal with a phase shift of 180°

7. What is a non- inverting amplifier?

Non inverting amplifier is the one in which a signal is applied to the non-inverting input terminal and the output is fed back to the inverting input terminal, the circuit amplifies without inverting the input signal.

8. Give an application of an inverting amplifier.[May/June 2013]

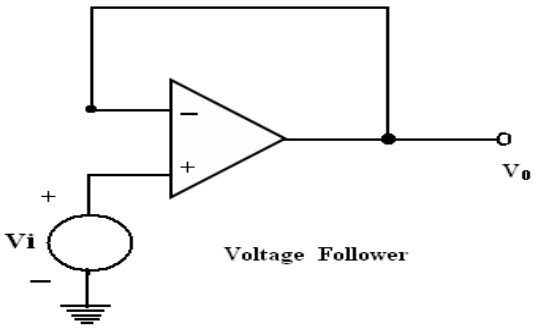
Sign changer is a typical application of an inverting amplifier. It is a special case with $R_f = R_1$ and hence $(V_0/V_{in}) = -1$

9. What is voltage follower? [April/May 2010, May/June 2014]

(OR)

What is an op-amp buffer? Draw the diagram. [Nov/Dec 2010]

A circuit in which the output voltage follows the input voltage is called voltage follower circuit. That is output voltage is equal to input voltage. This circuit is also called as op-amp buffer.



10. What are the applications of V-I converter?

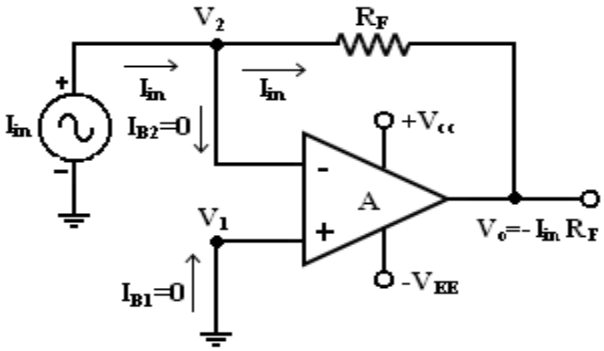
The applications of V-I converter are:

a. Low voltage dc and ac voltmeter
b. L E D
c. Zener diode tester

14. Give applications of voltage to current t converters.

The main applications of voltage to current converter are, LED & Zener diode tester Low voltage AC & DC voltmeters.

15. Give the schematic of op-amp based current to voltage converter. (April/May 2010)



16. Give the circuit of a voltage to current op-amp converter. [April/May 2011]

There are two circuits available for voltage to current converter

- ✓ V to I converter with floating load
- ✓ V to I with grounded load.

17. What is meant by summer (summing amplifier)?

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called summing amplifier or summer.

18. Draw the averaging circuit using operational amplifier. [Nov/Dec 2009]

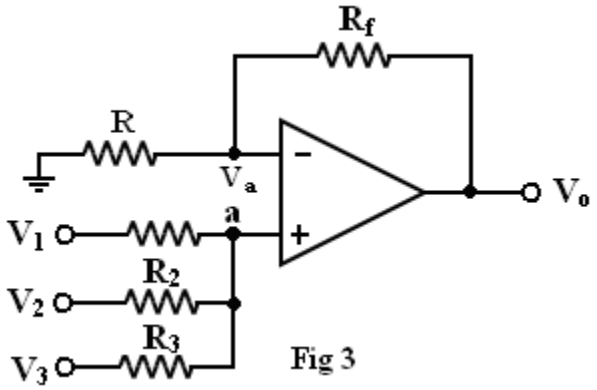


Fig 3

19. What is an instrumentation amplifier?

It is intended for precise, low- level signal amplification where noise, low thermal drift low. An Instrumentation is useful for amplifying low level signals which are obtained by sensing with a transducer in the measurement of physical quantities like temperature, water flow.

20. What is the need for an instrumentation amplifier? (May/June 2012)

In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

21. What is the major function of instrumentation amplifier?

To amplify the low level output signal of a transducer so that it can drive the indicator or display is the major function of an instrumentation amplifier.

22. List the features of instrumentation amplifier. (Nov/Dec'2013, April/May 2011,Nov/Dec 2004)

State the characteristics of an instrumentation amplifier. [Nov/Dec 2010,April/May 2005, Nov/Dec 2003]

The characteristics of an instrumentation amplifier are:

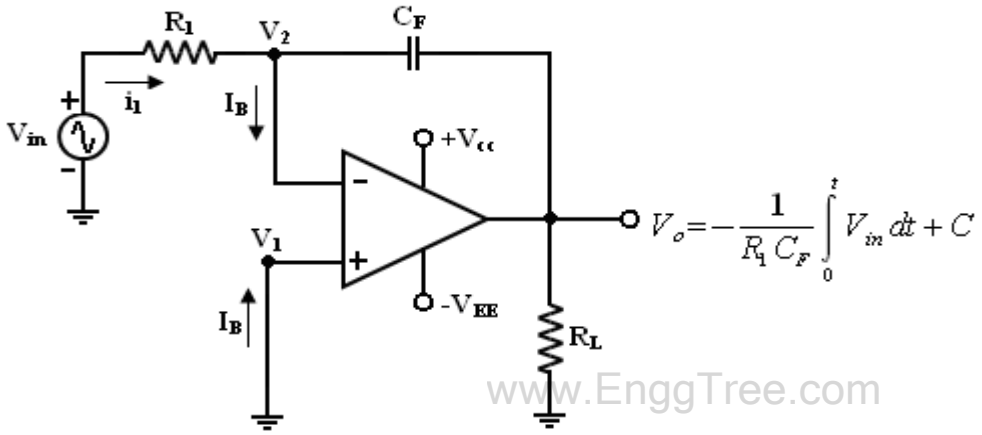
a. High gain accuracy
b. High CMRR
c. High gain stability with low temperature co-efficient
d. Low dc offset
e. Low output impedance
f. High input impedance

23. List the applications of instrumentation amplifier.

The applications of instrumentation amplifier are:

1. Temperature indicator
2. Temperature controller
3. Light intensity meter
4. Water flow meter

24. Draw and write the equation for of an integrator using an op-amp. (Nov/Dec'2006, May/June 2009, Nov/Dec2010), Nov/Dec 2008,April/May 2004)[Nov/Dec 2021]



25. Why integrators are preferred over differentiator in analog computers?(May/June 2009, Nov/Dec 2011)

An analog computer can perform linear operations such as multiplication by constant, addition, subtraction and integration. These operations are sufficient for solving linear differential equations. Linear differential equations can also be solved directly by using differentiator. But the gain of the differentiator increases linearly with frequency and it tends to amplify low frequency noise, which may result in false oscillations. Therefore, integrators are preferred over differentiators in analog computers.

26. Why practical integrators are called Lossy integrators? (Or) What is Lossy integrator?

The gain of an integrator at a low frequency (dc) can be limited to avoid saturation problem if the feedback capacitor is shunted by resistance RF. The parallel combination of RF & CF behaves like practical capacitor, which dissipates power unlike an ideal capacitor. So, this circuit is called Lossy integrator.

27. What are the limitations of the basic differentiator circuit?

. At high frequency, a differentiator may become unstable and break into oscillations

. The input impedance decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

28. What are the limitations of an ideal active differentiator?

At high frequency, differentiators may become unstable and break into oscillation. The input impedance i.e. (1/ωC1) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

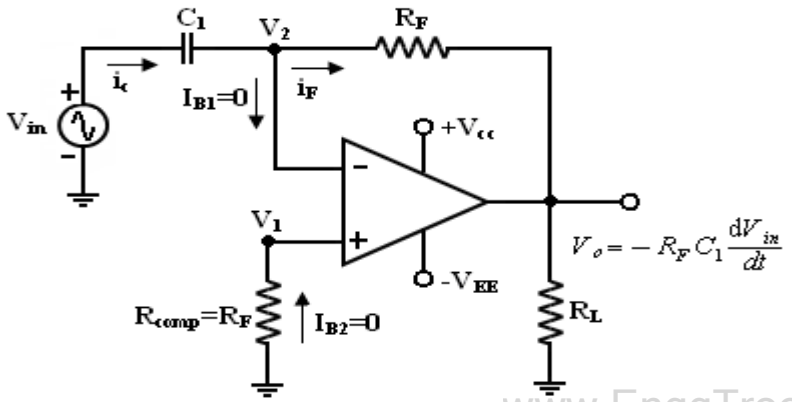
29. Write down the condition for good differentiation.

For good differentiation, the time period of the input signal must be greater than or equal to $R_f C_1$

$T > R_f C_1$ Where, R_f is the feedback resistance, Cf is the input capacitance

30. Draw the circuit diagram of differentiator and give its output equation.

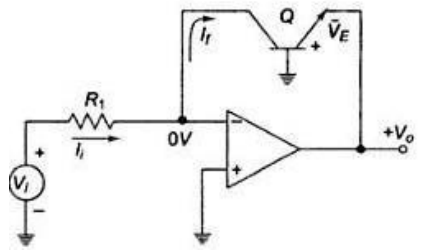
(April/May 2010,Nov/Dec'2012,Nov/Dec 2009)



31. List the applications of Log amplifiers:

- Analog computation may require functions such as ln x, log x, sin hx etc. These functions can be performed by log amplifiers.
- Log amplifier can perform direct dB display on digital voltmeter and spectrum analyzer.
- Log amplifier can be used to compress the dynamic range of a signal.

32. Draw the circuit of a log amplifier. [April/May 2010]



33. What is an antilog amplifier? [Nov/Dec 2007]

A circuit that performs the mathematical operation of antilog is called as antilog amplifier.It performs the reverse operation of log amplifier. Antilog amplifier is a decoding circuit to convert a logarithmically encoded signal back to the real signal.

34. What is a comparator? (May/June 2012, Nov/Dec 2011, Nov/Dec2010)

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is an open loop op - amp with only two possible outputs + Vsat and $-V_{sat}$.

35. List the types of comparators.

The comparator has two types, they are :

- ✓ Inverting comparator
- ✓ Non-inverting comparator

36. What is Trip point?

The point at which transfer characteristics of a comparator is a straight line is called Trip point is the input voltage at which the output changes from low to high or vice versa.

37. What are the applications of comparator? (April/May 2008, Nov/Dec 2011, Nov/Dec 2010)

- ➢ Zero crossing detectors
- ➢ Window detector
- ➢ Time marker generator
- ➢ Phase meter
- ➢ Digital interfacing
- ➢ Schmitt trigger
- ➢ Oscillators

38. What is a window detector?

A device, usually consisting of a pair of voltage comparators, in which output indicates whether the measured signal is within the voltage range bounded by two different thresholds.

39. What are the characteristics of a comparator?

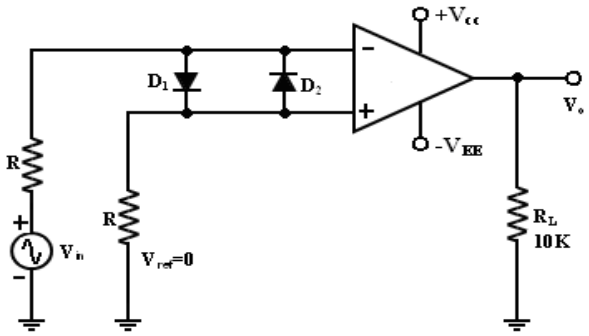
. Speed of operation

. Accuracy

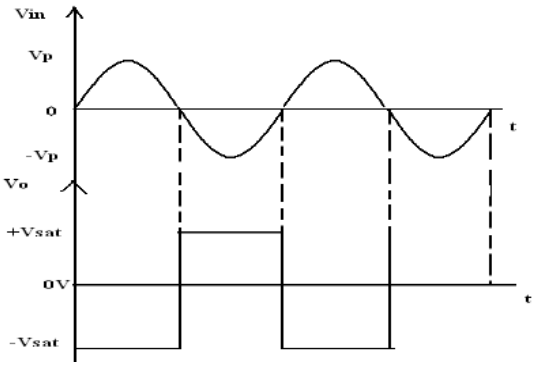
. Compatibility of the output

40. What is zero crossing detectors? [May/June 2009, Nov/Dec2004]

Zero crossing detectors is one of the application of op-amp comparator. The circuit finds the point at which the input voltage crosses zero or dc level.



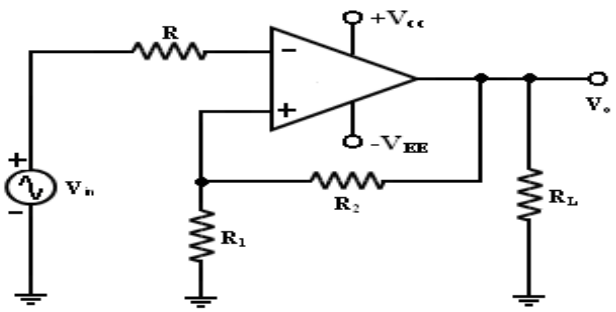
41. Draw the input and output wave form for window detector.



42. What is a Schmitt trigger or regenerative comparator? [April/May 2010] State the principle of a regenerative comparator. [Nov/Dec 2007]

Schmitt trigger is a regenerative comparator. It converts any irregular shaped input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform. The input voltage Vin > Vu_T, output V_0 goes to -Vsat and Vin < V_{LT} , V_0 is at +Vsat and the result is a square wave output.

43. Draw the Schmitt trigger circuit. (May/June 2009)



44. Mention two applications of schmitt trigger. [April/May2005]

Schmitt trigger is mainly used to convert very slowly varying signals into a fastly switching square wave signals and often used as a wave shaping circuit.

45. Differentiate Schmitt trigger and comparator.

A Schmitt trigger is a comparator with a small amount of positive feedback applied to create hysteresis for the input level.

46. What do you mean by a precision diode? [Nov/Dec 2009/April/May 2011]

The major limitation of ordinary diode is that it cannot rectify voltages below the cut – in voltage of the diode. A circuit designed by placing a diode in the feedback loop of an op – amp is called the precision diode and it is capable of rectifying input signals of the order of milli volt.

47. State the difference between conventional and precision rectifier. [April/May 2009,Nov/Dec 2014]

How does precision rectifier differ from conventional rectifier? [Nov/Dec 2012]

S.No.	Conventional rectifier	Precision rectifier
1	Practical diode used	Precision diode used
2	Conducts when $V_i > V_t = 0.7V$ for silicon and 0.3V for Germanium	Diode conducts when $V_i = V_t / A_d$ = 0.7V (Silicon)/10^5 ,V_i =60μ V
3	Cross over distortion occurs	Cross over distortion is completely eliminated.

48. Write down the applications of precision diode.

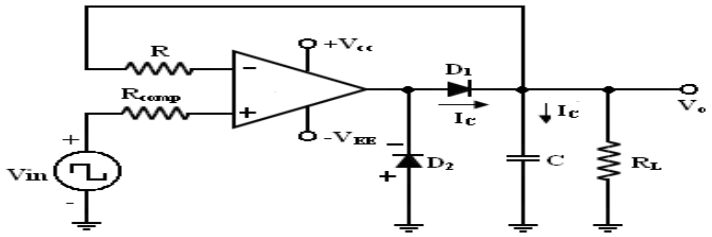
The applications of precision diode are

- Half - wave rectifier
- Full - Wave rectifier
- Peak – value detector
- Clipper
- Clamper

48. What is peak detector?

The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value on a capacitor.

49. Draw the circuit diagram of peak detector. [May/June 2014]



50. What is meant by dc inserter or restorer?

The clamper is also known as dc inserter or resorter.The circuit is used to add a desired dc level to the output voltage. The output is clamped to desired dc level.

51. How does the precision rectifier differ from the conventional rectifier? (April/May 2011, Nov/Dec'2012)

These rectifiers are used to rectify very small voltages or currents for which the diode never gets forward biased in the conventional one. i.e. voltage or currents are always less than .7V which cannot be rectified by normal rectifiers. This rectifier doesn't give any kind of drop in output since diodes are previously biased using op-amp.

52. Give an application for each of the following circuits.[Nov/Dec 2013]

a. **Voltage follower**: It has high input impedance and low output impedance. So it is used to eliminate loading effect. Also used as a buffer.

b. **Peak detector**: Used in amplitude modulation as detector and in test and measurement instrument applications

c. **Schmitt trigger**: Used in wave shaping circuit to convert any input to square wave output and acts as square wave converter.

d. **Clamper:** It is used to add dc signal to the ac output both in positive and negative sides. Often it is used in Television.(TV)

53. What is a filter?

Filter is a frequency selective circuit that passes signal of specified band of frequencies and attenuates the signals of frequencies outside the band.

54. Write the types of filters.

Filters are classified as:

a. Analog or digital
b. Passive or active
c. Audio or radio frequency.

55. Why Butterworth filter is called flat-flat filter?

The main characteristics of Butterworth filter is that, it has flat pass band as well as stop band. So, it is called flat-flat filter.

56. What are the demerits of passive filters? (Nov/Dec'2013,Nov/Dec 2003)

- Passive filters works well for high frequencies.
- At audio frequencies, the inductors become problematic, as they become large, heavy and expensive.

- For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation.

57. What are the advantages of active filters?

- Active filters used op- amp as the active element and resistors and capacitors as passive elements.
- By enclosing a capacitor in the feedback loop, inductor less active filters can be obtained
- Op-amp used in non – inverting configuration offers high input impedance and low output impedance, thus improving the load drive capacity.

58. Mention some commonly used active filters:

Active filters are:

- Low pass filter (LPF)
- High pass filter (HPF)
- Band pass filter (BPF)

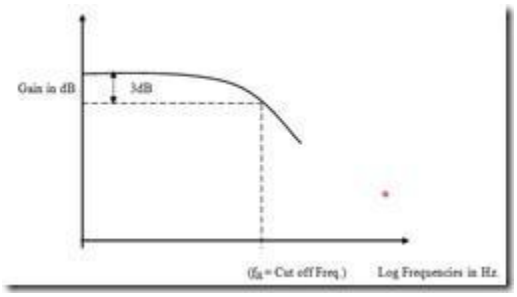
Band reject filter (BRF) or Band stop filter (BSF)

59. What are the advantages of active filters over the passive filters?

Active filters use amplifying elements, especially op amps, with resistors and capacitors in their feedback loops, to synthesize the desired filter characteristics. Active filters can have high input impedance, low output impedance, and virtually any arbitrary gain.

They are also usually easier to design than passive filters. Possibly their most important attribute is that they lack inductors, thereby reducing the problems associated with those components.

60. Draw the freq. response of the LPF.



61. What is frequency scaling?

A filter is designed; there may be a need to change its cut off frequency. The procedure used to convert an original cut off frequency to new cut off frequency is called frequency scaling.

62. Define bandwidth of a filter.[Nov/Dec 2014]

Bandwidth is defined as the difference between higher cut off frequency and lower cut off frequency. It is give as $BW=f_H - f_L$

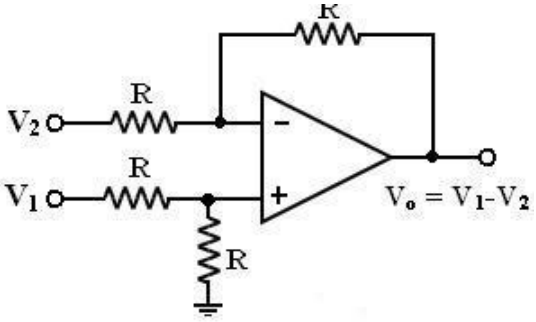
63. What is the function of phase shifter circuits? (May 2018)

- ✓ The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters.
- ✓ That constant delay refers to time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

64. Write the other name for clipper circuit. (May 2018)

Diode clipper is also known as Diode Limiter, is a wave shaping circuit that takes an input waveform and clips its top half, bottom half or both halves together.

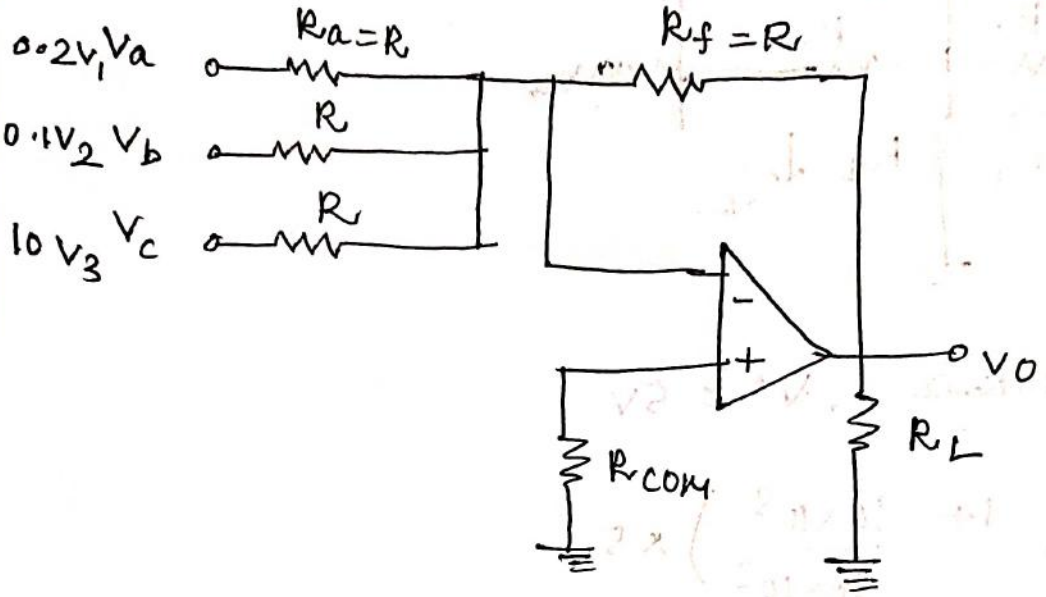
65. Draw the circuit of op amp as a subtractor. [Nov/Dec 2021]



UNIT-2

PART A:

1) Draw the circuit to get the mentioned output using op-amp $V_o = -(0.2V_1 + 0.1V_2 + 10V_3)$ [Nov/Dec 2022]



$$V_o = -\frac{R_f}{R}\{V_a + V_b + V_c\}$$

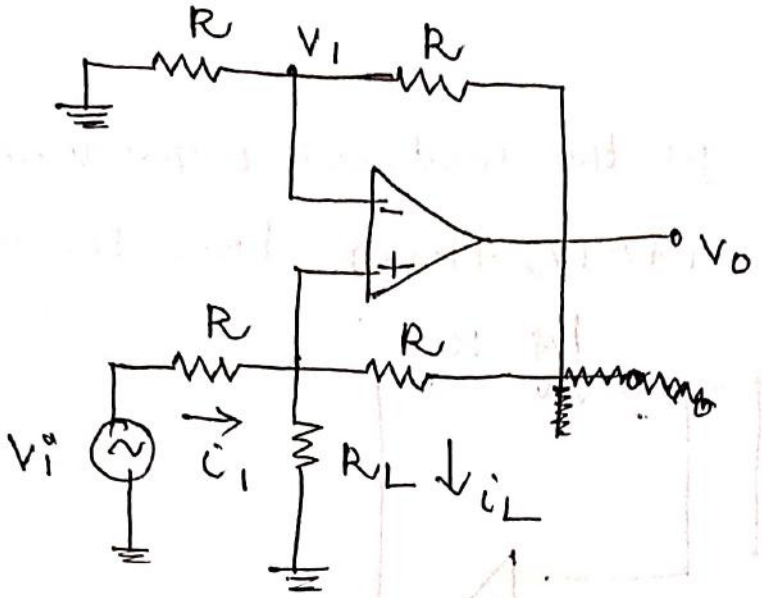
$R_f = R$

$$\therefore V_o = -(V_a + V_b + V_c) = -(0.2V_1 + 0.1V_2 + 10V_3)$$

2. If $V_{in} = 5V$, $R = 10K\Omega$ in a V-I converter. Draw suitable circuit & find gain. I_L of op-amp circuit in non-inverting mode assume potential at non-inverting input is I. What is the output voltage. [Nov/Dec 2022].

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_{in}$$

$V_{in} = 5V$, $R = 10K\Omega$.



$R = 10k\Omega$, $V_i = 5V$.

$$V_o = \left(1 + \frac{10\times10^3}{10\times10^3}\right) \times 5$$

$$= (1+1) \times 5$$

$$\boxed{V_o = 10V}$$

$$\text{Gain} = \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_i}\right) = 1+1 = 2.$$

PART B :-

1) Design a wide band pass filter having $f_L = 400Hz$ $f_H = 2KHz$. & band pass gain of 4. Find the quality factor of the filter. [NOV / DEC 2022]

Given data: $f_L = 400Hz$, $f_H = 2KHz$

Gain = 4

LPF: $C = 0.01\mu F$

$$R_2 = \frac{1}{2\pi f_H C} = \frac{1}{2\pi \times 2\times 10^3 \times 0.01\times 10^{-6}}$$

$$= \frac{1}{4\pi \times 0.01\times 10^{-3}}$$

$$= \frac{1\times 10^3}{0.1256}$$

$$R_2 = 7.96k\Omega$$

HPF $C = 0.01\mu F$

$$R_1 = \frac{1}{2\pi f_L C} = \frac{1}{2\pi \times 400 \times 0.01\times 10^{-6}}$$

$$= \frac{1\times 10^6}{800\times\pi\times 0.01} = \frac{10^6}{25.12}$$

$$R_1 = 39.8k\Omega$$

R_f ∴ $A_F = 4$

$$A_F = A_{F1} \times A_{F2} = 2\times 2$$

$$A_{F1} = 1 + \left(\frac{R_{f1}}{R_{11}}\right) = 2.$$

Quality factor $Q = \frac{f_0}{BW} = \frac{f_0}{f_H - f_L}$

$$f_0 = \sqrt{f_H f_L}$$

$$f_0 = \sqrt{400 \times 2 \times 10^3}$$

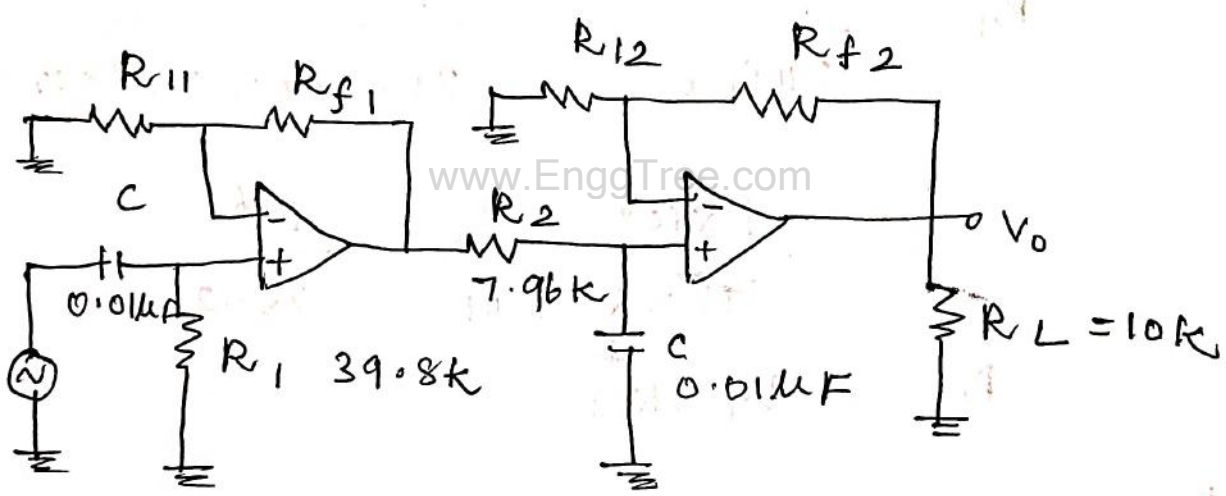
$$= \sqrt{400 \times 2000} = \sqrt{800000}$$

$$= 894.42$$

$$f_H - f_L = 2000 - 400 = 1600$$

$$\therefore Q = \frac{894.42}{1600}$$

$$Q = 0.559, \quad < 10 \rightarrow \text{Wide BPF.}$$



$$\frac{R_{f2}}{R_{12}} = 1$$

$$R_{f2} = R_{12} = R_{f1} = R_{11} = 1K\Omega$$

Unit – III

Analog Multiplier and PLL

Analog Multiplier using Emitter Coupled Transistor Pair - Gilbert Multiplier cell – Variable transconductance technique, analog multiplier ICs and their applications, Operation of the basic PLL, Closed loop analysis, Voltage controlled oscillator, Monolithic PLL IC 565, application of PLL for AM detection, FM detection, FSK modulation and demodulation and Frequency synthesizing.& clock Synchronisation

1. Analog Multiplier:

1.1 Introduction

- A multiplier is a circuit which produces output that is the product of two inputs applied.
- A circuit which performs multiplication of two analog voltages is called as analog multiplier.
- If V_1 and V_2 were the two input analog voltages applied, then the output voltage V_0 is given as

$$V_0 = k\, V_1\, V_2$$

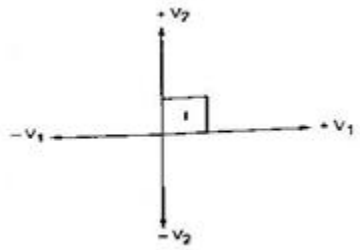
Where, k is the scaling factor.

1.2 Modes of operation of a multiplier

- The modes of operation of multiplier tell about the restriction on polarity of one or both input voltages V1 and V2 applied to multiplier. There were three modes
  - ❖ One quadrant multiplication
  - ❖ Two quadrant multiplication
  - ❖ Four quadrant multiplication

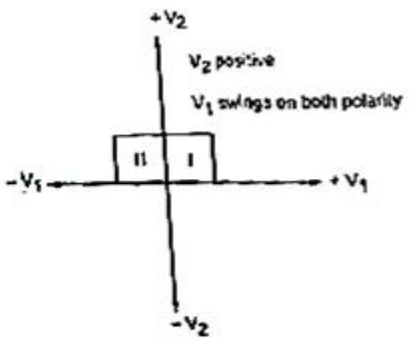
1.3 One quadrant

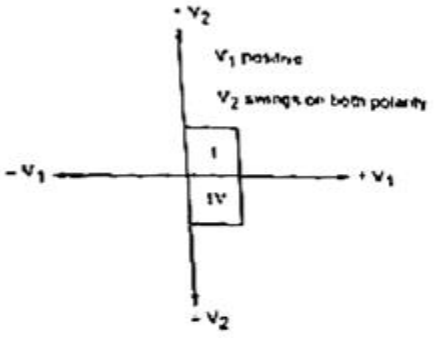
- Both input voltages V_1 and V_2 are restricted to positive polarity.
- That is, V_1 and V_2 must be positive as shown here. It uses first quadrant.



1.4 Two quadrant

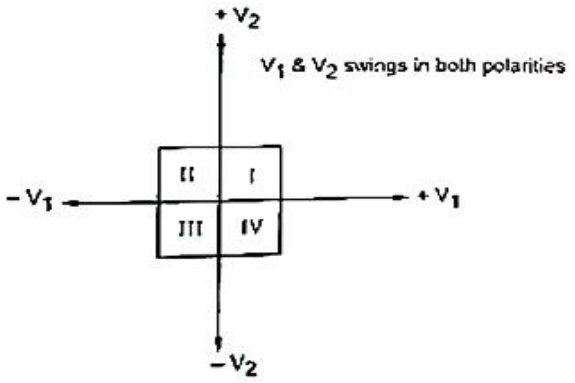
- In this mode, any one input voltage V_1 or V_2 is held positive and the other is allowed to swing in both positive and negative polarity.
- It uses any two or four quadrants (Quadrant I and II or I and IV) as shown here.





1.5 Four quadrant (Gilbert cell)

- In this mode, both the input voltages V_1 and V_2 are allowed to swing in both positive and negative polarity.



- It uses all four quadrants and hence the same.
- The figure here shows the four quadrant multiplication.

1.6 Characteristics or requirements of a multiplier

List and define various performance parameters of multiplier IC. ***[May 2012]***

The following characteristics or requirements are very important for a multiplier to achieve maximum efficiency. They are:

- ❖ Accuracy
- ❖ Linearity
- ❖ Squaring mode accuracy
- ❖ Bandwidth
- ❖ Quadrant

1.6.1 Accuracy

- The deviation of practical output from the ideal output of multiplier for the given input voltages within the operating range of multiplier.
- This characteristic tells how accurate the multiplier is and whether the expected output is obtained or not.

1.6.2 Linearity

- It is the maximum percentage deviation that a practical output compared with a linear straight line output.

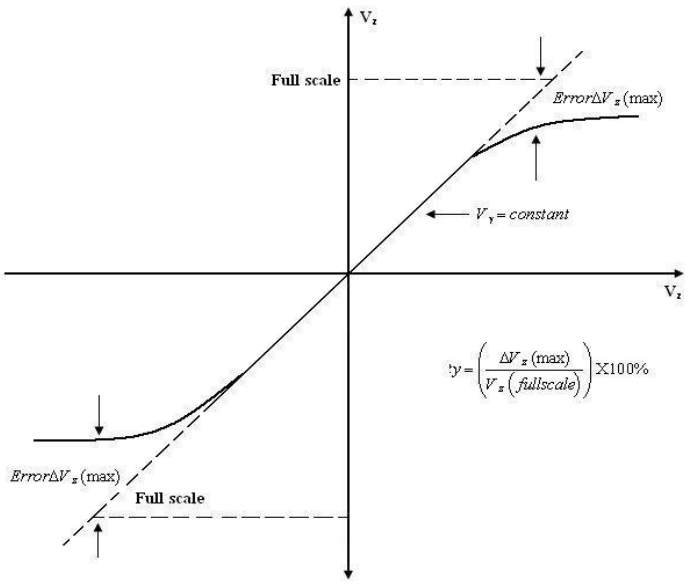
1.6.3 Squaring mode accuracy

- The accuracy of multiplier when both inputs tied together gives square – law curve.
- The deviation of practical squared output versus ideal square-law curve is squaring mode accuracy.

1.6.4 Bandwidth

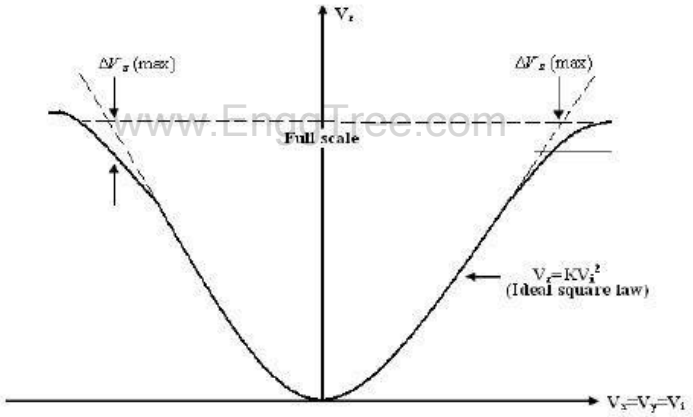
- The operating capability of a multiplier for high frequency analog inputs is indicated with bandwidth.

- Capability with high frequency indicates the improvement in bandwidth.



1.6.5 Quadrant

- It defines the unipolar or bipolar capabilities of input voltages applied.



1.7 Types of analog multipliers

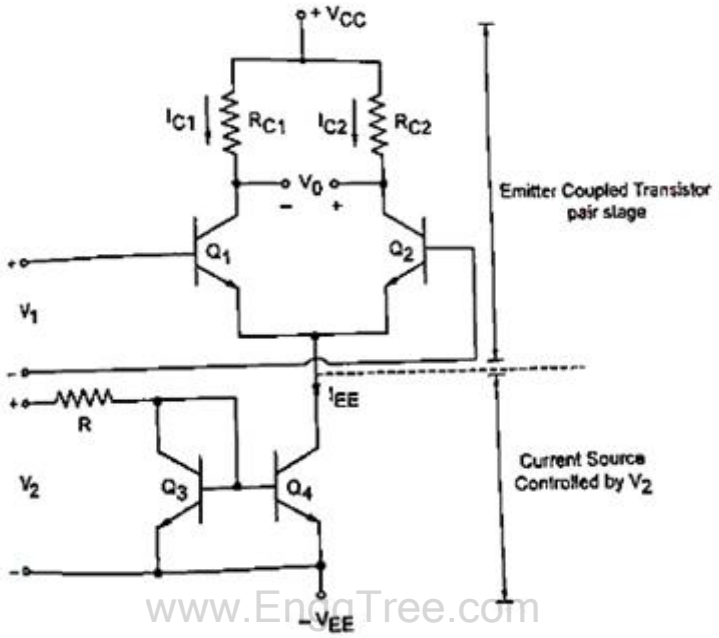
The basic techniques to achieve multiplication are:

- ❖ Logarithmic type
- ❖ Quarter square type
- ❖ Pulse width / height modulation type
- ❖ Current rating type
- ❖ Triangle averaging type
- ❖ Emitter coupled transistor pair type
- ❖ Variable transconductance type
- ❖ Four quadrant type based on variable transconductance (or) Gilbert cell

1.7.1 Analog multiplier using emitter coupled transistor pair

Sketch and explain the multiplier cell using emitter coupled transistor pair. Prove that the output voltage is proportional to the product of input voltage. [Nov 2011] [Dec 2018] [Nov/Dec 2022]

- A pair of transistor with their emitter connected together forms a basic multiplier.
- One input V_1 can be directly applied to the base of transistors Q_1 and Q_2.
- The other input V_2 is applied as the emitter current to both transistors as shown in figure below.



- Taking only the emitter coupled transistor pair stage, the output currents (collector currents) I_{C1} and I_{C2} are related to the differential input voltage V_1 by

$$I_{C1} = \frac{I_{EE}}{1+e^{-V_1/V_T}}$$

Where, V_T is the temperature equivalent voltage.

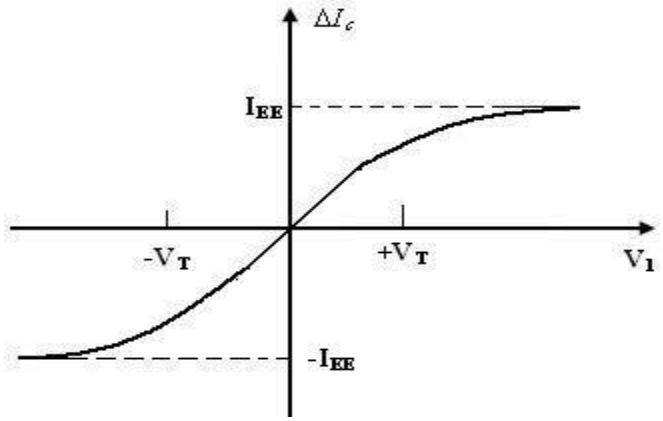
- The polarity in exponential $I_{C2} = \frac{I_{EE}}{1+e^{V_1/V_T}}$ l terms depends on the input voltage V_1.
- The polarity is negative when positive input of V_1 is applied to base of transistor Q_1.
- The polarity is positive when the negative input of V_1 is applied to base of transistor Q_2.
- Taking the difference between two collector currents I_{C1} and I_{C2} as ΔI_C, we can write

$$\Delta I_C = \frac{I_{EE}}{1+e^{-V_1/V_T}} - \frac{I_{EE}}{1+e^{V_1/V_T}}$$

$$\Delta I_C = I_{EE}\left[\frac{1}{1+e^{-V_1/V_T}} - \frac{1}{1+e^{V_1/V_T}}\right]$$

$$\Delta I_C = I_{EE} \tanh\left(\frac{V_1}{2V_T}\right) \qquad \text{---------- (1)}$$

- The dc transfer characteristics of the emitter coupled transistor pair is shown in figure below:



- If $V_1 << V_T$, eqn (1) can be approximated as

$$\Delta I_C = I_{EE} \tanh\left(\frac{V_1}{2V_T}\right) \cong I_{EE}\left(\frac{V_1}{2V_T}\right) \qquad \text{---------- (2)}$$

I_{EE} is the bias current for emitter-coupled pair. If I_{EE} is made proportional to the second input V_2, then eqn (2) becomes

$$\Delta I_C = V_2\left(\frac{V_1}{2V_T}\right) \text{where } V_2 \alpha I_{EE}$$

Thus the collector difference current is proportional to the product of two input voltages V_1 and V_2 multiplied by factor $\left(\frac{1}{2V_T}\right)$. But, considering the base to emitter voltage of transistor, I_{EE} can be written as

$$I_{EE} \cong k_0 (V_2 - V_{BE\,(ON)}) \qquad \text{---------- (3)}$$

Substitute the value of I_{EE} from equation (3) in ΔI_C of equation (2) we get,

$$\Delta I_C = \frac{k_0 V_1 (V_2 - V_{BE(ON)})}{2V_T}$$

Where, k_0 is the scaling factor.

- Two conditions must be satisfied by the input voltages in order to perform multiplication.
- V_1 must be less than 50 mV and V_2 must be greater than $V_{BE\,(ON)}$.

1.7.1.1 Drawbacks:

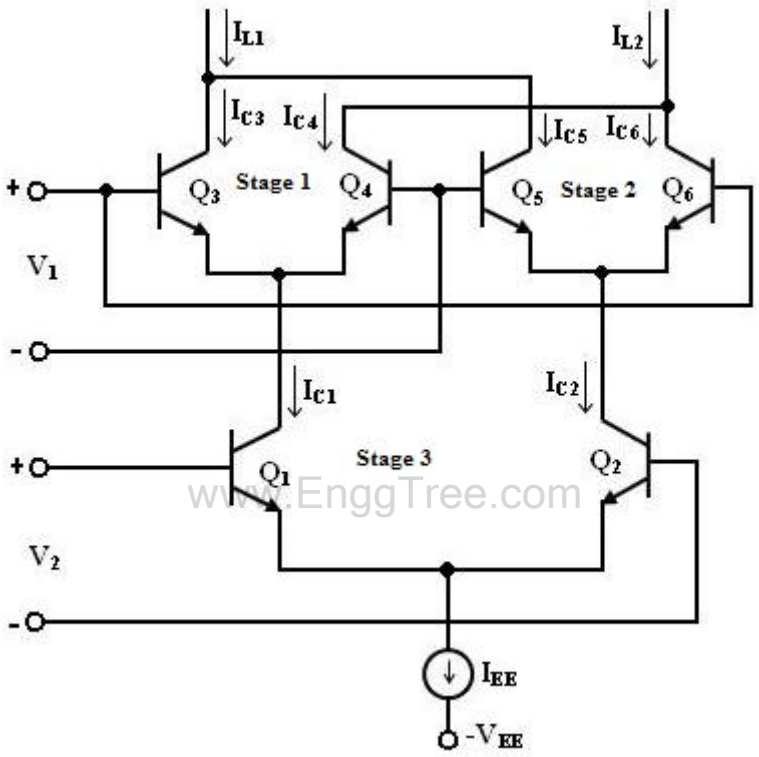
- The input voltage V_2 is offset by $V_{BE\,(ON)}$. So the desired input V_2 cannot be multiplied with other input V_1. Thus the preciseness in getting the product output is affected.
- V_2 must be always positive resulting in two-quadrant multiplication.
- $\tanh\left(\frac{V_1}{2V_T}\right)$ is approximated as $\left(\frac{V_1}{2V_T}\right)$ with the assumption $V_1 << V_T$. In room temperature, V_T = 26 mV. Therefore, V_1 must be very small to satisfy the approximation.

****

1.7.2 Gilbert multiplier cell

Explain the working principles of Gilbert multiplier cell. [April/May 2021] [Nov/Dec 2022]

- The first two drawbacks of emitter coupled transistor pair multiplier can be eliminated by Gilbert multiplier cell.
- Gilbert multiplier cell is also known as four-quadrant multiplier cell.
- It allows the two input voltages to swing in both polarities.
- This method is an extension of emitter coupled transistor pair.
- The circuit of Gilbert cell is shown in figure below.



- The circuit consists of three stages.
- Each stage is having a pair of transistors.
- All the stages are emitter coupled transistor pair with cross coupled stages 1 and 2 in series with stage 3.
- The analysis of the circuit can be done using two methods.
- Analysis 1 uses hyperbolic tangent function.
- Analysis 2 uses the basic principle of transconductance dependence.

1.7.2.1 Analysis 1:

The collector currents of all stages are related with input voltages as follows:

The collector currents of Q_1 and Q_2 are given as,

$$I_{C1} = \frac{I_{C5}}{1+e^{-V_1/V_T}} \quad \text{---------- (1)}$$

$$I_{C2} = \frac{I_{C5}}{1+e^{V_1/V_T}} \quad [\because I_{C5} \text{ is emitter current of pair } Q_1 \text{ and } Q_2] \quad \text{---------- (2)}$$

Similarly, collector currents of Q_3 and Q_4 are given as,

$$I_{C3} = \frac{I_{C6}}{1+e^{V_1/V_T}} \quad \text{---------- (3)}$$

$$I_{C4} = \frac{I_{C6}}{1+e^{-V_1/V_T}} [\because I_{C6} \text{ is emitter current of pair } Q_3 \text{ and } Q_4] \quad \text{---------- (4)}$$

And the collector current of Q_5 and Q_6 can be given as,

$$I_{C5} = \frac{I_{EE}}{1+e^{-V_2/V_T}} \quad \text{---------- (5)}$$

$$I_{C6} = \frac{I_{EE}}{1+e^{V_2/V_T}} [\because I_{EE} \text{ is emitter current of pair } Q_5 \text{ and } Q_6] \quad \text{---------- (6)}$$

Substitute the values of I_{C5} and I_{C6} from equations (5) and (6) in equations (1), (2), (3) & (4), we get

$$I_{C1} = \frac{I_{EE}}{\left[1+e^{-V_1/V_T}\right]\left[1+e^{-V_2/V_T}\right]} \quad \text{---------- (7)}$$

$$I_{C2} = \frac{I_{EE}}{\left[1+e^{V_1/V_T}\right]\left[1+e^{-V_2/V_T}\right]} \quad \text{---------- (8)}$$

$$I_{C3} = \frac{I_{EE}}{\left[1+e^{V_1/V_T}\right]\left[1+e^{V_2/V_T}\right]} \quad \text{---------- (9)}$$

$$I_{C4} = \frac{I_{EE}}{\left[1+e^{-V_1/V_T}\right]\left[1+e^{V_2/V_T}\right]} \quad \text{---------- (10)}$$

The differential output current ΔI is given as,

$$\Delta I = I_{L1} - I_{L2}$$

Where, $I_{L1} = I_{C1} + I_{C3}$ and $I_{L2} = I_{C2} + I_{C4}$ from the figure.

$$\therefore \Delta I = (I_{C1} + I_{C3}) - (I_{C2} + I_{C4})$$

(or)

$$\therefore \Delta I = (I_{C1} - I_{C4}) - (I_{C2} - I_{C3}) \quad \text{---------- (11)}$$

Substitute the equations (7) to (10) in (11) and taking exponential terms as hyperbolic tangent functions, we get

$$\Delta I = I_{EE}\left[\tanh\left(\frac{V_1}{2V_T}\right)\tanh\left(\frac{V_2}{2V_T}\right)\right]$$

Thus the differential current ΔI is the product of the hyperbolic tangent of two inputs voltages V_1 and V_2.

The output voltage V0 can be obtained from ΔI, by using two equal value resistors R connected to V_{CC} and sending current $I_{L1} = (I_{C1} + I_{C3})$ through one resistor and $I_{L2} = (I_{C2} + I_{C4})$ through other resistor.

1.7.2.2 Analysis 2:

The emitter currents of stage 1 and 2 are the collector currents of stage 3 (I_{C5} and I_{C6} in the figure).

The current relationships are,

$$I_{C1} + I_{C2} = I_{C5}$$

$$I_{C3} + I_{C4} = I_{C6}$$

$$I_{C5} + I_{C6} = I_{EE}$$

Assume that $|V_1|$ & $|V_2| << V_T$ and current imbalance is given by,

$$I_{C1} - I_{C2} = (g_m)_{12} V_1 \quad \text{---------- (1)}$$

$$I_{C3} - I_{C4} = (g_m)_{34} V_1 \quad \text{---------- (2)}$$

Where, $(g_m)_{12}$ and $(g_m)_{34}$ are transconductance of pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ respectively. And they are expressed as,

$$(g_m)_{12} = \frac{I_{C5}}{V_T}$$

$$(g_m)_{34} = \frac{I_{C6}}{V_T} \qquad [\text{In general } g_m = \frac{I_E}{V_T} \text{ in transconductance technique}]$$

Here I_{C5} and I_{C6} are nothing but emitter currents of stage 1 and stage 2 respectively.

The differential output voltage V_0 is,

$$V_0 = R_L [(I_{C1} - I_{C2}) - (I_{C3} - I_{C4})] \quad \text{---------- (3)}$$

Substituting the equations (1) & (2) in (3) we get,

$$V_0 = R_L [(g_m)_{12} V_1) - (g_m)_{34}) V_1]$$

$$V_0 = R_L V_1 \left[\frac{I_{C5}}{V_T} - \frac{I_{C6}}{V_T} \right]$$

$$V_0 = \frac{R_L V_1}{V_T} [I_{C5} - I_{C6}] \quad \text{---------- (4)}$$

If R_E is chosen such that

$I_{C5}R_E >> V_T$ & $I_{C6}R_E >> V_T$ then,

$$I_{C5} - I_{C6} = \frac{V_2}{R_E} \quad \text{---------- (5)}$$

Substitute equation (5) in (4)

$$V_0 = \frac{R_L V_1}{V_T} \left[\frac{V_2}{R_E} \right]$$

Rearranging, we get

$$V_0 = (V_1\ V_2)\ \frac{R_L}{V_T R_E}$$

$$V_0 = k\ V_1\ V_2$$

Where, $k = \frac{R_L}{V_T R_E}$ is the scaling factor.

Thus the output voltage V_0 is the product of two input voltages V_1 and V_2 multiplied by scaling factor k.

1.7.2.3 Applications

- Used in most of the IC multipliers as a four quadrant cell.
- Used as modulators or mixers in communication circuits.
- Used in signal processors.
- Used as detectors or demodulators to recover low frequency signals.
- Used as phase detectors.
- Used as frequency doubler, squarer, square rooter, divider, etc.

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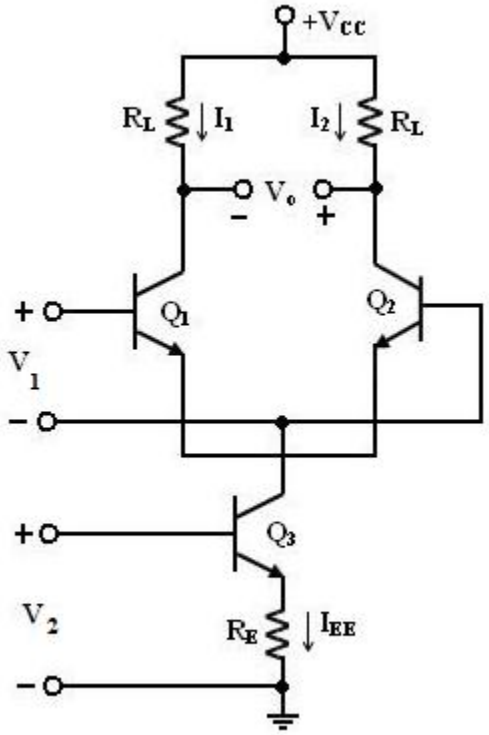
1.7.3 Variable transconductance technique

Explain the working principles of variable transconductance multiplier. (May 2010, 2016, Nov 2012, 2016) [Nov/Dec2021]

- The following figure shows the differential stage used for variable transconductance technique.
- The principle of operation is the dependence of transistor transconductance on the emitter current bias applied.
- The emitter current bias is controlled by the second input voltage V_2.
- Q_1 and Q_2 in the circuit form the differential amplifier.
- For very small differential voltage $V_1 << V_T$, the output voltage is given as,

$$V_0 = g_m R_L V_1 \quad \text{---------- (1)}$$

Where, $g_m = \frac{I_E}{V_T}$ is the transconductance. ---------- (2)



Note that V_0 depends on g_m and g_m depends on I_E. By changing V_2, I_E changes, thereby g_m changes. From the diagram,

$$V_2 = I_E R_E + V_{BE3}$$

If $I_E R_E >> V_{BE3}$

$$V_2 = I_E R_E$$

$$\text{Thus } I_E = \frac{V_2}{R_E}$$

Substituting I_E in (2) and then g_m in (1) we get,

$$V_0 = \frac{V_2}{R_E . V_T} . R_L V_1 \qquad \text{---------- (3)}$$

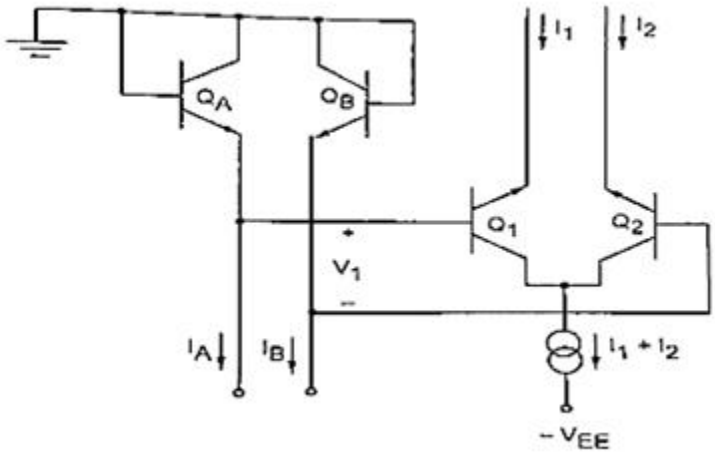
Rearranging (3) we get,

$$V_0 = (V_1 V_2) \frac{R_L}{R_E . V_T} \qquad [\text{Take } k = \frac{R_L}{R_E . V_T}]$$

$$V_0 = k V_1 V_2$$

Where, k is the scaling factor.

To improve linearity of the multiplier, exponential current voltage characteristics can be converted to linear characteristics a shown in the figure below.



The two transistors Q_A and Q_B is a diode connected transistor and are driven by I_A and I_B. I_1 and I_2 are related as,

$$\frac{I_1}{I_2} = e^{(V_1/V_2)} \qquad \text{---------- (4)}$$

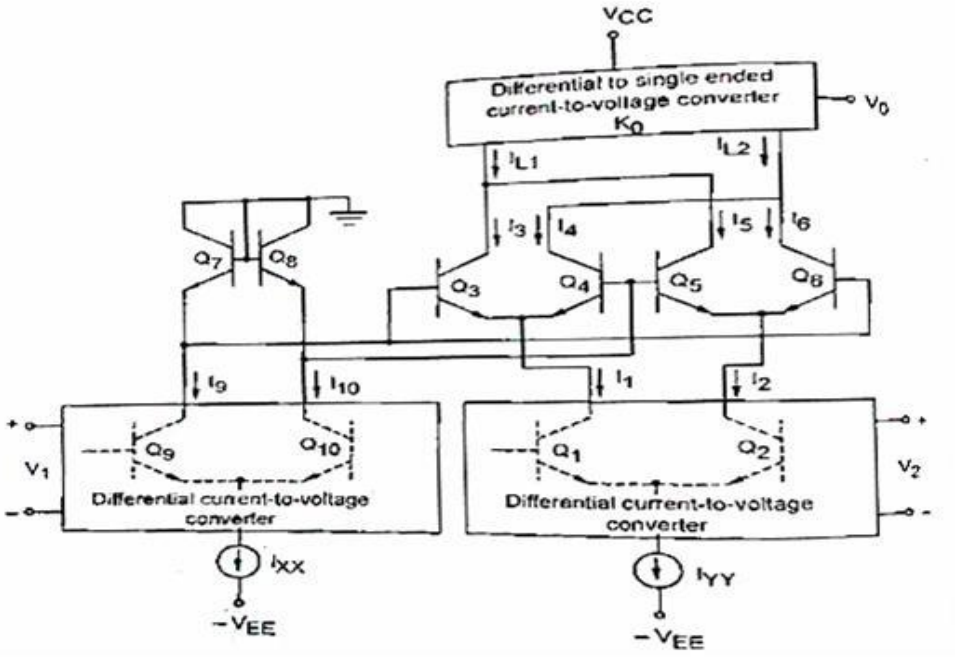
The net bias voltage V1 is logarithmic and given as,

$$V_1 = V_T \ln\left(\frac{I_B}{I_A}\right) \qquad \text{---------- (5)}$$

Substituting V_1 in $\frac{I_1}{I_2}$ we get,

$$\frac{I_1}{I_2} = \frac{I_B}{I_A}$$; Assuming that V_T is very small.

1.7.3.1 A four quadrant multiplier – Complete circuit



- As shown in figure, the complete circuit consists of voltage to current converters or current to voltage converters.
- The currents I_9 and I_{10} through the emitters of Q_7 and Q_8 generate a voltage between two emitter terminals that is proportional to inverse hyperbolic tangent of V_1.
- It uses Gilbert cell for four quadrant multiplication.

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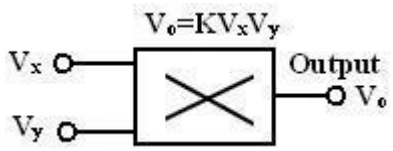
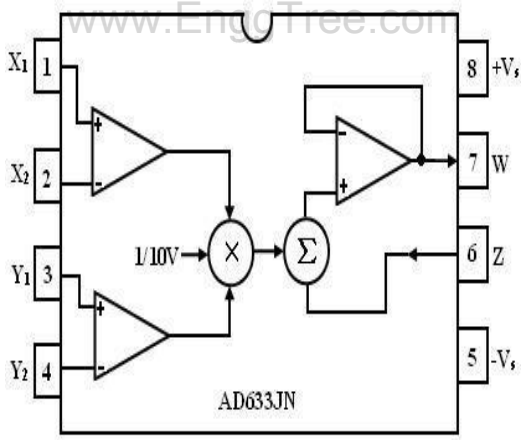
1.8 Analog Multiplier ICs (Discuss briefly about analog multiplier.) [May 2018]

- Analog multiplier is a circuit whose output voltage at any instant is proportional to the product of instantaneous value of two individual input voltages.



- Important applications of these multipliers are multiplication, division, squaring and square – rooting of signals, modulation and demodulation.
- These analog multipliers are available as integrated circuits consisting of op-amps and other circuit elements.
- The Schematic of a typical analog multiplier, namely, AD633 is shown in figure.



- The AD633 multiplier is a four – quadrant analog multiplier.
- It possesses high input impedance; this characteristic makes the loading effect on the signal source negligible.
- It can operate with supply voltages ranging from ±18V.
- The IC does not require external components.
- The typical range of the two input signals is ±10V.

1.8.1 Schematic representation of a multiplier:

- The schematic representation of an analog multiplier is shown in figure.
- The output V_0 is the product of the two inputs V_x and V_y is divided by a reference voltage V_{ref}.

- Normally, the reference voltage V_{ref} is internally set to 10V.
- Therefore, $V_0 = V_x V_y/10$.
- In other words, the basic input – output relationship can be defined by $KV_x V_y$ when K = 1/10, a constant.
- Thus for peak input voltages of 10V, the peak magnitude of output voltage is 1/10 *10 *10 =10V.
- Thus, it can be noted that, as long as $V_x < 10V$ and $V_y < 10V$, the multiplier output will not saturate.

1.8.2 Multiplier quadrants:

The transfer characteristics of a typical four-quadrant multiplier are shown in figure.

Both the inputs can be positive or negative to obtain the corresponding output as shown in the transfer characteristics.

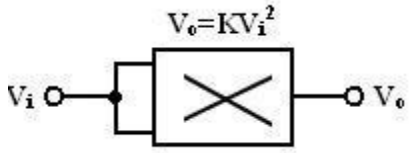
1.8.3 Applications of Multiplier ICs:

Sketch and explain the applications of multiplier. ***[May 2011]***

The multiplier ICs are used for the following purposes:

1. Voltage Squarer
2. Frequency doublers
3. Voltage divider
4. Square rooter
5. Phase angle detector
6. Rectifier

1.8.3.1 Voltage Squarer:



- Figure shows the multiplier IC connected as a squaring circuit.
- The inputs can be positive or negative, represented by any corresponding voltage level between 0 and 10V.
- The input voltage V_i to be squared is simply connected to both the input terminals.
- Hence we have, $V_x = V_y = V_i$ and the output is $V_0 = KV_i^2$.
- The circuit thus performs the squaring operation.
- This application can be extended for frequency doubling applications.

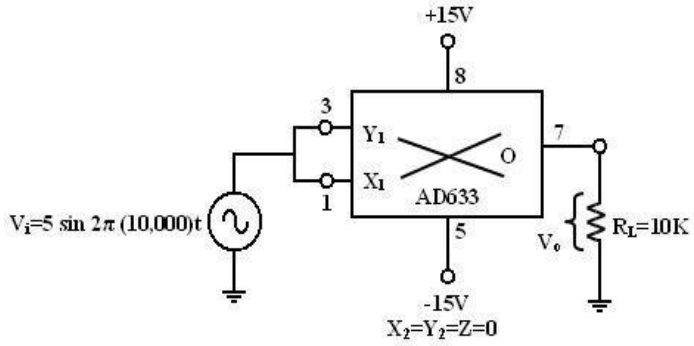
1.8.3.2 Frequency doublers:

How the multiplier IC used as the frequency doubler? ***[May 2012]***

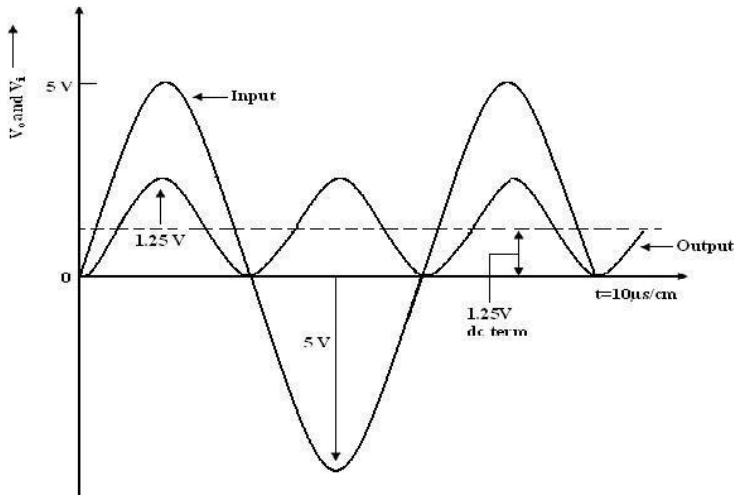
- The figure shows the squaring circuit connected for frequency doubling operation.
- A sine-wave signal V_i has a peak amplitude of A_v and frequency of f Hz.
- Then, the output voltage of the doublers circuit is given by

$$v_0 = \frac{A_v \sin 2\pi ft * A_v \sin 2\pi ft}{10} = \frac{A_v^2}{10} \sin^2 2\pi ft = \frac{A_v^2}{20}(1 - \cos 4\pi ft)$$

- Assuming a peak amplitude A_v of 5V and frequency f of 10 KHz, V_0 =1.25 – 1.25 cos2π (20000) t.
- The first term represents the dc term of 1.25V peak amplitude.
- The input and output waveforms are shown in figure.



- The output waveforms ripple with twice the input frequency in the rectified output of the input signal.
- This forms the principle of application of analog multiplier as rectifier of ac signals.



- The dc component of output V_0 can be removed by connecting a 1μF coupling capacitor between the output terminal and a load resistor, across which the output can be observed.

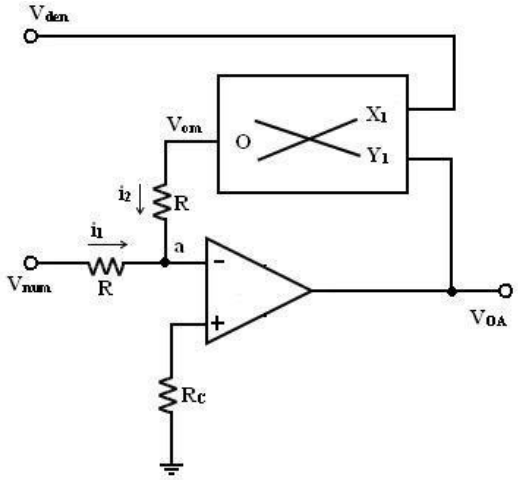
1.8.3.3 Voltage Divider:

How the multiplier IC used as the Voltage divider? ***[May 2012, Nov 2012]***

- Voltage divider can be implemented by connecting a multiplier in the feedback loop of an op-amp as

shown in the figure.

- Vnum is the numerator voltage and Vden is the denominator voltage.
- Note that node 'a' is at virtual ground and other end of Rc is physically grounded.



- From the diagram,

$$i_1 + i_2 = 0$$

substituting $i_1 = V_{num} / R$; $i_2 = V_{om}/R$

$$V_{num} / R + V_{om} / R = 0$$

$$V_{om} = k\, V_{OA}\, V_{den} = - V_{num}$$

Where, V_{om} is the output of multiplier with two inputs V_{OA} and V_{den}

$$V_{OA} = -V_{num} / K.V_{den}$$

K is the scale factor.

- Thus V_{OA} from op-amp is the divided voltage.
- This feature is used in automatic gain control (AGC) circuits.

1.8.3.4 Square Rooter:

- The divider voltage can be used to find the square root of a signal by connecting both inputs of the multiplier to the output of the op-amp.
- Substituting equal in magnitude but opposite in polarity (with respect to ground) to V_i.
- But we know that V_{om} is one - term (Scale factor) of $V_0 * V_0$ or $-V_i = V_{om} = V_2 / 10$.
- Solving for V_0 and eliminating $\sqrt{-1}$ yields.

$$V_0 = \sqrt{10}. |V_i|$$

- The equation states that V_0 equals the square root of 10 times the absolute magnitude of V_i.
- The input voltage Vi must be negative, or else, the op-amp saturates.
- The range of Vi is between -1 and -10V. Voltages less than -1V will cause inaccuracies in the result.
- The diode prevents negative saturation for positive polarity Vi signals.
- For positive values of Vi the diode connections are reversed.

1.8.3.5 Phase Angle detector: Explain the operation of phase detector with relevant sketches.[Nov/Dec 2022]

- The multiplier configured for phase angle detection measurement is shown in figure.
- When two sine - waves of the same frequency are applied to the inputs of the multiplier, the output V_0 has a dc component and an AC component.
- The trigonometric identity shows that Sin A sin B =1/2 (cos (A-B) – cos (A+B)).
- When the two frequencies are equal, but with different phase angles,

  E.g. A = 2πft + θ for signal V_x and B = 2πft for signal V_y,
- Then using the identity

$$[\text{Sin}(2\pi ft + \theta)][\text{Sin}2\pi ft)] = 1/2\,[\cos\theta - \cos(4\pi ft + \theta)]$$

$$= ½ \text{ (dc- ac frequency term).}$$

- Therefore, when the two input signals V_x and V_y are applied to the multiplier, V_0 (dc) is given by

$$v_v(dc) = \frac{v_{xp} v_{yp}}{20}\cos\theta$$

- Where V_{xp} and V_{yp} are the peak voltage amplitudes of the signals V_x and V_y.
- Thus, the output V_0 (dc) depends on the factor cos θ.
- A dc voltmeter can be calibrated as a phase angle meter when the product of V_{xp} and V_{yp} is made equal to 20.
- Then, a (0-1) V range dc voltmeter can directly read cos θ, with the meter calibrated directly in degrees from a cosine table.
- The input and output waveforms are shown in figure.
- Then the above eqn becomes V_0 (dc) = cos θ, if we make the product V_{xp} V_{yp} = 20 or in other words, $V_{xp} – V_{yp}$ = 4.47V.

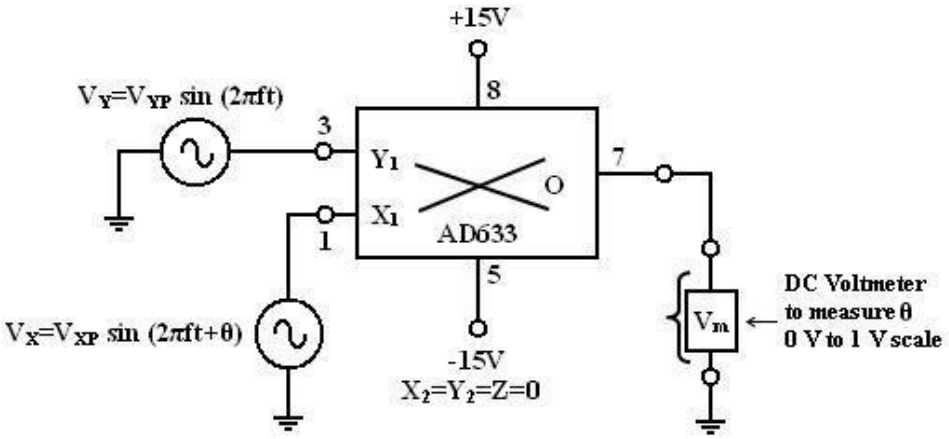


Fig: Phase angle measurement circuit diagram

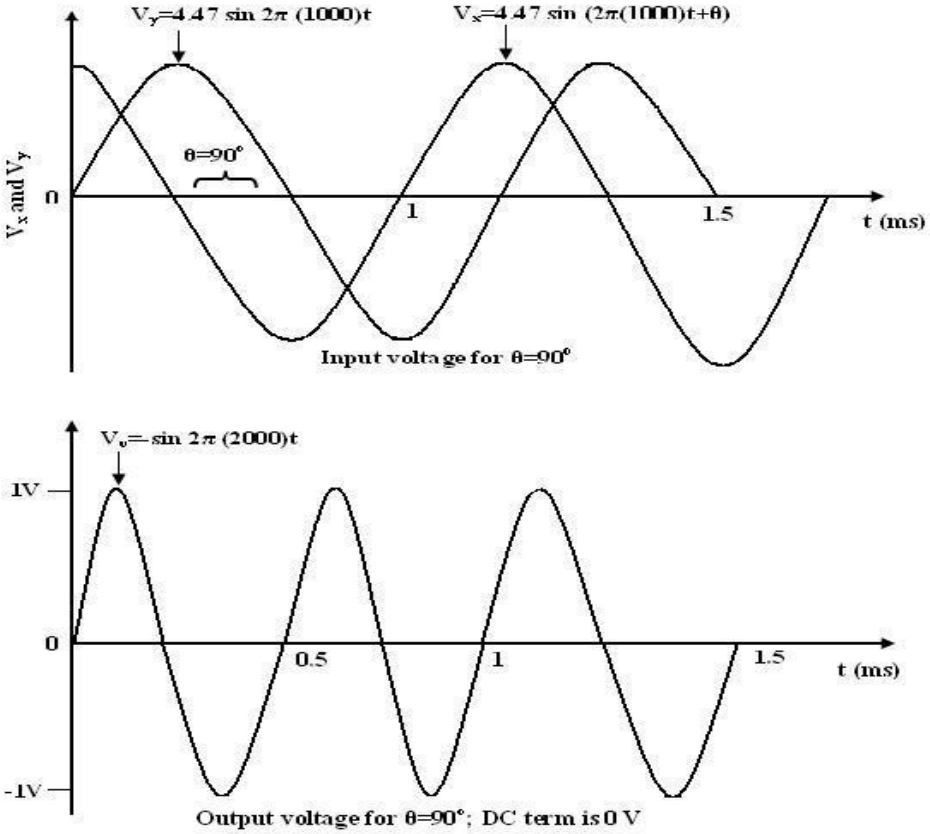


Fig: Input- output waveforms of phase angle detector

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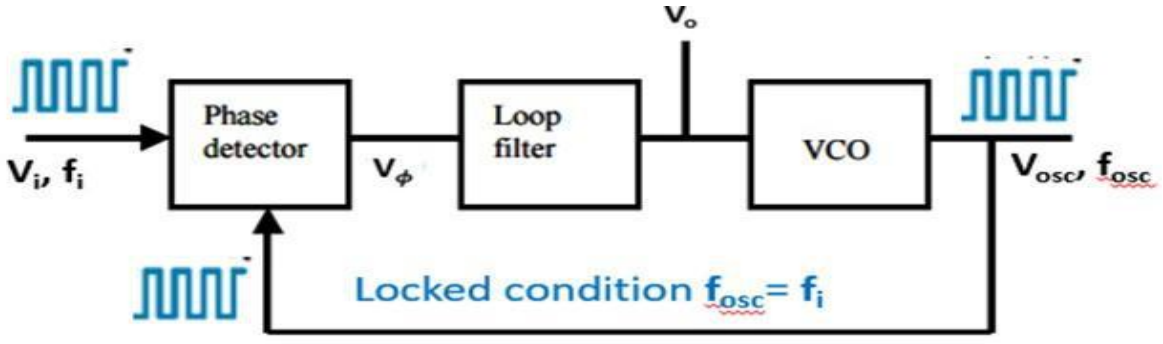
1.9 Operation of Basic Phase Locked Loop [April/May 2021] [Dec 2018]

What are the important building blocks of PLL? Explain its working. [May 2018]***[May 2010 Nov 2010]***

The basic PLL block diagram consists of three components connected in a feedback loop:

- A phase detector (PD) or phase frequency detector (PFD)
- A voltage-controlled oscillator (VCO)
- A loop filter (LF)



- ✓ The phase detector produces a signal V_ϕ proportional to the phase difference between the incoming signal and the VCO output signal.
- ✓ The output of the phase detector is filtered by a low-pass loop filter.
- ✓ The filter output voltage V_0 controls the frequency of the VCO.

- ✓ The voltage at the input of the VCO determines the frequency f_{osc} of the periodic signal V_{osc} at the output of the VCO.
- ✓ A basic property of the PLL is that it attempts to maintain the frequency lock $f_{osc} = f_i$ between V_{osc} and V_i even if the frequency f_i of the incoming signal varies in time.
- ✓ Suppose that the PLL is in the locked condition, and that the frequency f_i of the incoming signal increases slightly.
- ✓ The phase difference between the VCO signal and the incoming signal will begin to increase in time.
- ✓ As a result, the filter output voltage V_0 increases.
- ✓ The VCO output frequency f_{osc} increases until it matches f_{in}, thus keeping the PLL in the locked condition.

1.9.1 Locked Range and Capture Range of the PLL:

- **Locked condition:** $f_{osc} = f_i$
- **Unlocked condition:** $f_{osc} = f_o = const$

****

1.9.2 Lock Range of the PLL:

With Usual notations, show that the 'lock-in-range' of PLL is $\Delta f_L = \pm 7.8 f_o / V$. ***[Nov/Dec 2011]***

- The range of frequencies from $\mathbf{f_i = f_{min}}$ to $\mathbf{f_i = f_{max}}$ where the locked PLL remains in the locked condition.
- The lock range is wider than the capture range.
- If the PLL is initially locked, and if $\mathbf{f_i < f_{min}}$, or $\mathbf{f_i > f_{max}}$.
- The PLL becomes unlocked at $\mathbf{f_i \neq f_{osc}}$.
- When the PLL is unlocked, the VCO oscillates at the frequency $\mathbf{f_o}$ called the center frequency, or the free- running frequency of the VCO.
- If φ radians are the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by,

$$v_e = (\varphi - \pi/2) \quad \text{---------- (1)}$$

$Where, K_\varphi$ is the phase angle-to-voltage transfer coefficient of the phase detector.

- The control voltage to VCO is,

$$v_c = (\varphi - \pi/2) \quad \text{---------- (2)}$$

Where, A is the voltage gain of the amplifier.

- This $v_c$shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$$f = f_0 + K_v v_c \quad \text{---------- (3)}$$

Where, K_v is the voltage to frequency transfer coefficient of the VCO.

- When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_0 + K_v v_c \quad \text{---------- (4)}$$

- Since, $v_c = (f_s - f_0) / K_v = AK_\varphi(\varphi - \pi/2)$ ---------- (5)
- Thus, $\varphi = \pi/2 + (f_s - f_0)/K_V K_\varphi A$ ---------- (6)
- The maximum output voltage magnitude available from the phase detector occurs for φ = π and 0 radian and v_e(max) = $\pm K_\varphi . \pi/2$The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(\max)} = \pm\left(\frac{\pi}{2}\right).K_\varphi.A \quad \text{---------- (7)}$$

- The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_0)_{max} = K_v V_{c(\max)} = K_V K_\varphi A\left(\frac{\pi}{2}\right) \quad \text{---------- (8)}$$

- Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_0 \pm (f - f_0)_{max}$$

$$= f_0 \pm K_V K_\varphi A\left(\frac{\pi}{2}\right) = f_0 \pm \Delta f_L \quad \text{---------- (9)}$$

Where 2 Δf_L will be lock-in frequency range and is given by,

Lock-in range = $2\,\Delta f_L = K_V K_\varphi A\pi$ ---------- (10)

$$\Delta f_L = \pm K_V K_\varphi A\left(\frac{\pi}{2}\right) \quad \text{---------- (11)}$$

- The lock in range is symmetrically located with respect to VCO free running frequency f_0. For IC PLL 565,

$$K_V = \frac{8f_0}{V}$$

Where, $V = +V_{cc} - (-V_{cc})$

Again, $K_\varphi = \frac{1.4}{\pi}$

And $A = 1.4$

- Hence the lock-in range from eqn (11) becomes,

$$\boxed{\Delta f_L = \pm 7.8\, f_0 / V} \quad \text{---------- (12)}$$

****

1.9.3 Capture Range of the PLL:

Derive the expression for the capture range of PLL.

- When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\varphi = (\omega_s t + \theta_s) - (\omega_0 t + \theta_0) = (\omega_s - \omega_0)t + \Delta\theta \quad \text{---------- (13)}$$

- Thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\varphi}{dt} = \omega_s - \omega_0 \quad \text{---------- (14)}$$

- The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\varphi\left(\frac{\pi}{2}\right)$ and a fundamental frequency$(f - f_0) = \Delta f$.
- The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) \approx \frac{1}{1+j\left(\frac{f}{f_1}\right)} \quad \text{---------- (15)}$$

Where, f1 = ½ π RC is the 3 dB point of LPF. In the slope portion of LPF where $(f/f1)^2 >> 1$, then

$$T(f) = \frac{f_1}{jf} \quad \text{---------- (16)}$$

- The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_0$. If$\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \approx f_1/\Delta f = f_1/(f_s - f_0) \quad \text{---------- (17)}$$

- The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \quad \text{---------- (18)}$$

Or, $v_{c(max)} = v_{e(max)} \times T(f) \times A$

$$= \pm K_\varphi\left(\frac{\pi}{2}\right) A(f_1/\Delta f) \quad \text{[From eqn.7] ---------- (19)}$$

- Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_0)_{max} = K_V v_{c(max)} = \pm K_\varphi\left(\frac{\pi}{2}\right) A(f_1/\Delta f) \quad \text{---------- (20)}$$

- For the acquisition of signal frequency, we should put f = f_s so that the maximum signal frequency range that can be acquired by PLL is,

$$(f - f_0)_{max} = \pm K_V\, K_\varphi\left(\frac{\pi}{2}\right) A(f_1/\Delta f_c) \quad \text{---------- (21)}$$

- Now, $\Delta f_c = (f - f_0)_{max}$
- So,

$$(\Delta f_c)^2 = \pm K_V\, K_\varphi\left(\frac{\pi}{2}\right) A f_1 \text{[from eqn.21]}$$

- Since, $\Delta f_L = \pm K_V\, K_\varphi\left(\frac{\pi}{2}\right) A$

We get, $(\Delta f_c) = \pm\sqrt{f_1 \Delta f_L}$ ---------- (22)

- Therefore, the total capture range is,

$$2\Delta f_c \approx 2\sqrt{f_1 \Delta f_L}$$

- Where the lock-in range $=2\Delta f_c = K_V K_\varphi A\pi$.
- In case of IC PLL 565, R = 3.6 KΩ, so the capture range is

$$\pm\left[\frac{\Delta f_L}{2\pi(3.6\times10^3)}\right]^{\frac{1}{2}} \qquad \text{---------- (23)}$$

Where, C is in farads.

- The capture range is symmetrically located with respect to VCO free running frequency f_0 as shown in the figure below.

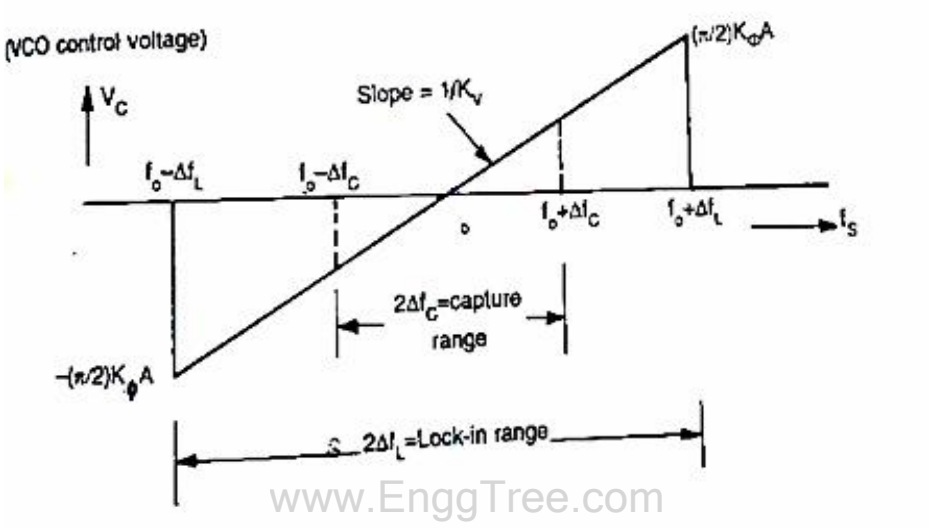


Figure: PLL lock in range and capture range

- The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range.
- In order to increase the ability of lock-in range large capture range is required.
- However, a large capture range will make the PLL more susceptible to noise and undesirable signal.
- Hence a suitable compromise is often reached between these two opposing requirements of the capture range.
- Many a times the LPF bandwidth is first set for a large value for initial acquisition of signal.
- Once the signal is captured, the bandwidth of LPF is reduced substantially.
- This will minimize the interference of undesirable signals and noise.

1.9.4 Phase Detector

- Phase detector compares the input frequency and VCO frequency and generates DC voltage.
- That is proportional to the phase difference between the two frequencies.
- Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively.

- Even though most monolithic PLL integrated circuits use analog phase detectors.

E.g for Analog: Double-balanced mixer

E.g for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

1.9.5 Ex-OR Phase Detector:

- This uses an exclusive OR gate.
- The output of the Ex-OR gate is high only when f_{IN} or f_{OUT} is high.
- The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs.
- The maximum dc output voltage occurs when the phase difference is Π radians or 180 degrees.
- The slope of the curve between 0 or Π radians is the conversion gain k_p of the phase detector.
- For eg; if the Ex-OR gate uses a supply voltage Vcc = 5V, the conversion gain Kp is

$$k_{p=\frac{5}{\pi}=1.59rad}$$

1.9.6 Advantages of Edge Triggered Phase Detector over Ex-OR:

- The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.
- Better Capture, tracking & locking characteristics.
- Edge triggered type of phase detector using RS Flip – Flop is formed from a pair of cross coupled NOR gates.
- RS FF is triggered, i.e., the output of the detector changes its logic state on the positive edge of the inputs f_{IN} & f_{OUT}.

1.9.7 Monolithic Phase detector:

- It consists of 2 digital phase detector, a charge pump and an amplifier.
- Phase detector 1 is used in applications that require zero frequency and phase difference at lock.
- In Phase detector 2, quadrature lock is desired.
- When detector 1 is used in the main loop, detector can also be used to indicate whether the main loop is in lock or out of lock.

1.9.8 Low – Pass filter

- The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise.
- LPF controls the characteristics of the phase locked loop. i.e., capture range, lock ranges, bandwidth.

1.9.9 Lock range (Tracking range):

- The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency f_{IN}.

1.9.10 Capture range:

- Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

1.9.11 Filter Bandwidth:

- If filter b andwidth is reduced, its response time increases.
- However reduced Bandwidth reduces the capture range of the PLL.
- Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

1.9.12 Voltage Controlled Oscillator (VCO):

- The third section of PLL is the VCO.
- It generates an output frequency that is directly proportional to its input voltage.
- The maximum output frequency of NE/SE 566 is 500 KHz.

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1.10 Closed Loop Analysis of PLL

Explain the closed loop analysis of PLL.

- Phase locked loops can also be analyzed as control systems by applying the Laplace transform.
- The loop response can be written as:

$$\frac{\theta_o}{\theta_i} = \frac{K_p K_v F(s)}{s + K_p K_v F(s)}$$

Where

θo is the output phase in radians

θi is the input phase in radians

Kp is the phase detector gain in volts per radian

Kv is the VCO gain in radians per volt-second

$F(s)$ is the loop filter transfer function (dimensionless)

- The loop characteristics can be controlled by inserting different types of loop filters.
- The simplest filter is a one-pole RC circuit.
- The loop transfer function in this case is:

$$F(s) = \frac{1}{1 + sRC}$$

- The loop response becomes:

$$\frac{\theta_o}{\theta_i} = \frac{\frac{K_p K_v}{RC}}{s^2 + \frac{s}{RC} + \frac{K_p K_v}{RC}}$$

- This is the form of a classic harmonic oscillator.

- The denominator can be related to that of a second order system:

$$s^2 + 2s\zeta\omega_n + \omega_n^2$$

Where,

ζ is the damping factor

ω_n is the natural frequency of the loop.

- For the one-pole RC filter,

$$\omega_n = \sqrt{\frac{K_p K_v}{RC}} \quad \zeta = \frac{1}{2\sqrt{K_p K_v RC}}$$

- The loop natural frequency is a measure of the response time of the loop.
- The damping factor is a measure of the overshoot and ringing.
- Ideally, the natural frequency should be high and the damping factor should be near 0.707 (critical damping).
- With a single pole filter, it is not possible to control the loop frequency and damping factor independently.
- For the case of critical damping,

$$RC = \frac{1}{2K_p K_v}$$

$$\omega_c = K_p K_v \sqrt{2}$$

- A slightly more effective filter, the lag-lead filter includes one pole and one zero.
- This can be realized with two resistors and one capacitor.
- The transfer function for this filter is

$$F(s) = \frac{1 + sCR_2}{1 + sC(R_1 + R_2)}$$

- This filter has two time constants $\tau_1 = C(R_1 + R_2)$ τ_2

$$= CR_2$$

- Substituting above yields the following natural frequency and damping factor

$$\omega_n = \sqrt{\frac{K_p K_v}{\tau_1}}$$

$$\zeta = \frac{1}{2\omega_n \tau_1} + \frac{\omega_n \tau_2}{2}$$

- The loop filter components can be calculated independently for a given natural frequency and damping factor

$$\tau_1 = \frac{K_p K_v}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n} - \frac{1}{K_p K_v}$$

- Real world loop filter design can be much more complex.

  E.g: Using higher order filters to reduce various types or source of phase noise.

1.10.1 Applications of PLL:

The PLL principle has been used in applications such as

- ✓ FM stereo decoders
- ✓ Motor speed control
- ✓ Tracking filters
- ✓ FM modulation and demodulation
- ✓ FSK modulation
- ✓ Frequency multiplier
- ✓ Frequency synthesis etc.,

1.10.2 Example of PLL ICs: 560 series (560, 561, 562, 564, 565 & 567).

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1.11 Voltage Controlled Oscillator:

Briefly explain the working of voltage controlled oscillator. [May 2018] ***[May 2010, 2011, Nov 2010, 2011]***

1.11.1 Introduction

- A VCO is inbuilt in a PLL.
- The IC VCO is 566 IC.
- The frequency of oscillation is determined by external resistor and capacitor.
- It contains a current source, buffer, Schmitt trigger and an inverter.

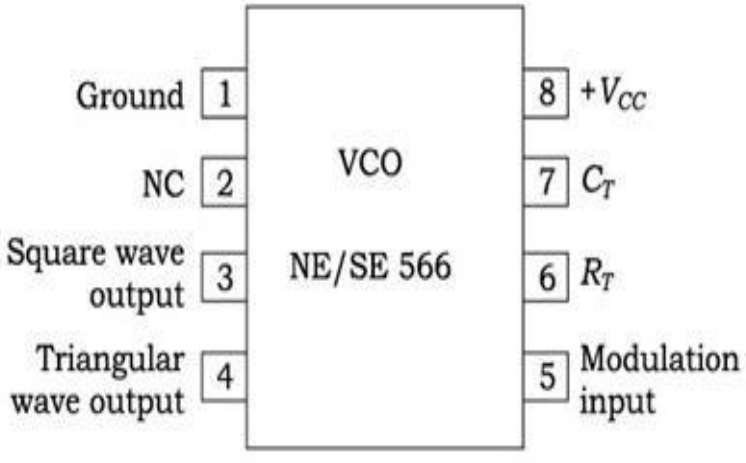


Fig: Pin diagram of VCO

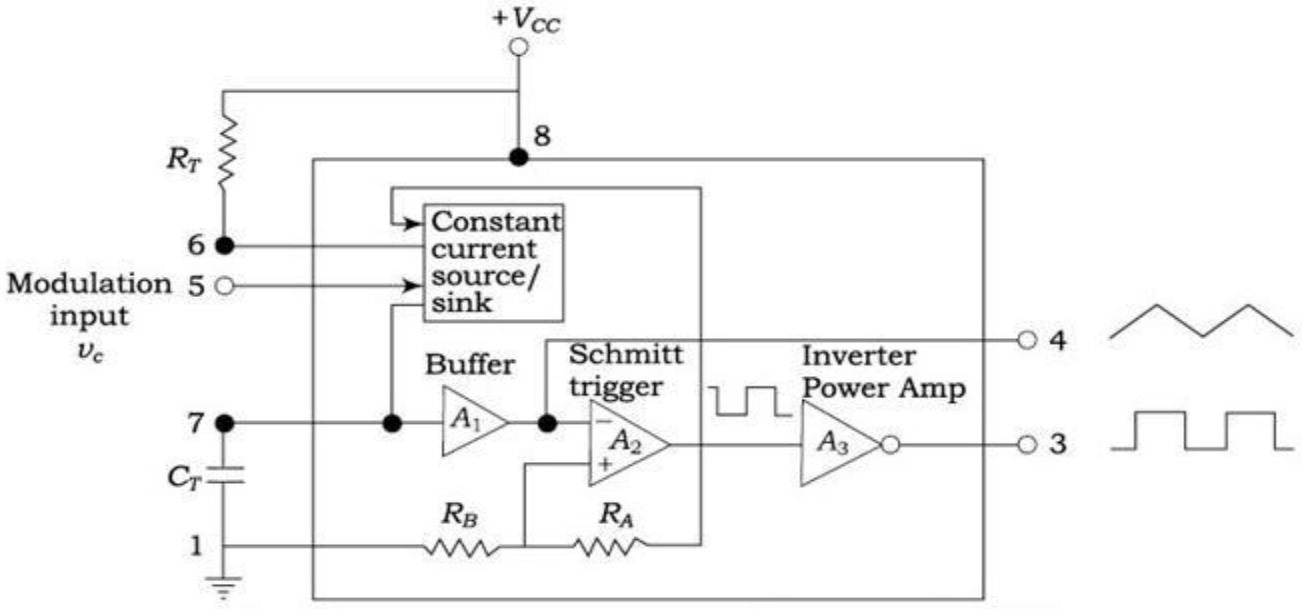


Fig: Block diagram of VCO

1.11.2 Operation of a VCO

- The modulating input V_C is applied to constant source which generates current.
- The capacitor C_1 charges and discharges due to the reference set at the non-inverting terminal of op-amp A_2 from 0.5 V_{CC} to 0.25 V_{CC} by resistor potential divider R_a & R_b.
- If the output of buffer tries to exceed 0.5 V_{CC} the Schmitt trigger goes low and the capacitor discharges until 0.25 V_{CC}.
- Again Schmitt trigger goes high state and this process repeats.
- The output of buffer is a triangle voltage and the output of inverter is a square wave.
- The output of Schmitt trigger is fed to constant current source to get a controlled current output to charge and discharge C_1.

1.11.3 Calculation of free – running frequency [Dec 2018]

- The voltage change across the capacitor C_1 is $\Delta v = 0.255\ V_{CC}\ C_1$.
- The rate of change of voltage across the capacitor is given as

$$\frac{\Delta v}{\Delta t} = \frac{i}{C_1} = \frac{0.25V_{CC}}{\Delta t}$$

$$\Delta t = \frac{0.25V_{CC}C_1}{i}$$

- The time period 'T' of the triangular waveform is $2\Delta t$.
- The frequency of oscillation f_0 is,

$$f_0 = \frac{1}{T}$$

$$= \frac{1}{2\Delta t}$$

$$= \frac{1}{2\left(\frac{0.25V_{CC}C_1}{i}\right)}$$

$$= \frac{i}{0.5V_{CC}C_1}$$

Where, $f_0 = \frac{2(V_{CC} - V_C)}{R_1C_1V_{CC}}$ $\quad \because i = \frac{V_{CC} - V_C}{R_1}$

- The output frequency thus depends on V_C, R_1 & C_1.

1.11.4 Voltage to Frequency conversion factor

- V to F conversion factor is given as $k_v = \frac{\Delta f_0}{\Delta V_C}$

  Where, ΔV_C →Change in control voltage

  Δf_0 →Change in frequency due to change in V_C (ΔV_C).

- Assuming that the free-running frequency of VCO is f_0 and the new frequency is f_1. We get,

  $$\Delta f = f_1 - f_0$$

- From the previous analysis,

$$\Delta f = \frac{2(V_{CC} - V_C + \Delta V_C)}{R_1C_1V_{CC}} - \frac{2(V_{CC} - V_C)}{C_1R_1V_{CC}}$$

$$\Delta f = \frac{2\Delta V_C}{R_1C_1V_{CC}}$$

$$\text{Now } k_v = \frac{\Delta f}{\Delta V_C} = \frac{2\Delta V_C}{R_1C_1V_{CC}\Delta V_C} = \frac{2}{R_1C_1V_{CC}}$$

- From previous analysis,

$$f_0 = \frac{2(V_{CC} - V_C)}{R_1C_1V_{CC}} \text{ \& if } V_C = \frac{7}{8}V_{CC}$$

$$f_0 = \frac{1}{4R_1C_1}$$

K_v can be written in terms of f0 as

$$K_v = \frac{8f_0}{V_{CC}}$$

1.11.5 Low pass filter

- The function of LPF in PLL is to remove high frequency harmonics or components generated in the output of phase detector.

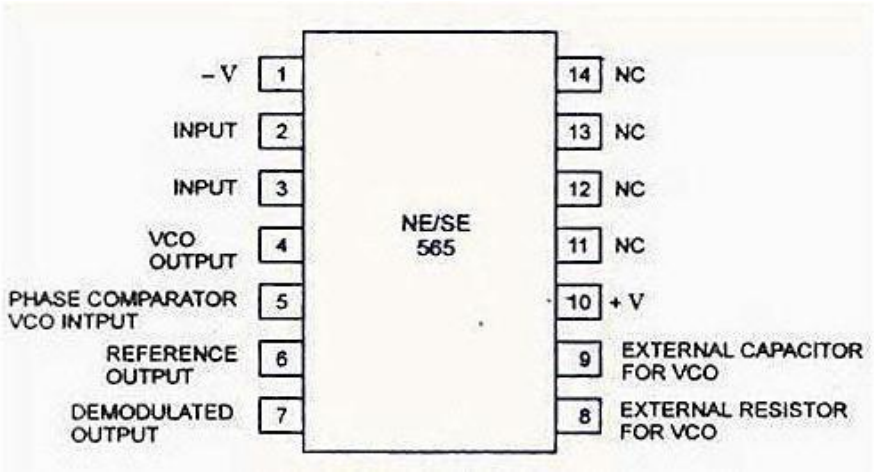
- The bandwidth of the filter determines the response time and the capture range.

****

1.12 Monolithic Phase Locked Loops (PLL IC 565):

Discuss the principles of operations of NE565 PLL circuit. [May 2018] ***[May 2016, Nov 2016]***

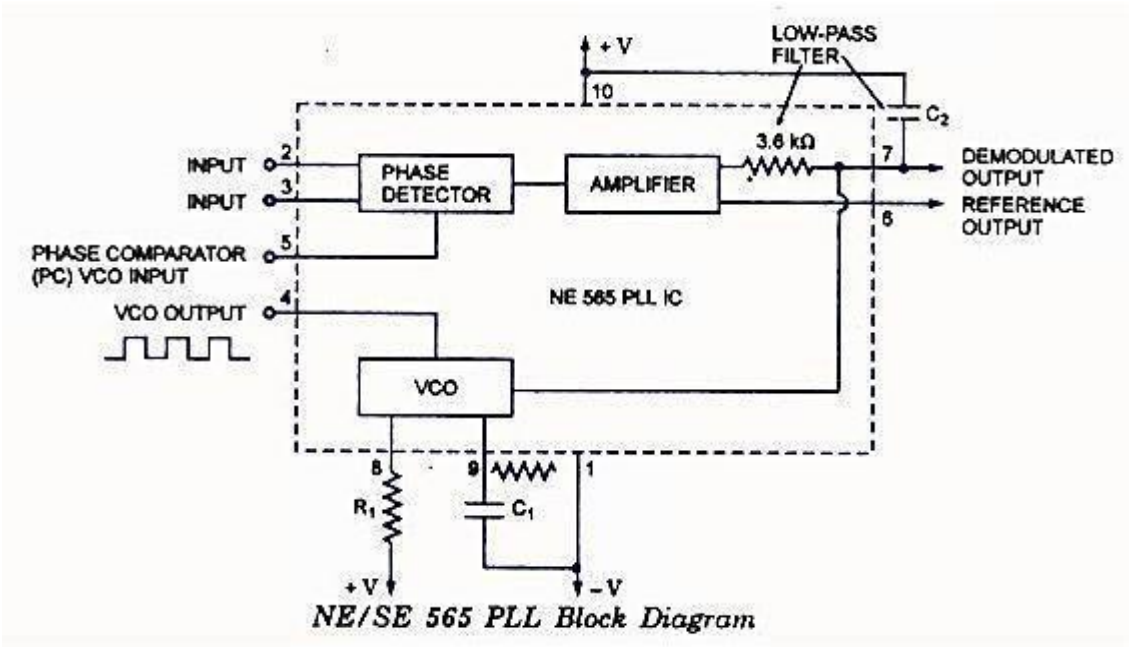
1.12.1 Pin Configuration of PLL IC 565



1.12.2 Basic Block Diagram Representation of IC 565

The important electrical characteristics of the 565 PLL are,

- ***Operating frequency range:*** 0.001Hz to 500 KHz.
- ***Operating voltage range:*** ±6 to ±12v
- ***Input level required for tracking:*** 10mv rms min to 3 V_{pp} max
- ***Input impedance:*** 10 K ohms typically.
- ***Output sink current:*** 1mA
- ***Output source current:*** 10 mA



NE/SE 565 PLL Block Diagram

- The center frequency of the PLL is determined by the free running frequency of the VCO, which is given by $f_{OUT} = 1.2 / 4R_1C_1$, where R_1 & C_1 are an external resistor & a capacitor connected to pins 8 & 9.
- The VCO free-running frequency f_{OUT} is adjusted externally with R_1 & C_1 to be at the center of the input frequency range.
- C_1 can be any value; R_1 must have a value between 2 k ohms and 20 K ohms.
- Capacitor C_2 connected between 7 & +V.
- The filter capacitor C_2 should be large enough to eliminate variations in the demodulated output voltage in order to stabilize the VCO frequency.
- The lock range f_L & capture range f_c of PLL is given by,

$$\Delta fL = \pm 7.8 \ fout / V \quad Hz$$

Where f_{OUT} = free running frequency of VCO (Hz)

V = (+Vcc) - (-Vcc) volts

$$\Delta f_C = \pm [\ \Delta fL/(2\Pi)(3.6)(10^3)C2\ ]^{½}$$

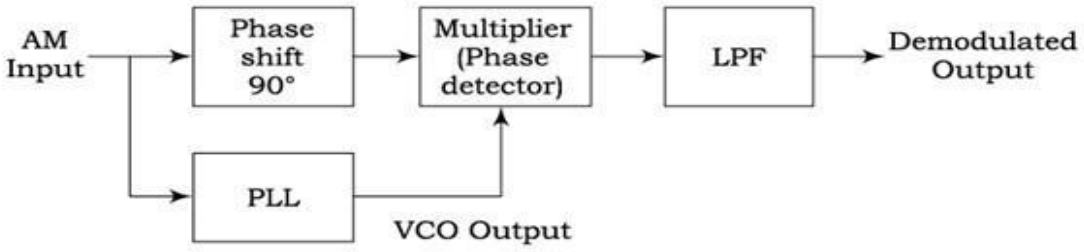
****

1.13 Monolithic PLL IC 565 applications:

1.13.1 AM Demodulation:

Draw the circuit of PLL as AM detection and explain its working. [Nov/Dec 2022]***[May 2011, May 2012]***

- ✓ A PLL used to demodulate AM signals as shown in the figure below.
- ✓ The PLL is locked to the carrier frequency of the incoming AM signal.
- ✓ The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier.
- ✓ Since VCO output is always 90^0 it is being fed to the multiplier.
- ✓ This makes both the signals applied to the multiplier and the difference signals.
- ✓ The demodulated output is obtained after filtering high frequency components by the LPF.
- ✓ Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

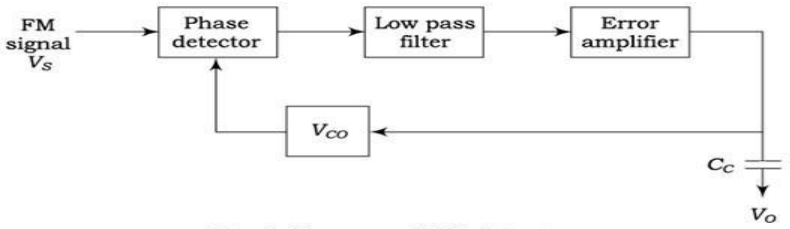


PLL used as AM demodulator

1.13.2 FM Demodulation:

Explain with neat block diagram, how PLL is used for FM demodulation. ***[May 2012]***

- If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal.
- The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.
- The VCO transfer characteristics determine the linearity of the demodulated output.
- Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.



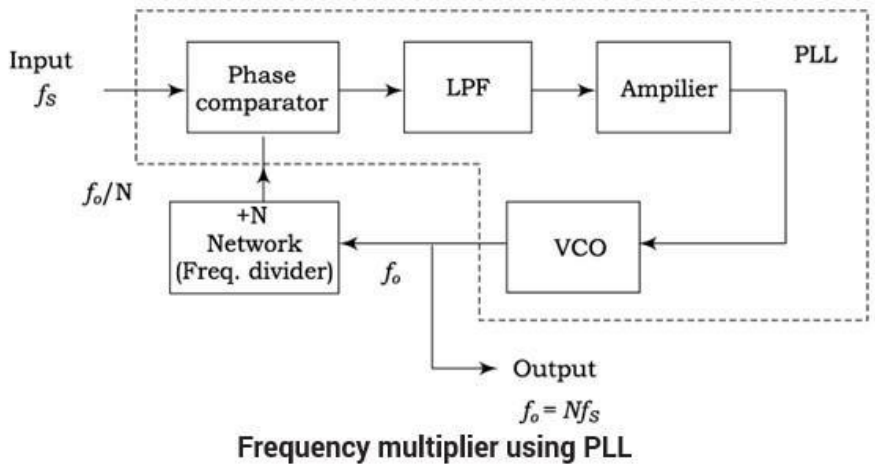
Block diagram of FM detector

1.13.3 Frequency multiplication/division:

How PLL can be modeled as a frequency multiplier. ***[May 2016]***

Brief the application of PLL IC for frequency multiplication. [Nov/Dec 2021] [Nov/Dec 2022] ***[Nov 2016]***

- The block diagram shown below shows a frequency multiplier/divider using PLL.
- A divide by N network is inserted between the VCO output and the phase comparator input.
- In the locked state, the VCO output frequency f_o is given by $f_o = Nf_s$.
- The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.
- Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.
- If the input signal is rich in harmonics e.g. square wave, pulse train etc., then the VCO can be directly locked to the n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n.
- Typically n is kept less than 10.



Frequency multiplier using PLL

1.13.4 FSK Generator:

Draw the FSK modulator and demodulator and explain its operation.[April2021]

- ✓ The FSK generator is formed by using a 555 as an astable multivibrator, whose frequency is controlled by the state of transistor Q_1.
- ✓ In other words, the output frequency of the FSK generator depends on the logic state of the digital data input.
- ✓ 150 Hz is one the standards frequencies at which the data are commonly transmitted.
- ✓ When the input is logic 1, the transistor Q_1 is off.
- ✓ Under the condition, 555 timer works in its normal mode as an astable multivibrator.
- ✓ i.e., capacitor C charges through R_A & R_B to 2/3 Vcc & discharges through R_B to 1/3 V_{cc}.
- ✓ Thus capacitor C charges & discharges between 2/3 V_{cc} & 1/3 V_{cc} as long as the input is logic 1.
- ✓ The frequency of the output waveform is given by,

$$fo = \frac{1.45}{(RA + 2RB)C} = 1070 \text{ Hz (mark frequency)}$$

- ✓ When the input is logic 0, (Q_1 is ON saturated) which in turn connects the resistance R_C across R_A.
- ✓ This action reduces the charging time of capacitor C1 increases the output frequency, which is given by,

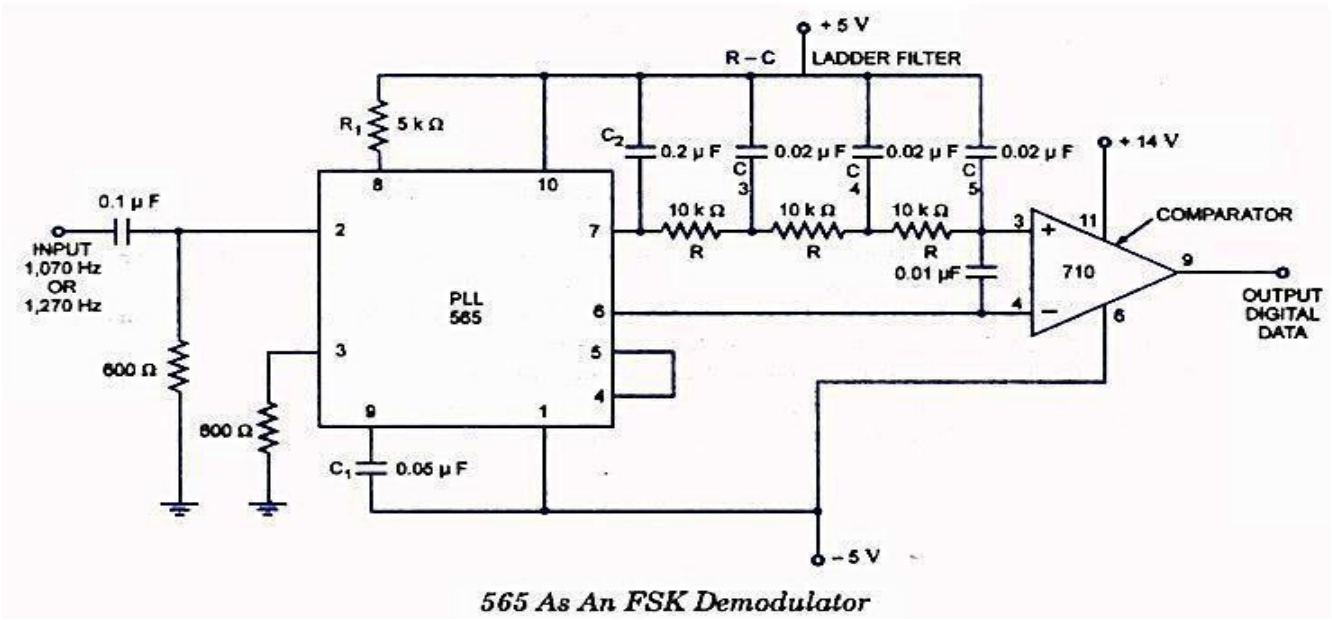
$$fo = \frac{1.45}{(RA \parallel RC + 2RB)C} = 1270 \text{ Hz (space frequency)}$$

- ✓ By proper selection of resistance R_C, this frequency is adjusted to equal the space frequency of 1270 Hz.
- ✓ The difference between the FSK signals of 1070 Hz & 1270 Hz is 200 Hz, this difference is called "frequency shift".
- ✓ The output 150 Hz can be made by connecting a voltage comparator between the output of the ladder filter and pin 6 of PLL.
- ✓ The VCO frequency is adjusted with R_1 so that at f_{IN} = 1070 Hz.

1.13.5 FSK Demodulation:

Explain how IC 565 PLL can be used as FSK demodulator. ***[Nov 2011]***

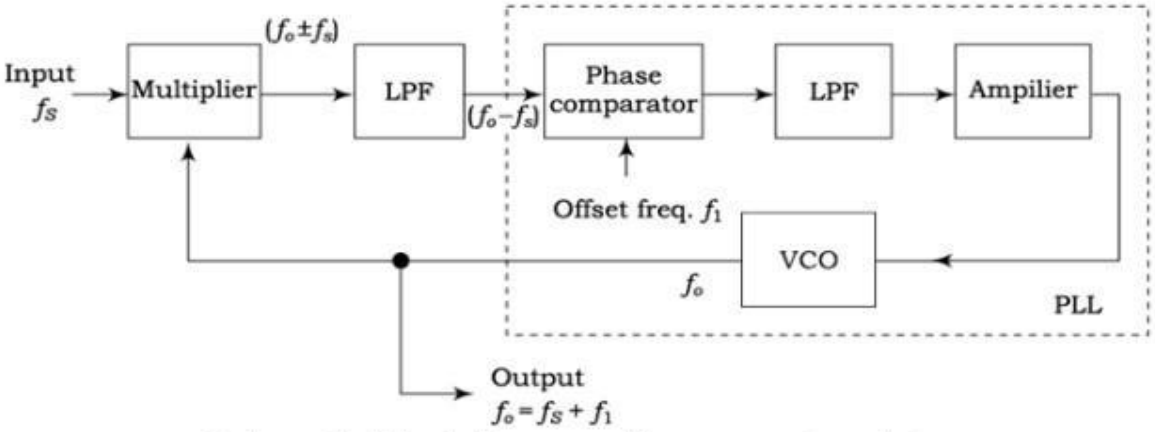
- ✓ The output of 555 FSK generators is applied to the 565 FSK demodulator.
- ✓ Capacitive coupling is used at the input to remove dc line.
- ✓ At the input of 565, the loop locks to the input frequency & tracks it between the 2 frequencies.
- ✓ R_1 & C_1 determine the free running frequency of the VCO.
- ✓ 3 stages RC ladder filter is used to remove the carrier component from the output.



565 As An FSK Demodulator

1.13.6 Frequency translation: Explain frequency translation using PLL.[Nov/Dec2021]

- ✓ The frequency translation means shifting the frequency of an oscillator by a small factor.
- ✓ The figure below shows the block schematic for frequency translator using PLL.
- ✓ It consists of mixer, low pass filter and the PLL.
- ✓ The input frequency f_S which have to be shifted are applied to the mixer.
- ✓ Another input to the mixer is the output voltage of VCO, f_0.
- ✓ Therefore, the output of mixer contains the sum and difference signal ($f_0 \pm f_S$).
- ✓ The low pass filter connected at the output of mixer rejects the ($f_0 + f_S$) signal and gives only ($f_0 - f_S$) signal at the output.
- ✓ The ($f_0 - f_S$) signal is applied to the phase detector.
- ✓ Another input for phase detector is the offset frequency f_1.
- ✓ In the locked mode, the VCO output frequency is adjusted to make two input frequencies of phase detector equal.

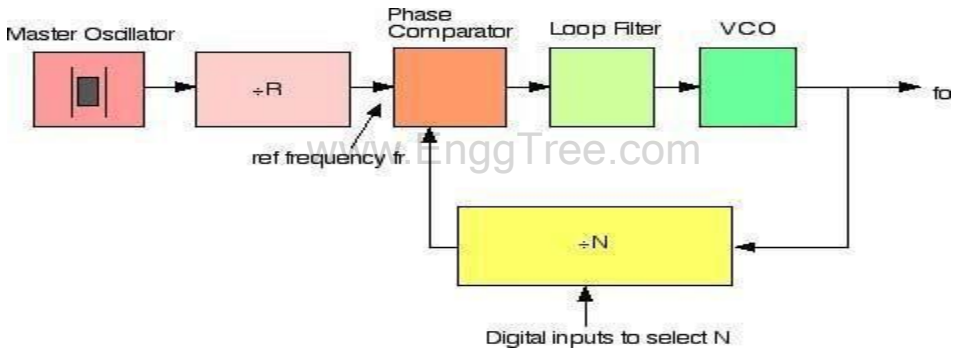


Schematic block diagram of frequency translator

1.13.7 Frequency Synthesizer:

Explain with neat block diagram, how PLL used for frequency synthesizer. [Dec 2018] ***[May 2012]***

- ✓ A phase locked loop compares the frequencies of two signals.
- ✓ It produces an error signal which is proportional to the difference between the input frequencies.
- ✓ The error signal is then low pass filtered and used to drive a voltage-controlled oscillator (VCO) which creates an output frequency.
- ✓ The output frequency is fed through a frequency divider back to the input of the system, producing a negative feedback loop.
- ✓ If the output frequency drifts, the error signal will increase, driving the frequency in the opposite direction so as to reduce the error.
- ✓ Thus the output is locked to the frequency at the other input.
- ✓ This input is called the reference and is derived from a crystal oscillator, which is very stable in frequency.
- ✓ The block diagram below shows the basic elements and arrangement of a PLL based frequency synthesizer.



- ✓ The key to the ability of a frequency synthesizer to generate multiple frequencies is the divider placed between the output and the feedback input.
- ✓ This is usually in the form of a digital counter, with the output signal acting as a clock signal.
- ✓ The counter is preset to some initial count value, and counts down at each cycle of the clock signal.
- ✓ When it reaches zero, the counter output changes state and the count value is reloaded.
- ✓ This circuit is straightforward to implement using flip-flops.
- ✓ It is digital in nature.
- ✓ It is very easy to interface to other digital components or a microprocessor.
- ✓ This allows the frequency output by the synthesizer to be easily controlled by a digital system.

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UNIT- III (Two Marks)

Anolog Multiplier and PLL

1. List the basic building blocks of PLL.

The basic building blocks of PLL are:

- Phase detector/comparator
- Low pass filter
- Error amplifier
- Voltage controlled oscillator

2. Define FSK modulation. [Nov/Dec2021] **[May 2010]**

FSK is a type of frequency modulation, in which the binary data or code is transmitted by means of a carrier frequency that is, shifted between two fixed frequencies namely mark (logic 1) and space frequency (logic 0).

3. What is analog multiplier? **[May 2010]**

A multiplier produces an output V_0, which is proportional to the product of two inputs v_x and v_y.

$$V_0 = kv_xv_y$$

4. List out the various methods available for performing an analog multiplier.

The following methods are available for analog multiplier,

- Logarithmic summing technique
- Pulse height /width modulation technique
- Variable transconductance technique
- Multiplication using gilbert cell
- Multiplication technique using transconductance technique

5. Mention some areas where PLL is widely used. **[Dec 2009]**

The PLL principle has been used in applications such as

- ✓ FM stereo decoders
- ✓ Motor speed control
- ✓ Tracking filters
- ✓ FM modulation and demodulation
- ✓ FSK modulation
- ✓ Frequency multiplier
- ✓ Frequency synthesis etc.,

6. What are the three stages through which PLL operates?

The stages of PLL operation are,

- Free running

- Capture
- Locked/ tracking

7. Define lock-in range of a PLL. [May 2010]

- The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range.
- It is expressed as a percentage of the VCO free running frequency.

8. Define capture range of PLL. [May 2010]

- The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range.
- It is expressed as a percentage of the VCO free running frequency.

9. Write the expression for FSK modulation. [May 2010]

The expression (or) output of FSK demodulation is $\Delta v_f = f_2 - f_1 / k_0$

10. What is free running mode? [May 2010]

- Free running mode is an interactive computer mode that allows more than one user to have simultaneous use of a program.

11. For perfect lock, what should be the phase relation between the incoming signal and VCO output signal?

The VCO output should be 90 degrees out of phase with respect to the input signal.

12. Mention the classification of phase detector.

The phase detector can be classified as:

- Analog phase detector
- Digital phase detector

13. What is a switch type phase detector?

- An electronic switch is opened and closed by the signal coming from VCO.
- The input signal is chopped at a repetition rate determined by the VCO frequency.
- This type of phase detector is called a half wave detector since the phase information for only one half of the input signal is detected and averaged.

14. What are the problems associated with switch type phase detector?

- The output voltage V_e is proportional to the input signal amplitude.
- This is undesirable because it makes phase detector gain and loop gain dependent on the input signal amplitude.
- The output is proportional to cosφ making it non-linear.

15. What is a voltage controlled oscillator?

- Voltage controlled oscillator is a free running multivibrator operating at a set frequency called the

free running frequency.

- This frequency can be shifted to either side by applying a dc control voltage.
- The frequency deviation is proportional to the dc control voltage.

16. Define Voltage to Frequency conversion factor.

Voltage to Frequency conversion factor is defined as, $K_v = f_o / V_c = 8f_o / V_{cc}$.

Where, V_c is the modulation voltage.

f_o is the frequency shift.

17. What is the purpose of having a low pass filter in PLL?

The purpose of having a low pass filter in PLL is:

- It removes the high frequency components and noise.
- Controls the dynamic characteristics of the PLL such as capture range, lock-in range, band-width and transient response.
- The charge on the filter capacitor gives a short- time memory to the PLL.

18. Mention the effect of having large capture range.

- The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the frequency goes beyond the lock-in range.
- Thus, to increase the ability of lock range, large capture range is required.
- But, a large capture range will make the PLL more susceptible to noise and undesirable signal.

19. Name a few applications of an analog multiplier. [Dec 2021] **[Nov/Dec 2009] [Apr/May 2017]** [Nov/Dec 2022]

Applications of analog multiplier are:

- Frequency doubling.
- Frequency shifting.
- Phase angle detection.
- Squaring.
- Multiplication.
- Division.
- Waveform generation.

20. Define pull time of PLL.

Pull time of a PLL is defined as the total time taken by the PLL to establish lock.

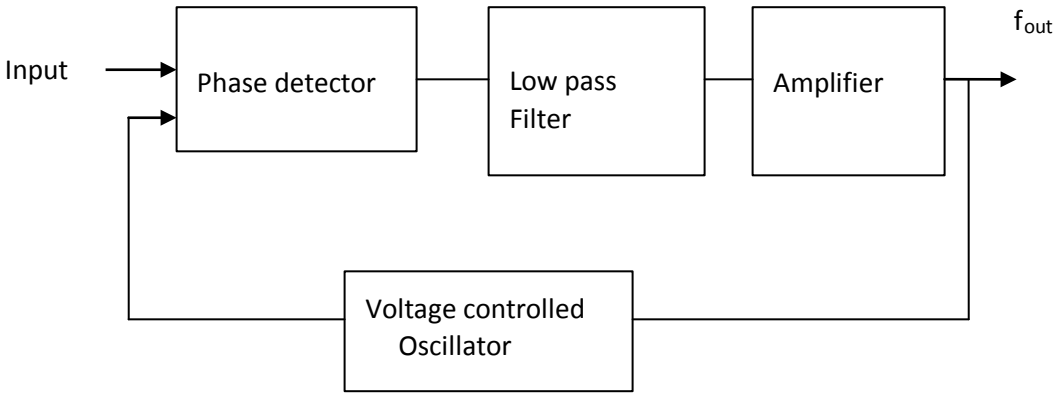
21. What are the functional blocks of PLL? **[April/May 2010]**

The functional blocks of PLL are,

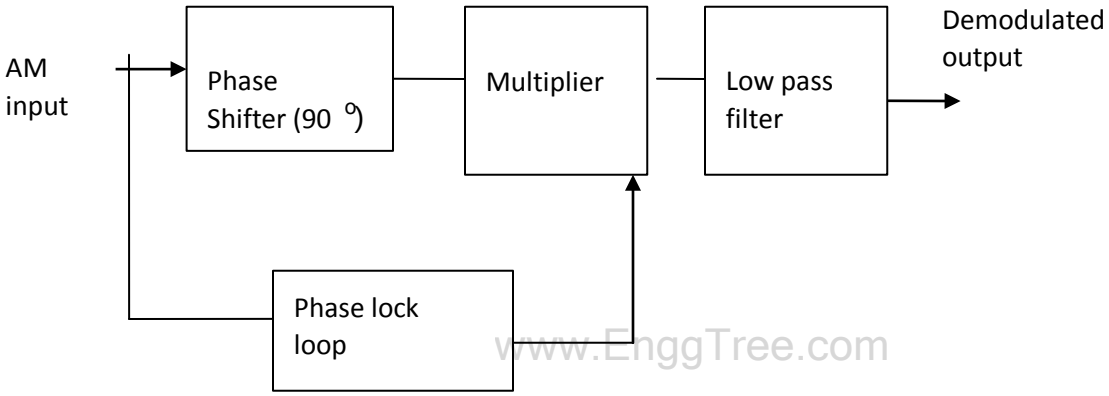
- Comparator
- Low pass filter.

- Error amplifier.
- Voltage controlled oscillator.

22. Draw the functional block diagram of a PLL.



23. Draw circuit diagram of an AM detector using PLL. **[May/June 2009]**

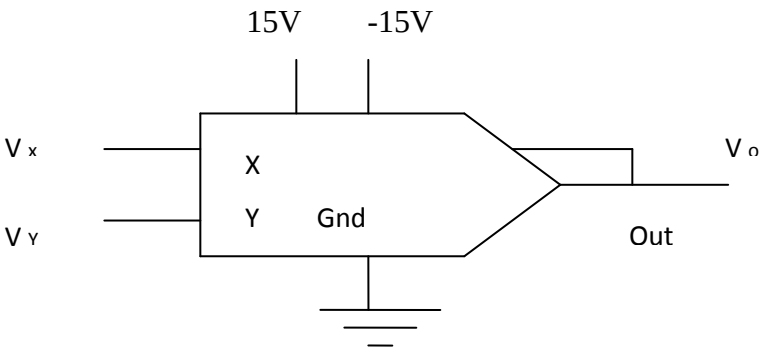


24. Mention a few applications of PLL. [Dec 2018[**[Nov/Dec 2009]**

The applications of PLL are:

- Frequency multiplication.
- Frequency division.
- AM detection.
- FM detection.
- FSK demodulator.
- Frequency translation.

25. Give the schematic symbol of multiplier.



26. Define multiplier.

- The multipliers are defined as circuits used for multiplying two applied signals.
- Apart from this, multipliers can be used for phase angle detection, frequency doubling and shifting and for demonstrating the principle of amplitude modulation and demodulation.

27. Give the classification of multiplier.

The classification of multipliers is:

- One- quadrant multiplier.
- Two- quadrant multiplier.
- Three - quadrant multiplier.
- Four- quadrant multiplier.

28. List the characteristics of multipliers. [Dec 2018]

The characteristics of multipliers are:

- Bandwidth.
- Feed through.
- Zero train.
- Quadrant.
- Scale factor.
- Scale-factor train.
- Accuracy.
- Linearity.

29. What is a trans-conductance multiplier?

- Log-amps require the input and reference voltages to be of the same polarity.
- This restricts log-antilog multipliers to one quadrant operation.
- A technique that provides four quadrant multiplication is called trans-conductance multiplier.

30. What is a four quadrant multiplier?

- If both inputs are positive, the IC is said to be a one-quadrant multiplier.
- A two- quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative.
- If both inputs are either positive or negative, the IC is called a four quadrant multiplier.

31. List the various multiplier techniques.

The various multiplier techniques are:

- Logarithmic multipliers
- Quarter square multipliers
- Pulse width/height modulation multipliers

- Variable trans-conductance multipliers.

32. What is the range of modulating input voltage applied to a voltage controlled oscillator?

The modulating input voltage ranges from 0.75 V_{cc} to 1 V_{cc}.

33. Define VCO.

- The VCO is a free running multivibrator and operates at a set frequency called free running frequency.
- This frequency is determined by an external timing capacitor and an external resistor.

34. List the features of VCO. [April/May 2021]

The features of VCO are:

- Wide supply voltage range from 10V to 24V.
- Very linear modulation characteristics.
- High temperature stability.
- Excellent power supply rejection.
- 10 to 1 frequency range with fixed C.
- The frequency can be controlled by means of a control voltage resistor or capacitor.

35. Give the applications of VCO.

The applications of VCO are:

- FM modulation.
- Signal generation(triangular or square wave)
- Function generation.
- In frequency multipliers.
- Converting low frequency signals such as EEG and ECG into audio frequency range signals.

36. What are the different stages of operation in a PLL?

The different stages of operation in a PLL are,

- Free running range.
- Capture range.
- Locked or tracking range.

37. Define lock-in range. [April/May 2021] **[April/May 2008][Nov/Dec 2015]**

The range of frequency over which the PLL can maintain lock with the incoming signal is called the lock-in range.

38. What is meant by capture range of PLL? **[April/May 2008][Nov/Dec 2015]**

The range of frequency over which the PLL can acquire lock with an input signal is called capture range.

39. Give the types of analog phase detectors and digital phase detectors.

The types of analog phase detectors are as follows:

- Switch type phase detector.
- Balanced modulator type phase detector.

The types of digital phase detectors are as follows:

- X-OR phase detector.
- Flip-flop phase detectors.

40. List the advantages of flip-flop type phase detector over EX-OR phase detector.

The flip flop phase detector has the following advantages over the EX-OR circuit:

- The dc output voltage is linear over 2π radians or 360^o, as opposed to π or 180^o in the case of EX-OR detector.
- The flip-flop detector exhibits between capture, tracking, and locking characteristics than the EX-OR detector.
- The RS flip-flop works best with low duty cycle (50%) input waveform. However both the types of detectors are sensitive to harmonics of the input signal and change in duty cycle of f_i and f_o.

41. What should be the phase difference between the input signal and voltage controlled oscillator output to active lock?

Input signal and voltage controlled oscillator should be 90^o out of phase with each other.

42. A PLL has a free running frequency of 500 kHz and bandwidth of the low pass filter is 10 kHz. Will the loop acquire lock for an input signal of 600 kHz? Justify your answer. Assume that the phase detector produces 50 m and difference frequency components.

The phase detector output

$f_i + fc$ = 600 kHz + 500 kHz

= 1100 kHz

$f_i - fc$ = 600 kHz + 500 kHz

= 100 kHz

As both the components are outside the pass band of low pass filter, the loop will not acquire lock.

43. Give the advantages of variable Transconductance technique.

The advantages of variable Transconductance technique are,

- Good accuracy.
- Economical.
- Simple to integrate into monolithic chip.
- Higher bandwidth.

44. What is companding?

- The combination of words compression and expanding in a communication system is called companding.
- The compression is done in the transmitter and expanding is done in the receiver.

45. What is the purpose of companding?

The purpose of companding is to preserve the signal to noise ratio of the original signal and to avoid nonlinear distortion of the signal when the input amplitude is large.

46. Define scale factor of multiplier.

Scale factor is proportionally constant (k) relating the output voltage and the product of two input voltage.

$$k = (V_0 / V_1 V_2).$$

47. What is an OTA?

An OTA (Operational Transconductance amplifier) is a voltage-input current output amplifier.

48. Give the applications of OTA.

Some of the applications of OTA are,

- Programmable gain voltage amplifier.
- Sample and hold circuits.
- Programmable resistor or electronically tunable resistor or voltage controlled resistor.
- Current-controlled relaxation oscillator.
- Integrators in audio processing.
- Electronic music synthesis.

49. What is the need for frequency synthesizer? [May/June 2014]

- The frequency synthesizer is used to produce a large number of precise frequencies which are derived from a single reference source of frequency.
- The reference source usually is a crystal oscillator.

50. What are advantages of emitter coupled transistor pair? [April/ May 2011]

The advantages of emitter coupled transistor pair are,

- High current gain
- More stability
- Compact and easily implemented in IC

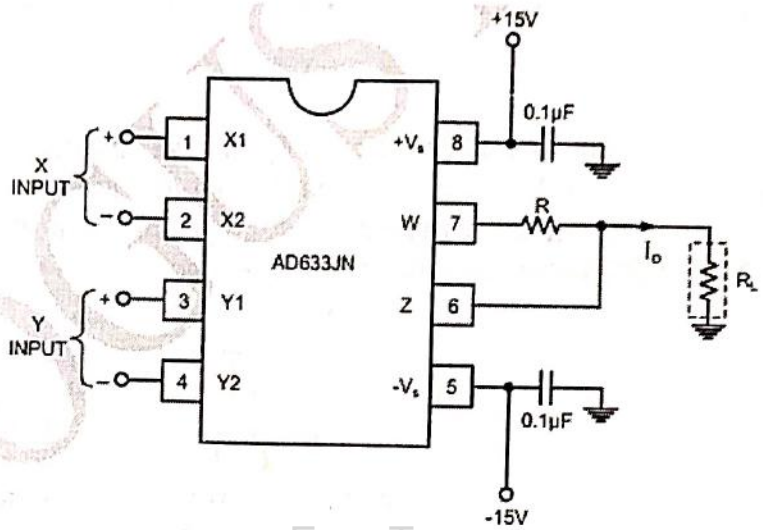
****

Part A

1. State the importance of active filter in PLL with neat sketches. [Nov/Dec 2022]

The charge on the filter capacitor gives a short time memory to the PLL. So, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of VCO, till it picks up the signal again.

2. Draw the pin diagram of AD633. [Nov/Dec 2022]



PART B

1) A VCO has a free running frequency of 21KHz/V & the input signal frequency $f_s = 20\,KHz$ & $k_V = 4\,KHz/V$. Find the change in the dc control voltage V_c during the lock time. [Nov/Dec 2022]

$$\Delta V_c = \frac{f_2 - f_1}{k_V}$$

$f_2 \rightarrow$ Free running frequency

$f_1 \rightarrow$ input signal frequency.

$f_2 = 21KHz, \quad f_1 = 20KHz$

$$\Delta V_c = \frac{(21-20)\times 10^3}{4\times 10^3} = \frac{1}{4} = 0.25V.$$

UNIT IV

ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

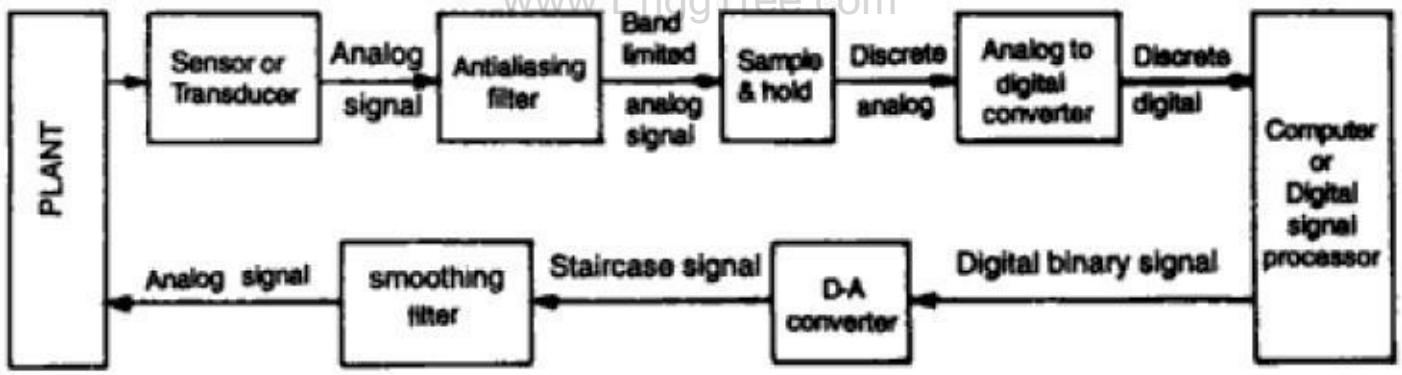
Analog and Digital Data Conversions, D/A converter – specifications - weighted resistor type, R-2R Ladder type, Voltage Mode and Current-Mode R □ 2R Ladder types - switches for D/A converters, high speed sample-and-hold circuits, A/D Converters – specifications - Flash type - Successive Approximation type - Single Slope type – Dual Slope type - A/D Converter using Voltage-to-Time Conversion - Over-sampling A/D Converters.

Introduction:

The transducer circuit will gives an analog signal. This signal is transmitted through the LPF circuit to avoid higher frequencycomponents, and then the signal is sampled at twice the frequency of the signal to avoid the overlapping.

The output of the sampling circuit is applied to A/D converter where the samples are converted into binary data i.e. 0's and 1's. Like this the analog data converted into digital data.

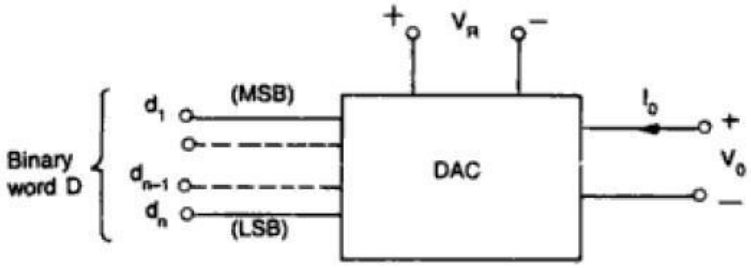
The digital data is again reconverted back into analog by doing exact opposite operation of first half of the diagram. Then the output of the D/A convertor is transmitted through the smoothing filter to avoid the ripples.



Circuit showing application of A/D and D/A converter

Digital to analog converter

Basic DAC techniques:



Schematic of a DAC

The input of the block diagram is binary data i.e, 0 and 1,it contain 'n' number of input bits designated as d1,d2,d3,…..dn .this input is combined with the reference voltage called Vdd to give an analog output. Where d1 is the MSB bit and dn is the LSB bit.

$$V_0 = K\, V_{FS}(d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots\ldots + d_n 2^{-n})$$

Where , V_0 = output voltage

V_{FS} = full scale output voltage

K = scaling factor

Digital to Analog Specifications

Explain the specifications of DAC. (May 2013)

D/A converters are available with wide range of specifications specified by manufacturer. Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

Resolution:

Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = VoFS / (2^n - 1) = 1 LSB increment

Where 'n' is the number of input bits

'VoFS' is the full scale output voltage.

Example: Resolution for an 8 – bit DAC for example is said to have

: 8 – bit resolution

: A resolution of 0.392 of full-Scale (1/255)

: A resolution of 1 part in 255.

Accuracy:

Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. The ideal converter is the one which does not suffer from any problem.

Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

The relative accuracy is the maximum deviation after the gain and offset errors have been removed. Accuracy is also given in terms of LSB increments or percentage of full-scale voltage.

Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

• • •

Linearity:

Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale. The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produce equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity:

A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input. A monotonic characteristic is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Conversion Time:

It is the time taken for the D/A converter to produce the analog output for the given binary input signal. It depends on the response time of switches and the output of the Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Settling time:

It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change). It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances. A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

Stability:

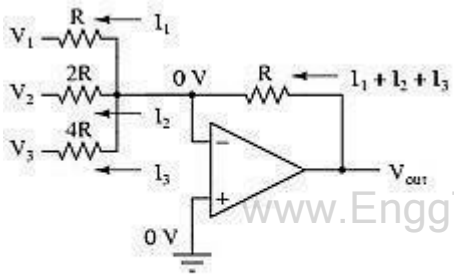
The ability of a DAC to produce a stable output all the time is called as Stability. The performance of a converter changes with drift in temperature, aging and power supply variations. So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet. Temperature sensitivity defines the stability of a D/A converter.

Digital To Analog Conversion Binary-

Weighted Resistor DAC

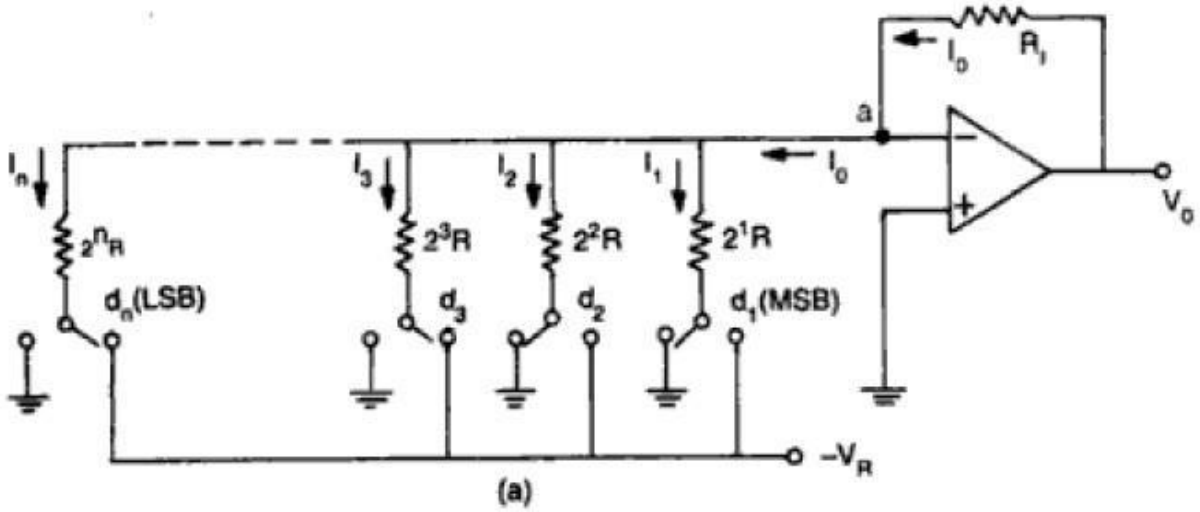
Explain Binary-Weighted Resistor DAC with neat circuit diagram. (May 2014)[Nov/Dec2021]

The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit. In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).



$$V_{out} = -(V_1 + \frac{V_2}{2} + \frac{V_3}{4})$$

Fig. Binary weighted DAC



The binary inputs, ai (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch.

The operational amplifier is used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, Vref.

For a 4-bit DAC, the relationship between Vout and the binary input is as follows:

$$V_{OUT} = -iR_f$$
$$= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f$$
$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right)$$
$$= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)$$

The negative sign associated with the analog output is due to the connection to a summing amplifier, which is a polarity-inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa).

For a n-bit DAC, the relationship between Vout and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref}R_f}{R}\sum_{i=1}^{n}\frac{a_i}{2^i}$$

The LSB, which is also the incremental step, has a value of - 0.625 V while the MSB or the full scale has a value of - 9.375 V.

Practical Limitations:

- ✓ The most significant problem is the large difference in resistor values required between the LSB and MSB, especially in the case of high resolution DACs (i.e. those that has large number of bits). For example, in the case of a 12-bit DAC, if the MSB is 1 k Ω, then the LSB is a staggering 2 MΩ.
- ✓ The maintenance of accurate resistances over a large range of values is problematic. With the current IC fabrication technology, it is difficult to manufacture resistors over a wide resistance range that maintains an accurate ratio especially with variations in temperature.

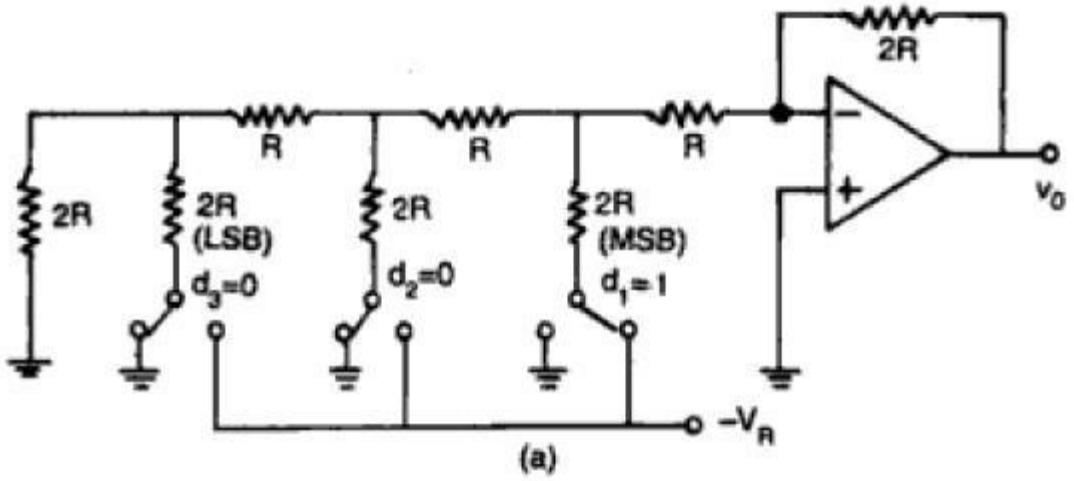
R-2R Ladder DAC

Explain R-2R Ladder DAC with neat circuit diagram. (Nov 2014)[Nov/Dec 2021] [Nov/Dec 2022]

An enhancement of the binary-weighted resistor DAC is the R-2R ladder network. This type of DAC utilizes Thevenin's theorem in arriving at the desired output voltages.

A disadvantage of the former DAC design was its requirement of several different precise input resistor values: one unique value per binary input bit.

The R-2R network consists of resistors with only two values - R and 2R. If each input is supplied either 0 volts or reference voltage, the output voltage will be an analog equivalent of the binary value of the three bits.



Inverted Or Current Mode DAC

Explain current mode DAC with neat circuit diagram.

Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into *i*1 , *i*2, *i*3 ……*i*n. in each arm. The currents are either diverted to the ground bus (*io*) or to the Virtual-ground bus *(io*).

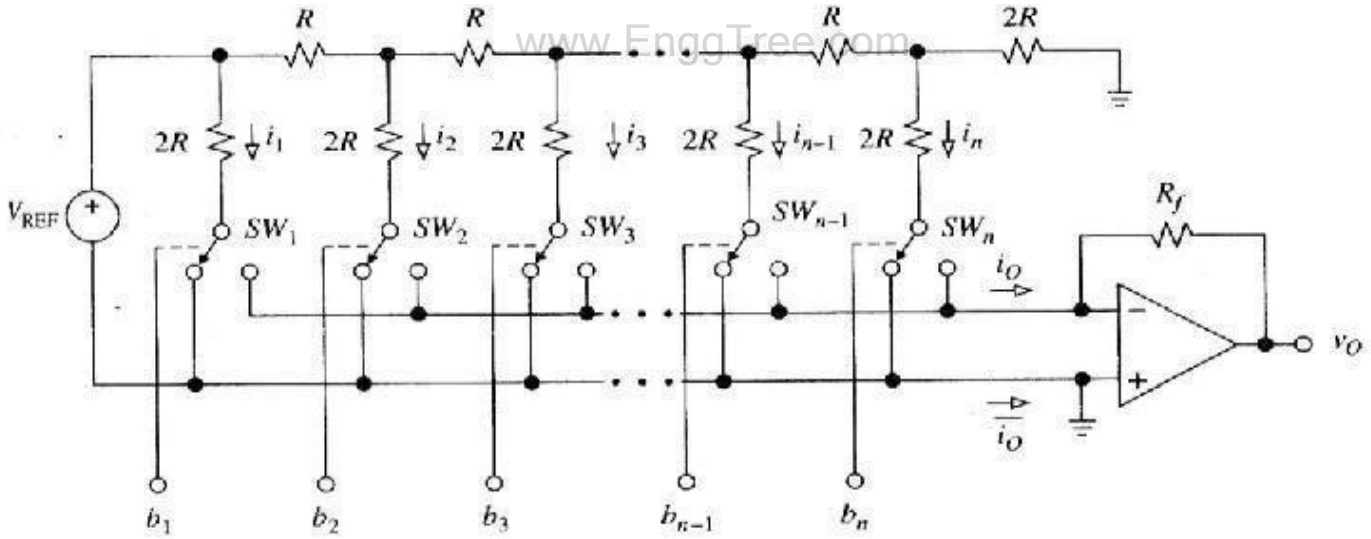


Fig. Current mode DAC

The currents are given as

$i1 = VREF/2R = (VREF/R)\ 2^{-1}$, $i2 = (VREF)/2)/2R = (VREF/R)\ 2^{-2}$……$in = (VREF/R)\ 2^{-n}$.

And the relationship between the currents are given as

i2 = i1/2

i3 = i1/4

i4 = i1/8

$in = i1/\ 2^{n-1}$

Using the bits to identify the status of the switches, and letting V0 = -Rf *io* gives

$V0 = -\ (Rf/R)\ VREF\ (b1\ 2^{-1} + b2\ 2^{-2} + \ldots\ldots\ldots + bn\ 2^{-n})$

Advantages

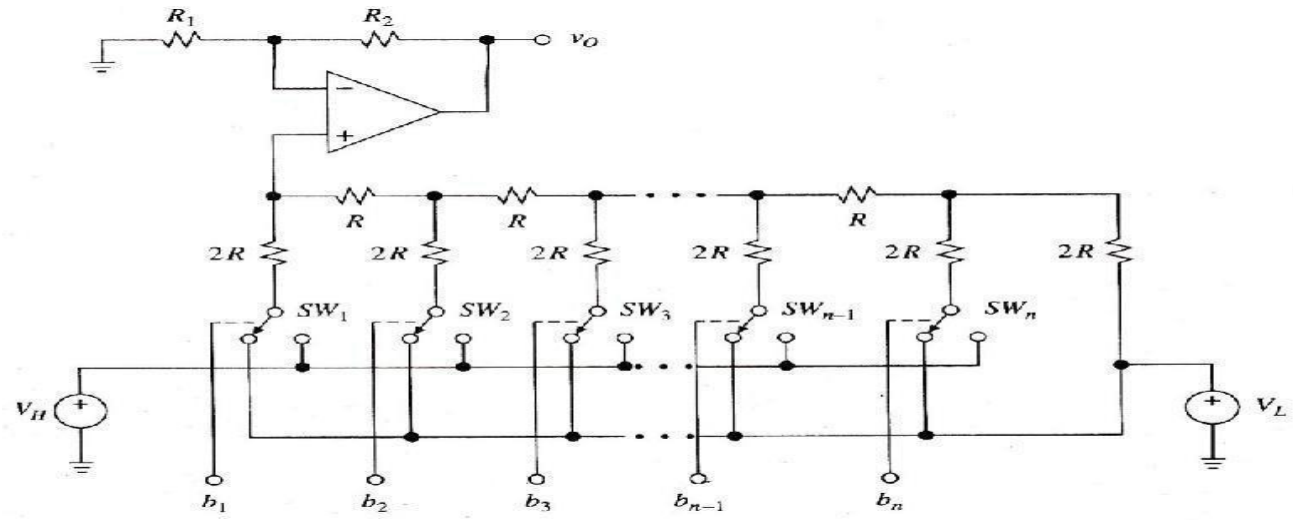
1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.

2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the Speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

Voltage Mode DAC

This is the alternative mode of DAC and is called so because the 2R resistance in the shunt path is switched between two voltages named as VL and VH. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1…..1).

The voltage of this node changes in steps of 2^{-n} (VH - VL) from the minimum voltage of Vo = VL to the maximum of Vo = VH - 2^{-n} (VH - VL).



The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by K = 1 + (R2/R1) results.

Advantages

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.

2. More accurate selection and design of resistors R and 2R are possible and simple construction.

3. The binary word length can be easily increased by adding the required number or R-2R sections.

Switches For DAC

What are the switches used for DAC? Explain its functions.

The Switches which connects the digital binary input to the nodes of a D/A converter is an electronic switch. Although switches can be made of using diodes, bipolar junction Transistors, Field Effect transistors or MOSFETs, there are four main configurations used as switches for DACs. They are

i) Switches using overdriven Emitter Followers.

ii) Switches using MOS Transistor- Totem pole MOSFET Switch and CMOS Inverter Switch.

iii) CMOS switch for Multiplying type DACs.

iv) CMOS Transmission gate switches.

These configurations are used to ensure the high speed switching operations for different types of DACs.

Switches using MOS transistor:

i) Totem pole MOSFET Switch:

As shown in the figure, the totem pole MOSFET Switch is connected in series with resistors of R-2R network. The MOSFET driver is connected to the inverting terminal of the summing op-amp.

The complementary outputs *Q* and *Q* drive the gates of the MOSFET M1 and M2 respectively. The SR flip flop holds one bit of digital information of the binary word under conversion. Assuming the negative logic (-5V for logic 1 and +5V for logic 0) the operation is given as two cases.

Case 1:

When the bit line is 1 with S=1 and R=0 makes *Q*=1 and *Q* =0. This makes the transistor M1 ON, thereby connecting the resistor R to reference voltage -VR. The transistor M2 remains in OFF condition.

Case 2:

When the bit line is 0 with S=0 and R=1 makes *Q*=0 and *Q* =1. This makes the transistor M2 ON, thereby connecting the resistor R to Ground. The transistor M1 remains in OFF condition.

ii) CMOS Inverter Switch:

The figure of CMOS inverter is shown here. It consists of a CMOS inverter connected with an opamp acting as a buffer. The buffer drives the resistor R with very low output impedance. Assuming positive logic (+5V for logic 1 and 0V for logic 0), the operation can be explained in two cases.

Case1:

When the complement of the bit line *Q* is low, M1 becomes ON connecting VR to the non- inverting input of the op-amp. This drives the resistor R HIGH.

Case2:

When the complement of the bit line *Q* is high, M2 becomes ON connecting Ground to the non- inverting input of the op-amp. This pulls the resistor R LOW (to ground).

High Speed Sample and Hold Circuits

Explain sample and hold circuits. [Nov/Dec 2022]

Introduction:

Sample-and-hold (S/H) is an important analog building block with many applications, including analog-to-digital converters (ADCs) and switched-capacitor filters. The function of the S/H circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

Taking advantages of the excellent properties of MOS capacitors and switches, traditional switched capacitor techniques can be used to realize different S/H circuits.

The simplest S/H circuit in MOS technology is shown in Figure 1, where *Vin* is the input signal, M1 is an MOS transistor operating as the sampling switch, Ch is the hold capacitor, ck is the clock signal, and Vout is the resulting sample-and-hold output signal.

As depicted by Figure, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward.

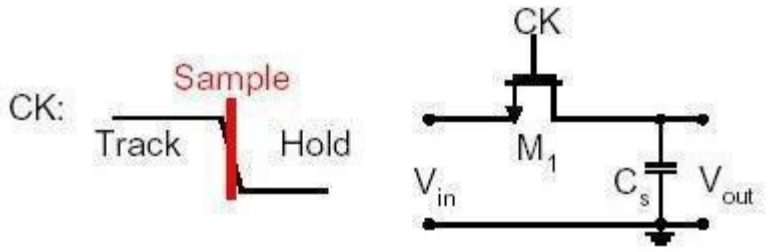


Figure 4.7 Simplest sample-and-hold circuits in MOS technology.

Figure 4.7, in the simplest sense, a S/H circuit can be achieved using only one MOS transistor and one capacitor. The operation of this circuit is very straightforward. Whenever *ck* is high, the MOS switch is on,

which in turn allows *Vout* to track *Vin*. On the other hand, when *ck* is low, the MOS switch is off. During this time, *Ch* will keep *Vout* equal to the value of *Vin* at the instance when *ck* goes low.

Alternative CMOS Sample-and-Hold Circuits

Three alternative CMOS S/H circuits that are developed with the intention to minimize charge injection and/or clock feed through are:

Series Sampling:

The S/H circuit of Figure 4.7. is classified as parallel sampling because the hold capacitor is in parallel with the signal. In parallel sampling, the input and the output are dc-coupled. On the other hand, the S/H circuit shown in Figure 4.8 is referred to as series sampling because the hold capacitor is in series with the signal.

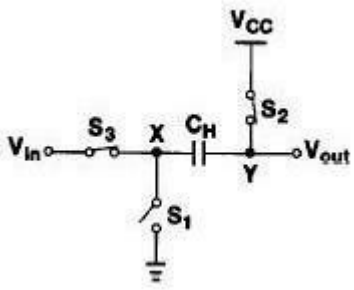


Figure 4.8 Series sampling.

When the circuit is in sample mode, both switches *S2* and *S3* are on, while *S1* is off. Then,*S2* is turned off first, which means *Vout* is equal to *VCC* (or *VDD* for most circuits) and the voltage drop across *Ch* will be *VCC – Vin*. Subsequently, *S3* is turned off and *S1* is turned on simultaneously. By grounding node *X*, *Vout* is now equal to *VCC –Vin*, and the drop from *VCC* to *VCC – Vin* is equal to the instantaneous value of the input.

As a result, this is actually an inverted S/H circuit, which requires inversion of the signal at a later stage. Since the hold capacitor is in series with the signal, series sampling can isolate the common- mode levels of the input and the output.

This is one advantage of series sampling over parallel sampling. In addition, unlike parallel sampling, which suffers from signal-dependent charge injection, series sampling does not exhibit such behavior because *S2* is turned off before *S3*. Thus, the fact that the gate-to-source voltage, *VGS*, of *S2* is constant means that charge injection coming from *S2* is also constant (as opposed to being signal-dependent), which means this error can be easily eliminated through differential operation.

Limitations:

On the other hand, series sampling suffers from the nonlinearity of the parasitic capacitance at node *Y*.

This parasitic capacitance introduces distortion to the sample-and hold value, thus mandating that *Ch* be much larger than the parasitic capacitance. On top of this disadvantage, the settling time of the S/H circuit during hold mode is longer for series sampling than for parallel sampling. The reason for this is because the value of

Vout in series sampling is being reset to *VCC* (or *VDD*) for every sample, but this is not the case for parallel sampling.

Switched Op-Amp Based Sample-and-Hold Circuit:

This S/H technique takes advantage of the fact that when a MOS transistor is in the saturation region, the channel is pinched off and disconnected from the drain. Therefore, if the hold capacitor is connected to the drain of the MOS transistor, charge injection will only go to the source junction, leaving the drain unaffected. Based on this concept, a switched op- amp (SOP) based S/H circuit, as shown in Figure 4.9

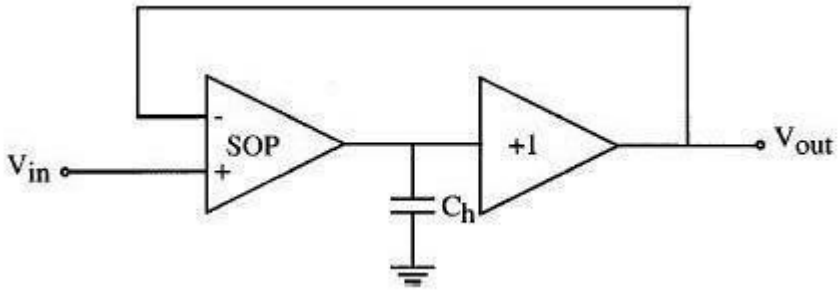
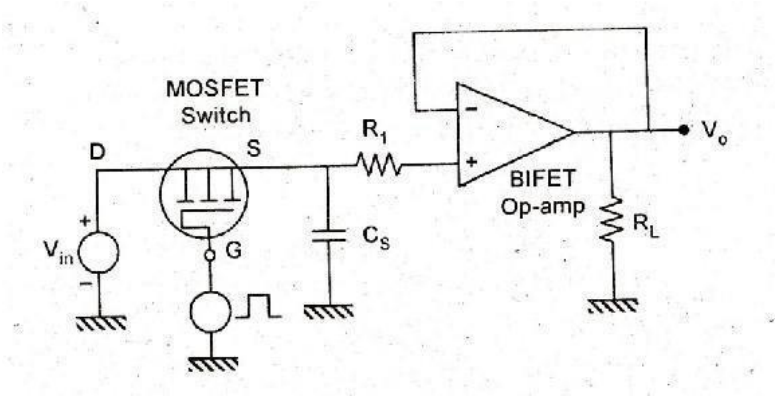


Fig. 4.9 Switched op-amp based sample and hold circuit.

During sample mode, the SOP behaves just like a regular op-amp, in which the value of the output follows the value of the input. During hold mode, the MOS transistors at the output node of the SOP are turned off while they are still operating in saturation, thus preventing any channel charge from flowing into the output of the SOP.

In addition, the SOP is shut off and its output is held at high impedance, allowing the charge on *Ch* to be preserved throughout the hold mode. On the other hand, the output buffer of this S/H circuit is always operational during sample and hold mode and is always providing the voltage on *Ch* to the output of the S/H circuit.

S/H circuits that operate in closed loop configuration can achieve high resolution, but their requirements for high gain circuit block, such as an op-amp, limits the speed of the circuits. As a result, better and faster S/H circuits must be developed.



The above figure shows a sample and holds circuit with MOSFET as Switch acting as a sampling device and also consists of a holding capacitor Cs to store the sample values until the next sample comes in. This is a high speed circuit as it is apparent that CMOS switch has a very negligible propagation delay.

Three S/H circuits to reduce error:

- ✓ Series sampling,
- ✓ SOP based S/H circuit,
- ✓ Bottom plate S/H circuit with bootstrapped switch

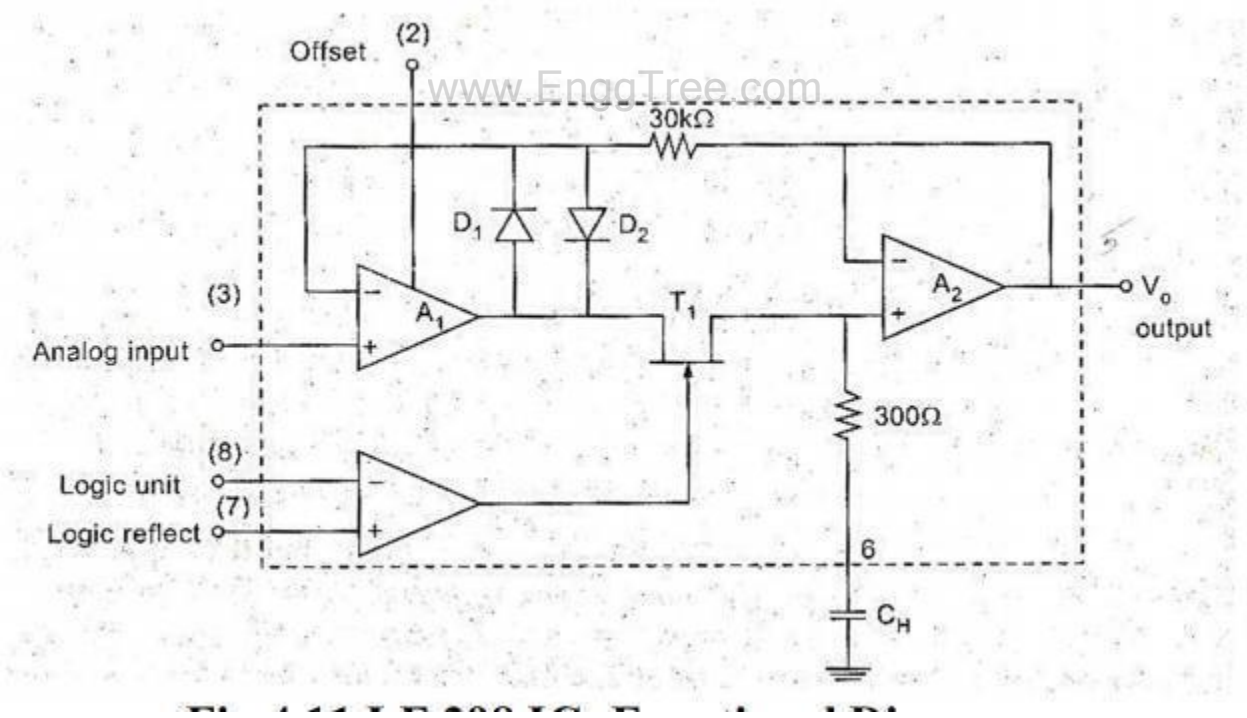


Fig. LF 398 IC- Functional Diagram

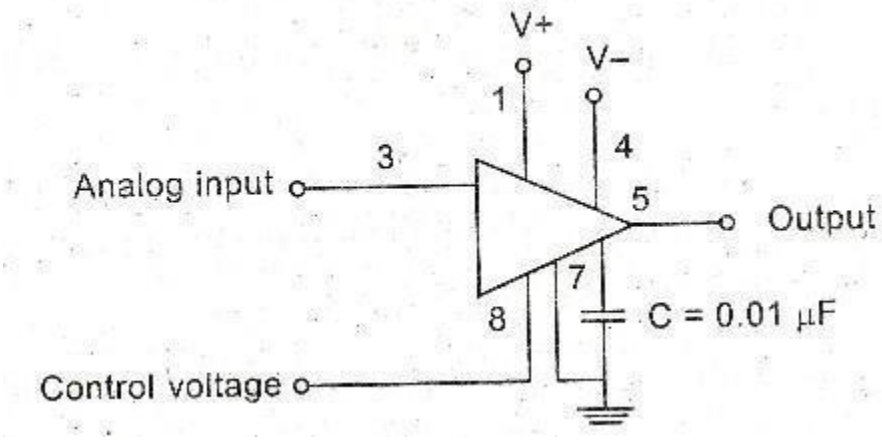


Fig. Connections of S&H IC

Analog to Digital Converter- Specifications

Explain the specifications used for ADC. (May 2014)

Like DAC, ADCs are also having many important specifications. Some of them are Resolution, Quantization error, Conversion time, Analog error, Linearity error, DNL error, INL error & Input voltage range.

Resolution:

The resolution refers to the finest minimum change in the signal which is accepted for conversion, and it is decided with respect to number of bits. It is given as 1/2n, where 'n' is the number of bits in the digital output word. As it is clear, that the resolution can be improved by increasing the number of bits or the number of bits representing the given analog input voltage.

Resolution can also be defined as the ratio of change in the value of input voltage Vi, needed to change the digital output by 1 LSB. It is given as

$$\text{Resolution} = ViFS / (2^n - 1)$$

Where 'ViFS' is the full-scale input

voltage. 'n' is the number of output bits.

Quantization error:

If the binary output bit combination is such that for all the values of input voltage Vi between any is a particular binary combination. This uncertainty is termed as quantization error. Its value is ± (1/2) LSB. And it is given as,

$$QE = ViFS / 2(2^n - 1)$$

Where 'ViFS' is the full-scale input

voltage 'n' is the number of output bits.

Maximum the number of bits selected, finer the resolution and smaller the quantization error.

Conversion Time:

It is defined as the total time required for an A/D converter to convert an analog signal to digital output. It depends on the conversion technique and propagation delay of the circuit components.

Analog error:

An error occurring due to the variations in DC switching point of the comparator, resistors, reference voltage source, ripples and noises introduced by the circuit components is termed as Analog error.

Linearity Error:

It is defined as the measure of variation in voltage step size. It indicates the difference between the transitions for a minimum step of input voltage change. This is normally specified as fraction of LSB.

Differential Non-Linearity(DNL) Error:

The analog input levels that trigger any two successive output codes should differ by 1 LSB. Any deviation from this 1 LSB value is called as DNL error.

Integral Non-Linearity (INL) Error:

The deviation of characteristics of an ADC due to missing codes causes INL error. The maximum deviation of the code from its ideal value after nulling the offset and gain errors is called as Integral Non-Linearity Error.

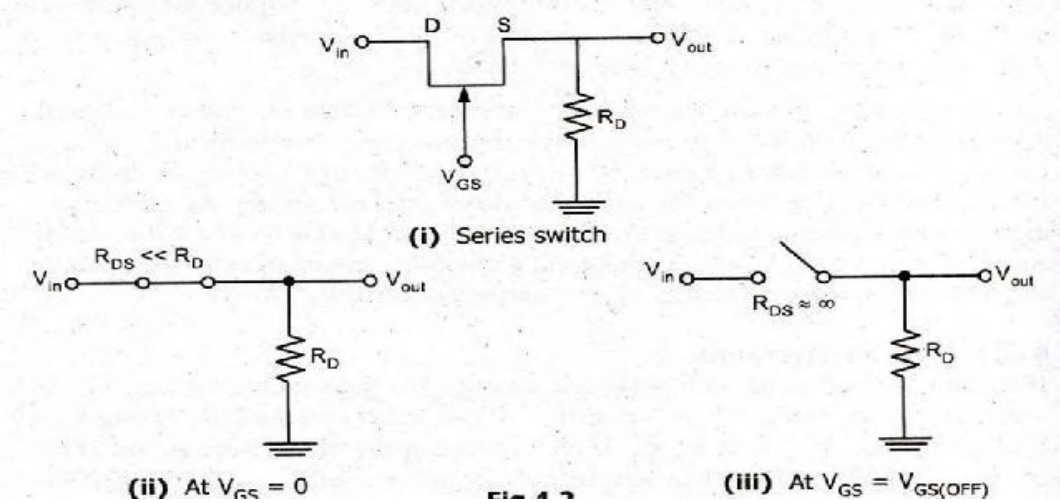
Input Voltage Range:

It is the range of voltage that an A/D converter can accept as its input without causing any overflow in its digital output.

Analog Switches

Explain the different types of analog switches for ADC. (May 2014)

There were two types of analog switches. Series and Shunt switch. The Switch operation is shown for both the cases VGS=0 VGS= VGs (off)



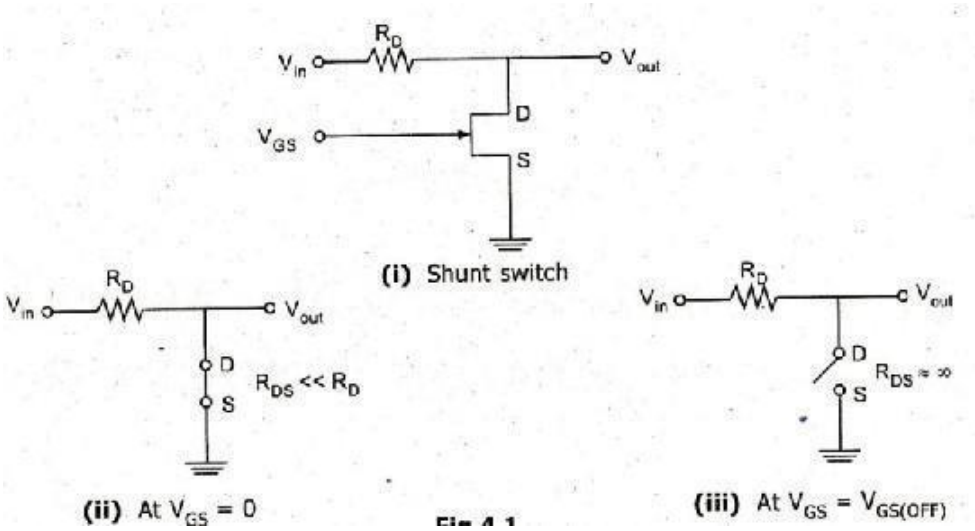
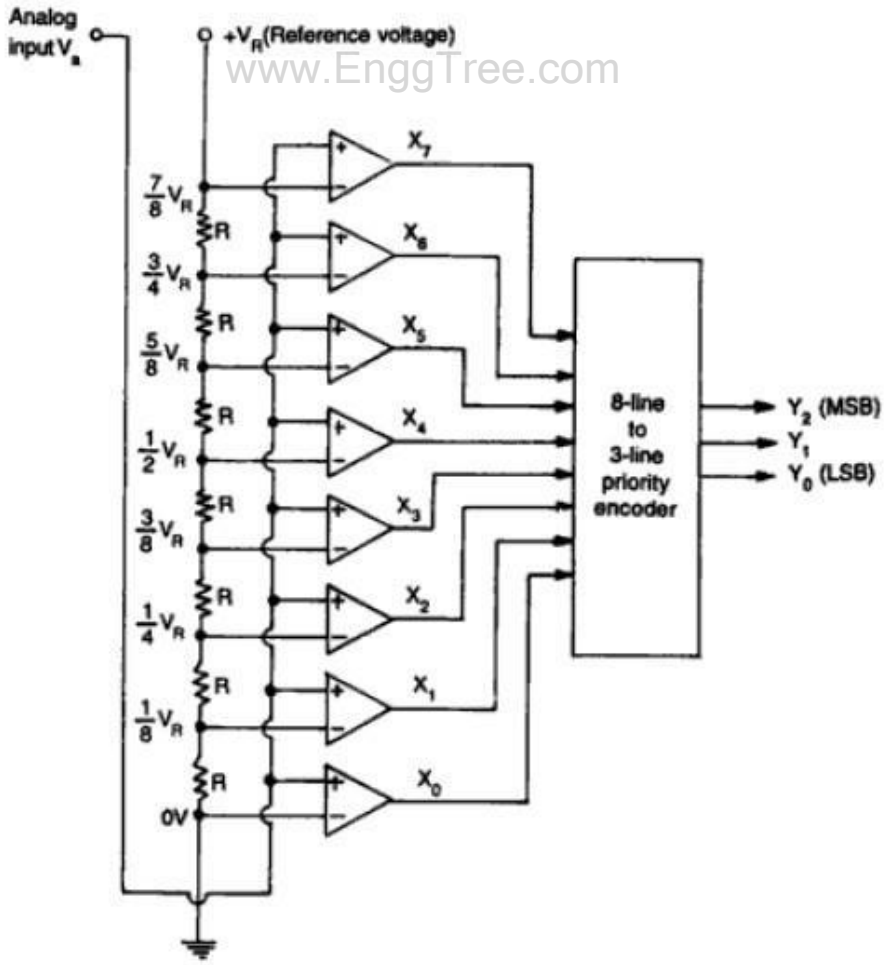


Fig 4.13 Series and shunt Analog switches

Direct-conversion ADC/Flash type ADC

Explain flash type ADC with neat circuit diagram. (Nov 2015)[Nov/Dec 2021] [Nov/Dec 2022]



This process is extremely fast with a sampling rate of up to 1 GHz. The resolution is however, limited because of the large number of comparators and reference voltages required. The input signal is fed simultaneously to all comparators. A priority encoder then generates a digital output that corresponds with the highest activated comparator.

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

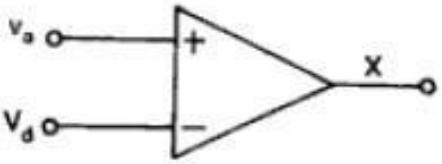


Fig. 10.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Successive-approximation ADCs

Explain Successive approximation type ADC with neat block diagram. (May 2014, 2015)
Explain counter type ADC. [Nov/Dec 2021]

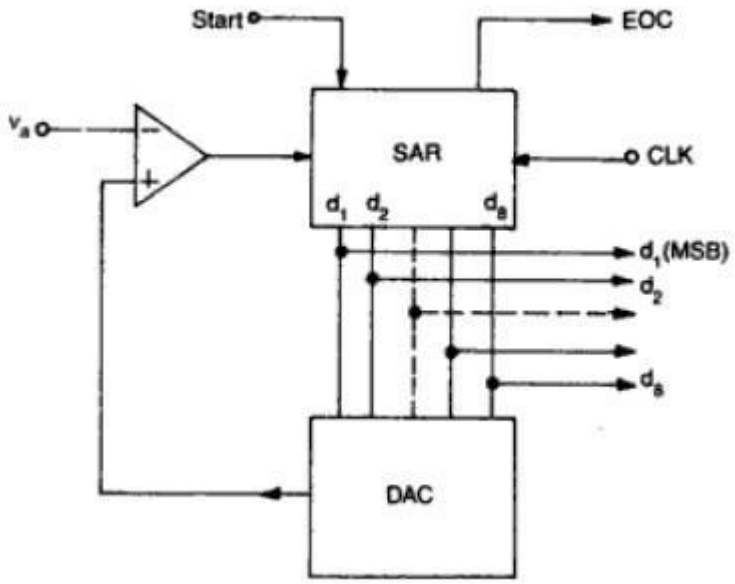
Successive-approximation ADC is a conversion technique based on a successiveapproximation register (SAR). This is also called bit-weighing conversion that employs a comparator to weigh the applied input voltage against the output of an N-bit digital-to-analog converter (DAC).

The final result is obtained as a sum of N weighting steps, in which each step is a single-bit conversion using the DAC output as a reference. SAR converters sample at rates up to 1Mbps, requires a low supply current, and the cheapest in terms of production cost.

A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter (DAC, fed by the current value of the approximation) until the best approximation is achieved.

At each step in this process, a binary value of the approximation is stored in a successive approximation

register (SAR). The SAR uses a reference voltage (which is the largest signal the ADC is to convert) for comparisons.

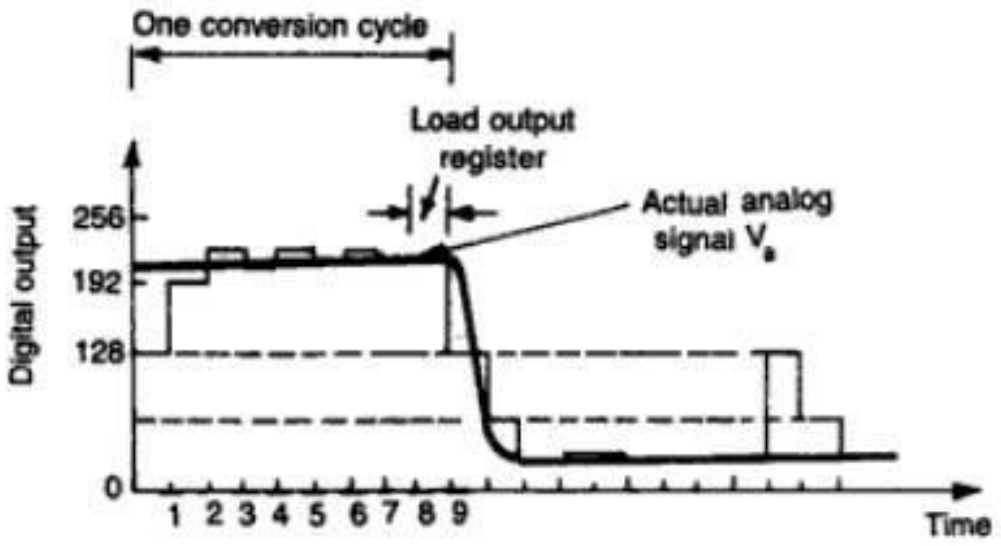


The analogue value is rounded to the nearest binary value below, meaning this converter type is mid-rise (see above). Because the approximations are successive (not simultaneous), the conversion takes one clock-cycle for each bit of resolution desired.

The clock frequency must be equal to the sampling frequency multiplied by the number of bits of resolution desired. For example, to sample audio at 44.1 kHz with 32 bit resolution, a clock frequency of over 1.4 MHz would be required.

ADCs of this type have good resolutions and quite wide ranges. They are more complex than some other designs.

Correct digital representation	*Successive approximation register output V_d at different stages in the conversion*	*Comparator output*
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	



Dual slope ADC (Integrating ADCs)

Explain dual slope ADC with neat circuit diagram. (May 2016)

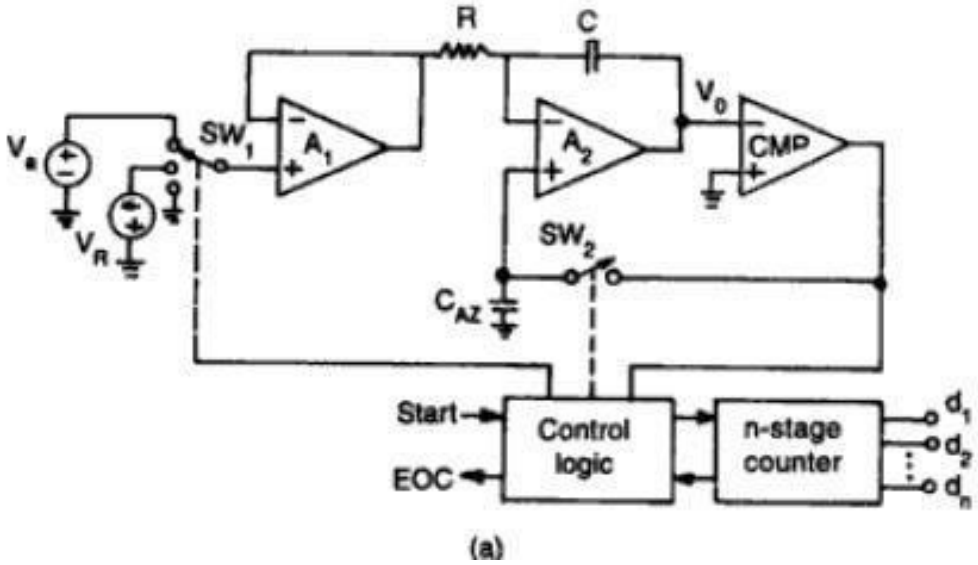
In an integrating ADC, a current, proportional to the input voltage, charges a capacitor for a fixed time interval T charge. At the end of this interval, the device resets its counter and applies an opposite-polarity negative reference voltage to the integrator input. Because of this, the capacitor is discharged by a constant current until the integrator output voltage zero again.

The T discharge interval is proportional to the input voltage level and the resultant final count provides the digital output, corresponding to the input signal. This type of ADCs is extremely slow devices with low input bandwidths. Their advantage, however, is their ability to reject high-frequency noise and AC line noise such as 50Hz or 60Hz. This makes them useful in noisy industrial environments and typical application is in multi-meters.

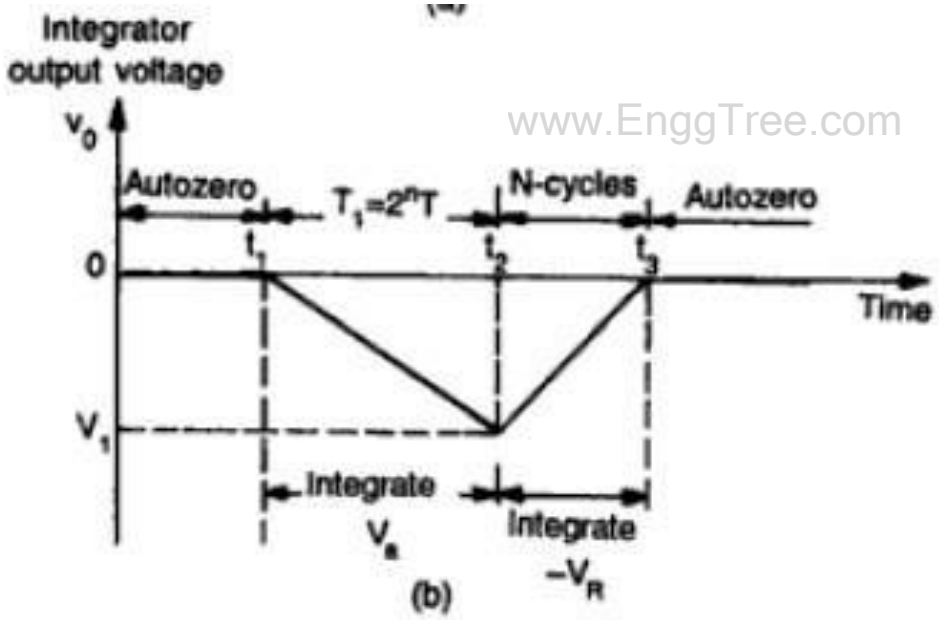
An integrating ADC (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period).

The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution.

Use: Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.



(a)



(b)

A/D Using Voltage to Time Conversion

Explain voltage to time conversion based ADC with neat circuit diagram.

The Block diagram shows the basic voltage to time conversion type of A to D converter. Here the cycles of variable frequency source are counted for a fixed period. It is possible to make an A/D converter by

counting the cycles of a fixed-frequency source for a variable period. For this, the analog voltage required to be converted to a proportional time period.

As shown in the diagram a negative reference voltage -VR is applied to an integrator, whose output is connected to the inverting input of the comparator. The output of the comparator is at 1 as long as the output of the integrator Vo is less than Va.

At t = T, Vc goes low and switch S remains open. When VEN goes high, the switch S is closed, thereby discharging the capacitor. Also the NAND gate is disabled. The waveforms are shown here.

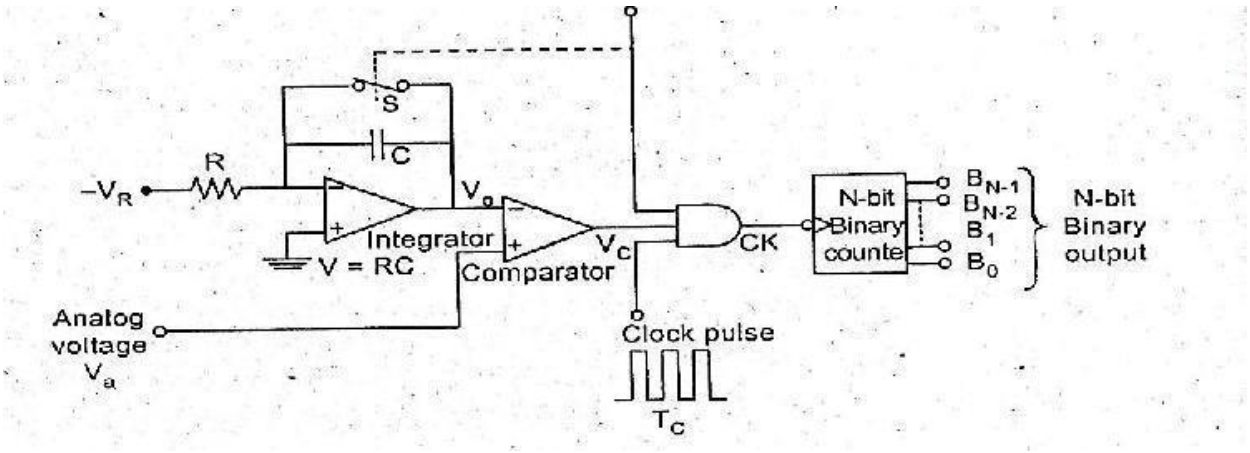


Fig. 4.16 A/D Using Voltage To Time Conversion

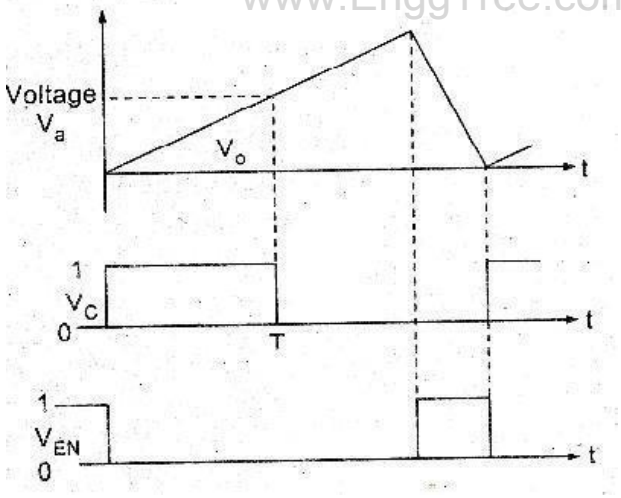


Fig.4.17 Conversion process

Sigma-delta ADCs / Over sampling Converters

Explain over sampling ADC. (May 2016) Discuss the sigma-delta converters.[Nov/Dec 2022]

It consists of 2 main parts - modulator and digital filter. The modulator includes an integrator and a comparator with a feedback loop that contains a 1-bit DAC. The modulator oversamples the input signal,

converting it to a serial bit stream with a frequency much higher than the required sampling rate. This is then transformed by the output filter to a sequence of parallel digital words at the sampling rate. The characteristics of sigma-delta converters are high resolution, high accuracy, Low noise and low cost.

Typical applications are for speech and audio.

A **Sigma-Delta ADC** (also known as a Delta-Sigma ADC) oversamples the desired signal by a large factor and filters the desired signal band. Generally a smaller number of bits than required are converted using a Flash ADC after the Filter.

The resulting signal, along with the error generated by the discrete levels of the Flash, is fed back and subtracted from the input to the filter. This negative feedback has the effect of noise shaping the error due to the Flash so that it does not appear in the desired signal frequencies.

A digital filter (decimation filter) follows the ADC which reduces the sampling rate, filters off unwanted noise signal and increases the resolution of the output. (sigma-delta modulation, also called delta-sigma modulation).

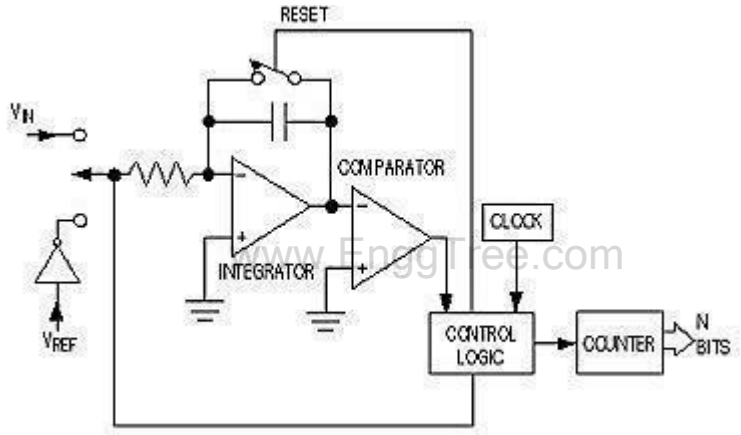


Fig . Sigma-delta ADCs/ Over sampling Converters.

Two Marks

1. What are the types of ADC and DAC. Types of ADC:

1. Flash (comparator) type converter , 2. Counter type converter , 3. Tracking or servo converter

4. Successive approximation type converter

Types of DAC:

1. Weighted resistor DAC , 2. R-2R Ladder , 3. Inverted R-2R Ladder

2. What is the difference between direct ADC and integrating type ADC.

a) The integrating type of ADC's do not need a sample/Hold circuit at the input.

b) It is possible to transmit frequency even in noisy environment or in an isolated form.

3. Define Resolution.

The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter.

Resolution (in volts)= VFS/2n-1=1 LSB increment. The resolution of an ADC is defined as the smallest change in analog input for a one bit change at the output.

4. Define Accuracy.

Absolute accuracy:

It is the maximum deviation between the actual converter output & the ideal converter output.

Relative accuracy:

It is the maximum deviation after gain & offset errors have been removed.

The accuracy of a converter is also specified in form of LSB increments or % of full scale voltage.

5. Define Monotonicity .

A monotonic DAC is one whose analog output increases for an increase in digital input.

6. Define Conversion time.

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used & the propagation delay of circuit components.

The conversion time of a successive approximation type ADC is given by

T(n+1) where T---clock period , Tc---conversion time n----no. of bits.

7. Explain the operation of basic sample and hold circuit.

A typical sample and hold circuit stores electric charge in a capacitor and contains at least one fast FET switch and at least one operational amplifier. To sample the input signal the switch connects the capacitor to the output of a buffer amplifier. The capacitor is invariably discharged by its own leakage currents and useful load currents, which makes the circuit inherently volatile, but the loss of voltage (*voltage droop*) within a specified

hold time remains within an acceptable error margin.

8. State the advantages and applications of sample and hold circuits.

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

9. List the drawbacks of binary weighted resistor technique of D/A conversion.

a) Wide range of resistor values needed

b) Difficulty in achieving and maintaining accurate ratios over a wide range of variations

10. What is the advantage and disadvantages of flash type ADC?

Flash type ADC is the fastest as well as the most expensive.

The disadvantage is the number of comparators needed almost doubles for each added bit (For a n-bit convertor 2(n-1) comparators, 2n resistors are required).

11. Find the resolution of a 12 bit DAC converter.

Resolution (volts) = VFS/(212-1) = I LSB increment

VFS – Full scale voltage

12. What are the advantages and disadvantages of R-2R ladder DAC.

Advantages:

a) Easier to build accurately as only two precision metal films are required.

b) Number of bits can be expanded by adding more sections of same R/2R values.

Disadvantage:

a) In this type of DAC, when there is a change in the input, changes the current flow in the resistor which causes more power dissipation which creates non-linearity in DAC.

13. **efine start of conversion and end of conversion.**

Start of Conversion in ADC (SOC): This is the control signal for start of conversion which initiates A/D conversion process.

End of Conversion in ADC (EOC): This is the control signal which is activated when the conversion is completed.

14. **What is integrating type converter?**

An ADC converter that perform conversion in an indirect manner by firstchanging the analog I/P signal to a linear function of time or frequency and then to adigital code is known as integrating type A/D converter.

15.Explain in brief the principle of operation of successive Approximation ADC.

The circuit of successive approximation ADC consists of a successive approximation register (SAR), to find the required value of each bit by trial & error. With the arrival of START command, SAR sets the MSB bit to

1. The O/P is converted into an analog signal & it is compared with I/P signal. This O/P is low or high. This process continues until all bits are checked.

16.**What are the main advantages of integrating type ADCs?**

- ✓ The integrating type of ADC's do not need a sample/Hold circuit at the input.
- ✓ It is possible to transmit frequency even in noisy environment or in an isolated form.

17.**Where are the successive approximation type ADC used?**

The Successive approximation ADCs are used in applications such as data loggers & instrumentation where conversion speed is important.

18.**What is the main drawback of a dual-slop ADC?**

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC.

19.**State the advantages of dual slope ADC**

It provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T.

20.**What is multiplying DAC?**

A digital to analog converter which uses a varying reference voltage VR is called a multiplying DAC(MDAC). If the reference voltage of a DAC, VR is a sine wave give by V(t)=Vin Cos 2f t

Then, Vo(t)=Vo m Cos(2 ft + 180º)

21.**What is a sample and hold circuit? Where it is used?**

A sample and hold circuit is one which samples an input signal and holds onto its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

22.**Define sample period and hold period.**

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period. The time period during which the voltage across the capacitor is held constant is called hold period.

23.**What is meant by delta modulation?**

Delta modulation is a technique capable of performing analog signal quantization with smaller bandwidth requirements. Here, the binary output representing the most recent sampled amplitude will be determined on the basis of previous sampled amplitude levels.

• • •

24. **Define sampling.**

Convert analog signal into digital signal is known as sampling.

25. **Write the names of the switches used in MOS transistors.**

The names of the switches used in MOS transistors.

CMOS Inverter switch

Totem pole MOSFET switch

26. **Give the resolution of an 8-bit ADC of by input voltage? [Nov/Dec2021]**

Resolution can also be defined as the ratio of change in the value of input voltage Vi, needed to change the digital output by 1 LSB. It is given as

Resolution = ViFS / $(2^n - 1)$

Where 'ViFS' is the full-scale input voltage.

'n' is the number of output bits.

27. **What output voltage would be produced by a D/A converter whose output range is 0 to 10V and whose input binary number is 10111100 (for a 8 bit DAC)? [Nov/Dec 2021]**

Output voltage = Resolution * binary number

Resolution R = V_{FS} / $(2^n - 1)$

= 10/ $(2^8 - 1)$

= 10/255

= 0.039

Output voltage = 0.03 * 10111100

=0.039 * 188

= 7.37 V

28. State applications of ADCs.[Nov/Dec 2022]

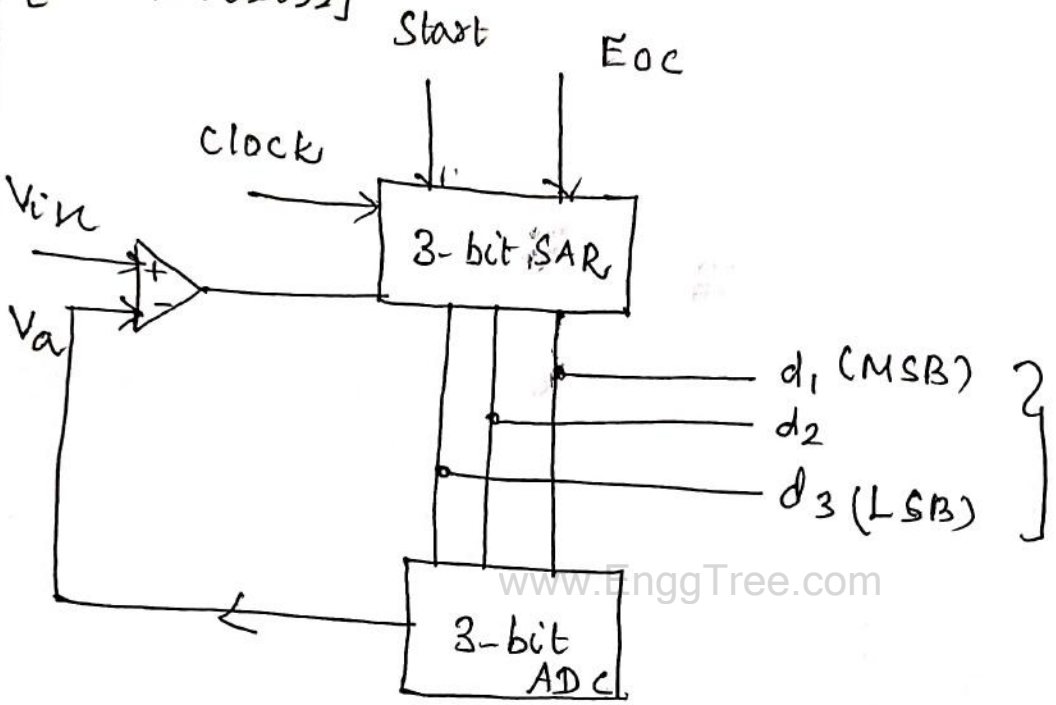
1. Digtal Signal Processing.
2. Audio processing
3. Scientific Instruments
4. Micro controllers.

UNIT-4

PART B

1) Design a 3-bit SAR type ADC with $V_{in} = 6.5V$. Tabulate the conversion process to show digital output?

[NOV|DEC 2022]



100
010
010
001

Vin > Va

100
010
010

UNIT V

WAVEFORM GENERATORS AND SPRCIAL FUNCTION ICs

Sine-wave generators, Multivibrators and Triangular wave generator, Saw-tooth wave generator, ICL8038 function generator, Timer IC 555, IC Voltage regulators – Three terminal fixed and adjustable voltage regulators - IC 723 general purpose regulator - Monolithic switching regulator, Switched capacitor filter IC MF10, Frequency to Voltage and Voltage to Frequency converters, Audio Power amplifier, Video Amplifier, Isolation Amplifier, Opto-couplers and fibre optic IC.

Basics of oscillators: Criteria for oscillation:

The canonical form of a feedback system is shown in Figure 5 . 1, and Equation 1 describes the performance of any feedback system (an amplifier with passive feedback Components constitute a feedback system).

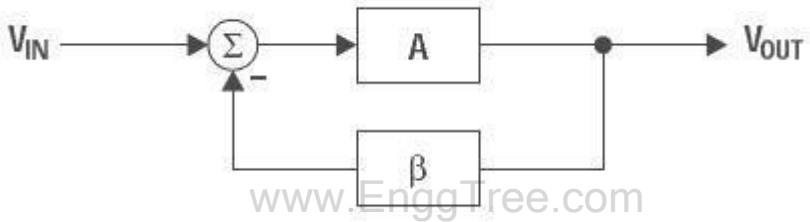


Fig. 5.1 Canonical form of feedback circuit

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta}$$

Oscillation results from an unstable state; i.e., the feedback system can't find a stable state because is an undefined state. Thus, the key to designing an oscillator is to insure that $A\beta = -1$ (called the Barkhausen criterion), or using complex math the equivalent expression is $A\beta = 1 \angle -180°$.

The 180° phase shift criterion applies to negative feedback systems, and 0° phase shift applies to positive feedback systems.

The output voltage of a feedback system heads for infinite voltage when $A\beta = -1$. When the output voltage approaches either power rail, the active devices in the amplifiers change gain, causing the value of A to change so the value of $A\beta \neq 1$; thus, the charge to infinite voltage slows down and eventually halts. At this point one of three things can occur.

First, nonlinearity in saturation or cutoff can cause the system to become stable and lock up.

Second, the initial charge can cause the system to saturate (or cut off) and stay that way for a long time before it becomes linear and heads for the opposite power rail.

Third, the system stays linear and reverses direction, heading for the opposite power rail.

Alternative two produces highly distorted oscillations (usually quasi square waves), and the resulting oscillators are called relaxation oscillators. Alternative three produces sine wave oscillators.

Sine Wave Generators (Oscillators)

Explain sine wave oscillators using op-amp.

Sine wave oscillator circuits use phase shifting techniques that usually employ

- ✓ Two RC tuning networks, and
- ✓ Complex amplitude limiting circuitry

RC Phase Shift Oscillator:

Q. Explain the circuit of a RC phase shift oscillator. [Nov/Dec 2021]

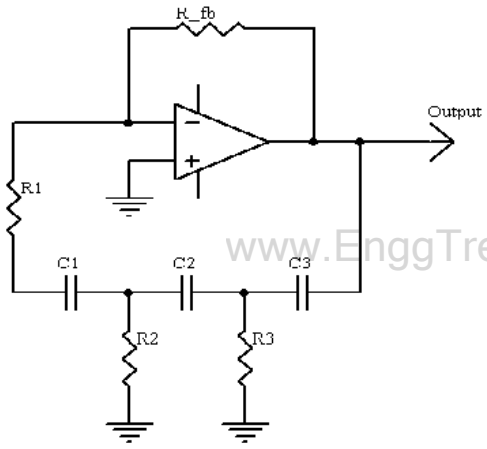


Fig.5.3 RC Phase shift oscillator

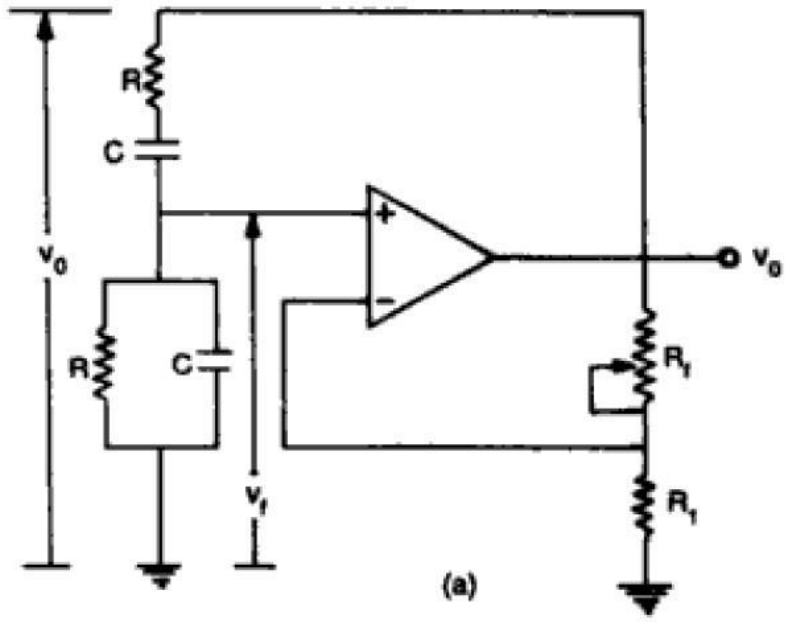
RC phase shift oscillator using op-amp in inverting amplifier introduces the phase shift of 180^0 between input and output. The feedback network consists of 3 RC sections each producing 60^0 phase shift. Such a RC phase shift oscillator using op-amp is shown in the figure.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180^0 of amplifier and 180^0 due to 3 RC sections, thus 360^0 . This satisfies the required condition for positive feedback and circuit works as an oscillator.

Frequency of oscillation $f=1/2\pi RC\sqrt{6}$

Wien Bridge Oscillator Q. Explain the operation of a Wein bridge oscillator with neat sketches.[Nov/Dec 2022]

Figure give the Wien-bridge circuit configuration. The loop is broken at the positive input.



When ω = 2πf = 1/RC, the feedback is in phase (this is positive feedback), and the gain is 1/3, so oscillation requires an amplifier with a gain of 3. When RF = 2RG, the amplifier gain is 3 and oscillation occurs at f = 1/2πRC. The circuit oscillated at 1.65 kHz rather than 1.59 kHz with the component values shown in Figure , but the distortion is noticeable.

If a resistor is placed in parallel with the amplifier input, it will cancel some of the negative resistance. If the net resistance is negative, amplitude will grow until clipping occurs.

Similarly, if the net resistance is positive, oscillation amplitude will decay. If a resistance is added in parallel with exactly the value of *R*, the net resistance will be infinite and the circuit can sustain stable oscillation at any amplitude allowed by the amplifier.

Increasing the gain makes the net resistance more negative, which increases amplitude. If gain is reduced to exactly 3 when suitable amplitude is reached, stable, low distortion oscillations will result.

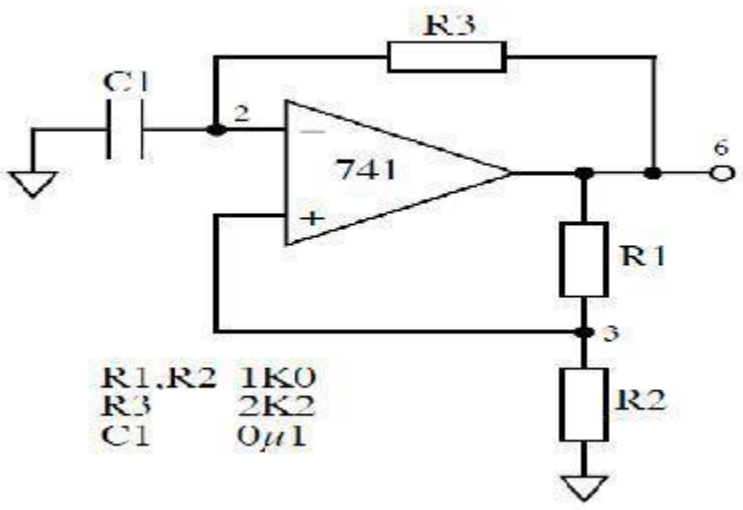
Amplitude stabilization circuits typically increase gain until suitable output amplitude is reached. As long as *R*, *C*, and the amplifier are linear, distortion will be minimal.

Multivibrator

Astable Multivibrator

Explain astable multivibrator using op-amp. (May 2014)

The two states of circuit are only stable for a limited time and the circuit switches between them with the output alternating between positive and negative saturation values.



Analysis of this circuit starts with the assumption that at time t=0 the output has just switched to state 1, and the transition would have occurred.

An op-amp Astable multivibrator is also called as free running oscillator. The basic principle of generation of square wave is to force an op-amp to operate in the saturation region (±Vsat).

A fraction β =R2/(R1+R2) of the output is feedback to the positive input terminal of op-amp. The charge in the capacitor increases & decreases upto a threshold value called ±βVsat.

The charge in the capacitor triggers the op-amp to stay either at +Vsat or –Vsat.

Asymmetrical square wave can also be generated with the help of Zener diodes. Astable multi vibrator do not require a external trigger pulse for its operation & output toggles from one state to another and does not contain a stable state.

Astable multivibrator is mainly used in timing applications & waveforms generators.

Design

1. The expression of fo is obtained from the charging period t1 & t2 of capacitor as

T=2RC ln (R1+2R2)/R1

2. To simplify the above expression, the value of R1 & R2 should be taken as R2 = 1.16R

Such that fo simplifies to fo =1/2RC.

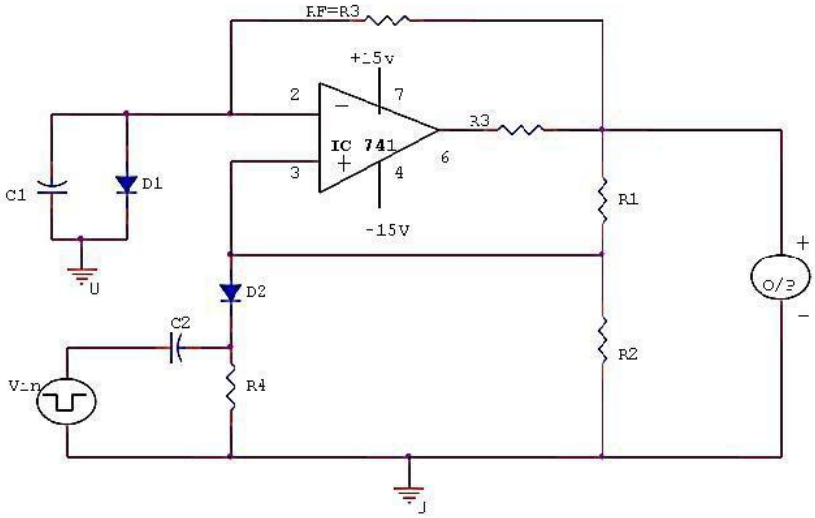
3. Assume the value of R1 and find R2.

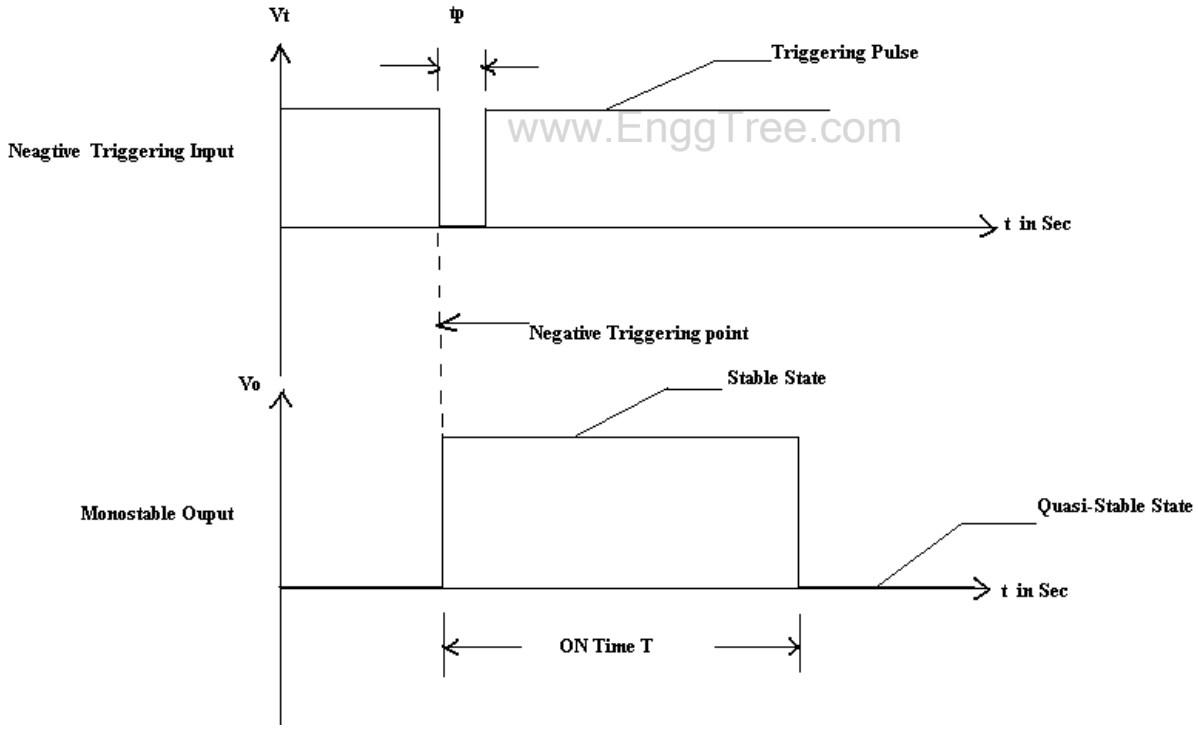
4. Assume the value of C & Determine R from fo =1/2R C

5. Calculate the threshold point from βV_{SAT}.

Monostable Multivibrator using Op-amp

Explain with neat diagram the monostable multivibrator using op-amp. (Dec 2015)





A multivibrator which has only one stable and the other is quasi stable state is called as Monostable multivibrator or one-short multivibrator. This circuit is useful for generating signal output pulse of adjustable time duration in response to a triggering signal.

The width of the output pulse depends only on the external components connected to the opamp. Usually a negative trigger pulse is given to make the output switch to other state. But, it then return to its stable state after a time interval determining by circuit components.

The pulse width T can be given as T = 0.69RC. For Monostable operation the triggering pulse width Tp should be less then T, the pulse width of Monostable multivibrator. This circuit is also called as time delay circuit or gating circuit.

Design:

1. Calculating β from expression

$$\beta = \frac{R1}{R1 + R2}$$

2. The value of R & C from the pulse width time expression.

$$T = RC \ln \frac{(1 + V_D / V_{sat})}{1 - \beta}$$

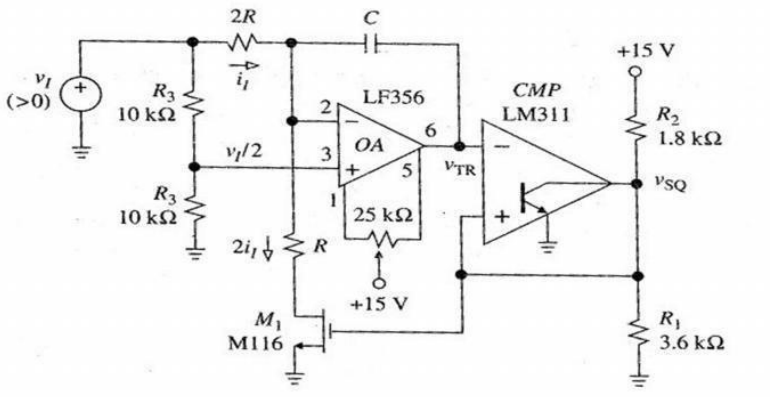
$$T = RC \ln \frac{(1 + V_D / V_{sat})}{0.5}$$

$$T \equiv 0.69RC.$$

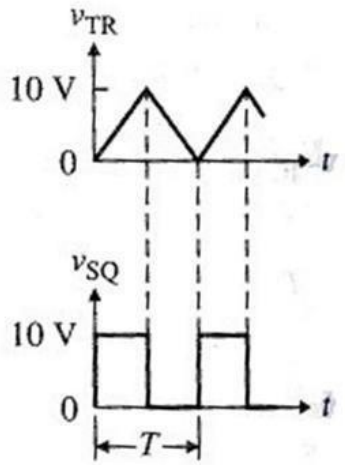
3. Triggering pulse width T_p must be much smaller then T. $T_p < T$.

Triangular Wave Generator Circuit

Explain triangular wave generator with neat diagram.

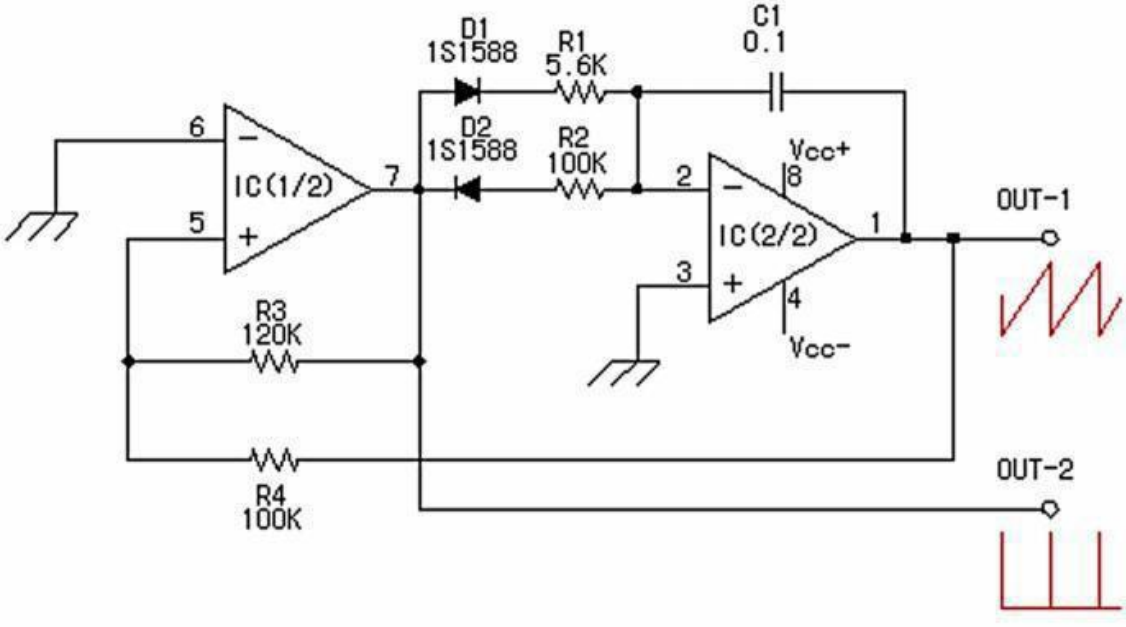


This signal generator gives two waveforms: a triangle-wave and a square- wave. The central component of this circuit is the integrator capacitor CI. Basically we are interested in performing two functions on CI: *charge it, discharge it - repeat indefinitely.* The output waveforms are shown here and it is apparent that a square wave generator followed by an integrator acts as a triangular wave generator.



Saw-Tooth Wave Generator

Explain sawtooth wave generator with neat diagram.



The saw tooth wave oscillator which used the operational amplifier. The composition of this circuit is the same as the triangular wave oscillator basically and is using two operational amplifiers.

At the circuit diagram above, IC(1/2) is the Schmitt circuit and IC(2/2) is the Integration circuit. The difference with the triangular wave oscillator is to be changing the time of the charging and the discharging of the capacitor. When the output of IC (1/2) is positive voltage, it charges rapidly by the small resistance (R1) value. (When the integration output voltage falls) When the output of IC(1/2) is negative voltage, it is made to charge gradually at the big resistance(R2) value.

The output waveform of the integration circuit becomes a form like the tooth of the saw. Such voltage is used for the control of the electron beam (the scanning line) of the television, When picturing a picture at the cathode-ray tube, an electron beam is moved comparative slow. (When the electron beam moves from the left to the right on the screen). When turning back, it is rapidly moved.(When moving from the right to the left).

Like the triangular wave oscillator, the line voltage needs both of the positive power supply and the negative power supply. Also, to work in the oscillation, the condition of R3>R4 is necessary.

However, when making the value of R4 small compared with R3, the output voltage becomes small. The near value is good for R3 and R4 The oscillation frequency can be calculated by the following formula. With the circuit diagram,the oscillation frequency is as follows.

f = (1/2C (R1+R2))*(R3/R4)

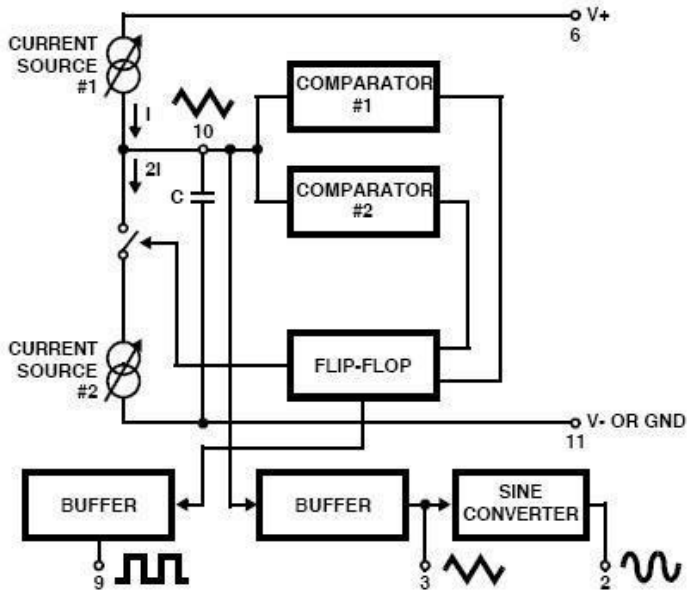
= (1/(2x0.1x10-6x(5.6x103+100x103))x(120x103/100x103)

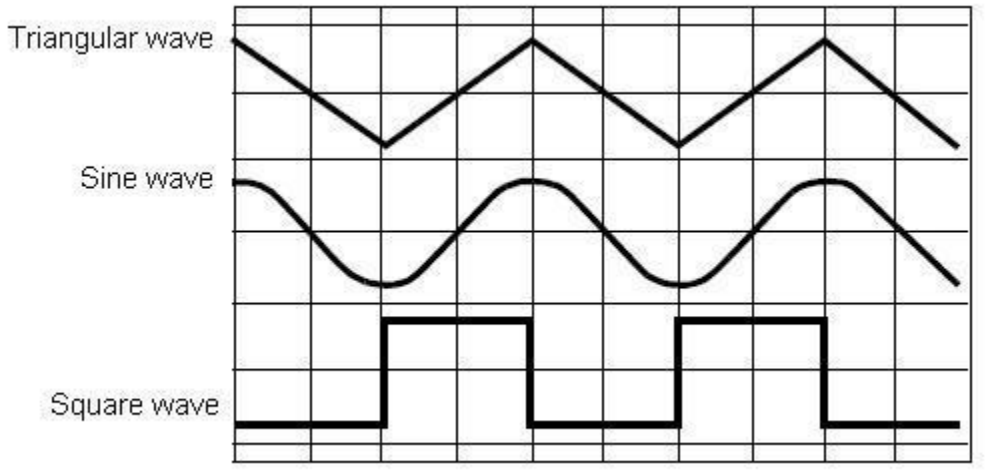
= (1/(21.12x10-3))x1.2

= 56.8 Hz

Function Generator IC 8038

Explain with block diagram the function generator IC 8038.





It consists of two current sources, two comparators, two buffers, one FF and a sine wave converter.

Pin description:

 Pin 1 & Pin 12: Sine wave adjusts: The distortion in the sine wave output can be reduced by adjusting the 100KΩ pots connected between pin12 & pin11 and between pin 1 & 6.

 Pin 2 Sine Wave Output: Sine wave output is available at this pin. The amplitude of this sine wave is 0.22 Vcc. Where ± 5V ≤ Vcc ≤ ± 15 V.

 Pin 3 Triangular Wave output: Triangular wave is available at this pin. The amplitude of the triangular wave is 0.33Vcc. Where ± 5V ≤ Vcc ≤ ± 15 V.

 Pin 4 & Pin 5 Duty cycle / Frequency adjust: The symmetry of all the output wave forms & 50% duty cycle for the square wave output is adjusted by the external resistors connected from Vcc to pin 4. These external resistors & capacitors at pin 10 will decide the frequency of the output wave forms.

 Pin 6 + Vcc: Positive supply voltage the value of which is between 10 & 30V is applied to this pin.

 Pin 7 : FM Bias: This pin along with pin no8 is used to TEST the IC 8038.

 Pin9 : Square Wave Output: A square wave output is available at this pin. It is an open collector output so that this pin can be connected through the load to different power supply voltages. This arrangement is very useful in making the square wave output.

 Pin 10 : Timing Capacitors: The external capacitor C connected to this pin will decide the output frequency along with the resistors connected to pin 4 & 5.

 Pin 11 : -VEE or Ground: If a single polarity supply is to be used then this pin is connected to supply ground & if (±) supply voltages are to be used then (-) supply is connected to this pin.

 Pin 13 & Pin 14: NC (No Connection)

Important features of IC 8038:

1. All the outputs are simultaneously available.
2. Frequency range : 0.001Hz to 500kHz
3. Low distortion in the output wave forms.
4. Low frequency drifts due to change in temperature.
5. Easy to use.

Parameters:

(i) Frequency of the output wave form: The output frequency dependent on the values of resistors R1 & R2 along with the external capacitor C connected at pin 10.

If RA= RB = R & if RC is adjusted for 50% duty cycle then f0= 0.3/RC; RA = R1, RB = R3, RC= R2.

(ii) Duty cycle / Frequency Adjust : (Pin 4 & 5): Duty cycle as well as the frequency of the output wave form can be adjusted by external resistors at pin 4 & 5.

The values of resistors RA & RB connected between Vcc pin 4 & 5 respectively along with the capacitor connected at pin 10 decide the frequency of the wave form. The values of RA & RB should be in the range of 1kΩ to 1MΩ.

(iii)FM Bias:

- The FM Bias input (pin7) corresponds to the junction of resistors R1 & R2.
- The voltage Vin is the voltage between Vcc & pin8 and it decides the output frequency.
- The output frequency is proportional to Vin as given by the following expression.

For RA = RB (50% duty cycle).

- f0= 5 Vin/CRAVcc ; where C is the timing capacitor.
- With pin 7 & 8 connected to each other the output frequency is given by f0= 0.3/RC where R = RA = RB for 50% duty cycle.
- This is because M Sweep input (pin 8):
- Vin=R1Vcc/R1+R2
- This input should be connected to pin 7, if we want a constant output frequency.
- But if the output frequency is supposed to vary, then a variable dc voltage should be applied to this pin.
- The voltage between Vcc & pin 8 is called Vin and it decides the output frequency as, f0=1.5 Vin/CRAVCC

A potentiometer can be connected to this pin to obtain the required variable voltage required to change the output frequency.

The 555 Timer IC

Explain the basic functions of 555 timer IC.

The 555 is a monolithic timing circuit that can produce accurate & highly stable time delays or oscillation. The timer basically operates in one of two modes: either

(i) Monostable (one - shot) multivibrator or

(ii) Astable (free running) multivibrator

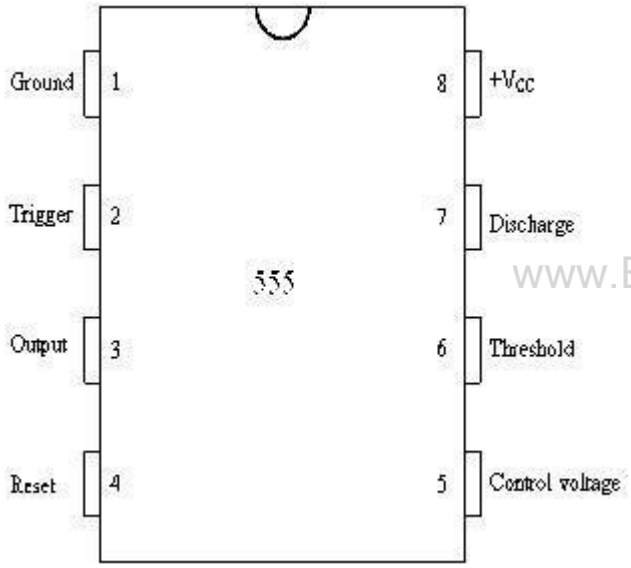
The important features of the 555 timer are these:

(i) It operates on +5v to +18 v supply voltages

(ii) It has an adjustable duty cycle

(iii) Timing is from microseconds to hours

(iv) It has a current o/p



Pin description:

Pin 1: Ground**:** All voltages are measured with respect to this terminal.

Pin 2: Trigger: The o/p of the timer depends on the amplitude of the external trigger pulse applied to this pin.

Pin 3: Output: There are 2 ways a load can be connected to the o/p terminal either between pin3 & ground or between pin 3 & supply voltage (Between Pin 3 & Ground ON load) (Between Pin 3 & + Vcc OFF load)

(i) When the input is low: The load current flows through the load connected between Pin 3 & +Vcc in to the output terminal & is called the sink current.

(ii) When the output is high: The current through the load connected between Pin 3 & +Vcc (i.e. ON load) is zero. However the output terminal supplies current to the normally OFF load. This current is called the source current.

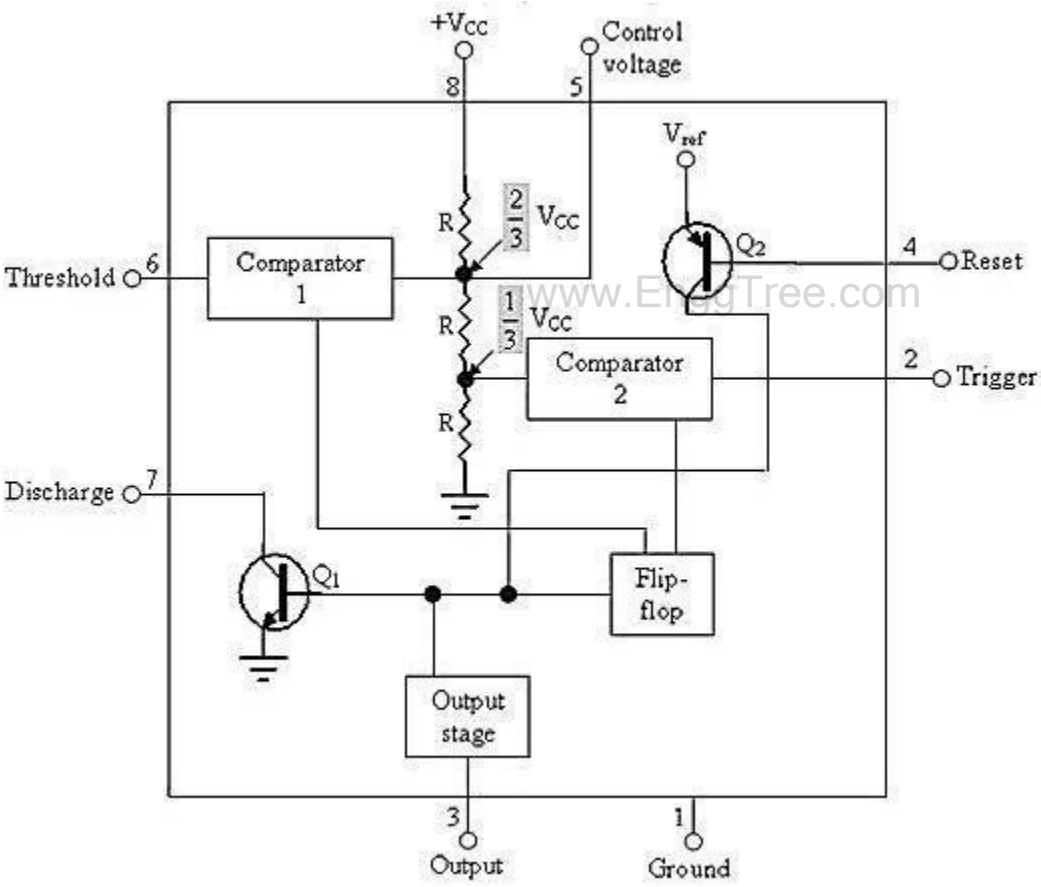
Pin 4: Reset: The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to +Vcc to avoid any false triggering.

Pin 5: Control voltage: An external voltage applied to this terminal changes the threshold as well as trigger voltage. In other words by connecting a potentiometer between this pin & GND, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with 0.01 capacitor to prevent any noise problems.

Pin 6: Threshold: This is the non inverting input terminal of upper comparator which monitors the voltage across the external capacitor.

Pin 7: Discharge: This pin is connected internally to the collector of transistor Q1. When the output is high Q1 is OFF. When the output is low Q is (saturated) ON.

Pin 8: +Vcc: The supply voltage of +5V to +18V is applied to this pin with respect to ground.



From the above figure, three 5k internal resistors act as voltage divider providing bias voltage of 2/3 Vcc to the upper comparator & 1/3 Vcc to the lower comparator. It is possible to vary time electronically by applying a modulation voltage to the control voltage input terminal (5).

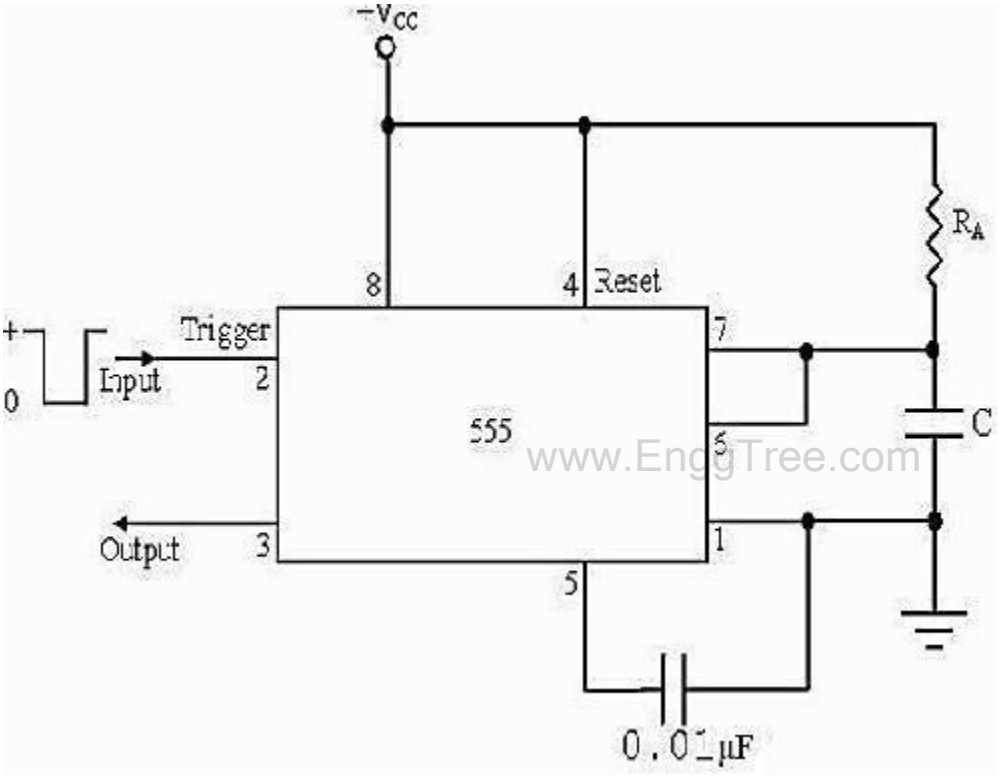
(i) In the Stable state: The output of the control FF is high. This means that the output is low because of power amplifier which is basically an inverter. Q = 1; Output = 0

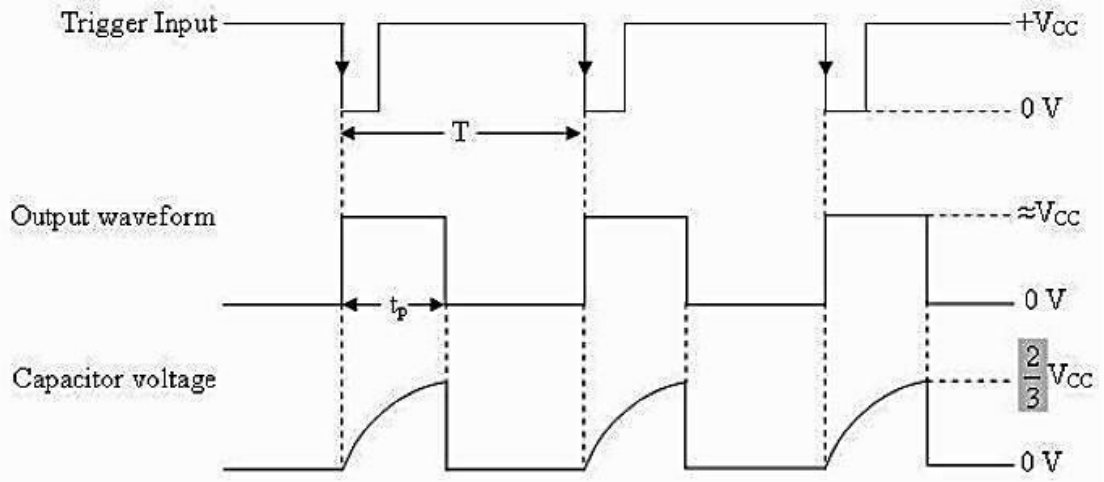
(ii) At the Negative going trigger pulse: The trigger passes through (Vcc/3) the output of the lower comparator goes high & sets the FF. Q = 1; Q = 0

(iii) At the Positive going trigger pulse: It passes through 2/3Vcc, the output of the upper comparator goes high and resets the FF. Q = 0; Q = 1 The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator.

Monostable Operation

Explain the monostable operation of 555 timer.





Initially when the output is low, i.e. the circuit is in a stable state, transistor Q1 is ON & capacitor C is shorted to ground. The output remains low. During negative going trigger pulse, transistor Q1 is OFF, which releases the short circuit across the external capacitor C & drives the output high. Now the capacitor C starts charging toward Vcc through RA.

When the voltage across the capacitor equals 2/3 Vcc, upper comparator switches from low to high. i.e. Q = 0, the transistor Q1 = OFF ; the output is high. Since C is unclamped, voltage across it rises exponentially through R towards Vcc with a time constant RC (fig b) as shown in below. After the time period, the upper comparator resets the FF, i.e. Q = 1, Q1 = ON; the output is low.[i.e discharging the capacitor C to ground potential (fig c)]. The voltage across the capacitor as in fig (b) is given by

$V_c = V_{cc}(1-e^{-t/RC})$ ……. (1)

Therefore At t = T, Vc = 2/3 Vcc

$2/3\ V_{cc} = V_{cc}(1-e^{-T/RC})$

or

$T = RC \ln(1/3)$

Or

$T = 1.1RC$ seconds ……. (2)

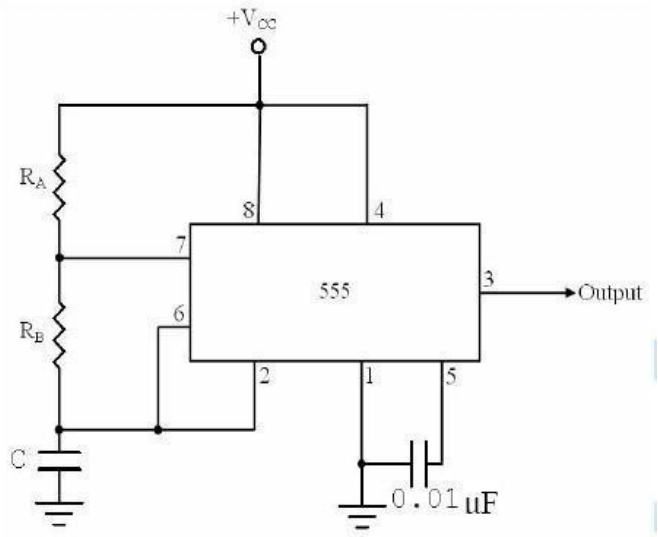
If the reset is applied Q2 = OFF, Q1 = ON, timing capacitor C immediately discharged. The output now will be as in figure (d & e). If the reset is released output will still remain low until a negative going trigger pulse is again applied at pin 2.

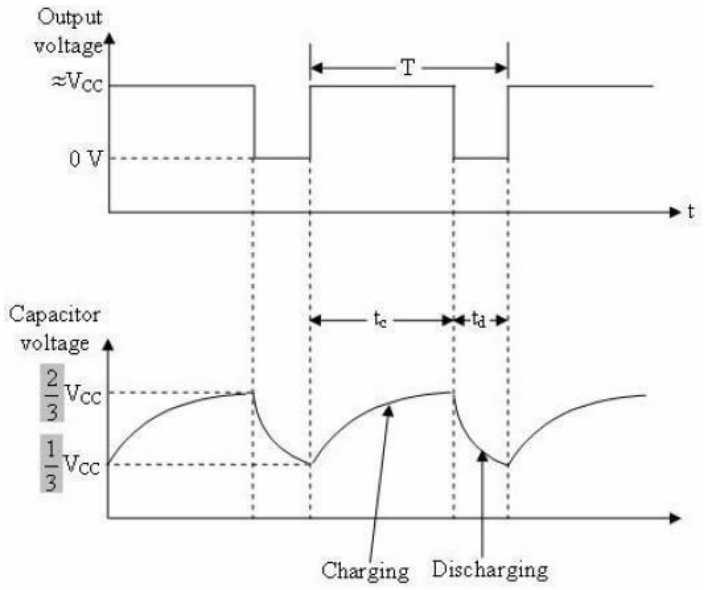
Astable Multivibrator:

Explain the operation of astable multivibrator sing 555 timer.

An Astable multivibrator, often called a free running multivibrator, is a rectangular wave generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name free running.

However, the time during which the output is either high or low is determined by 2 resistors and capacitors, which are externally connected to the 55 timer.





The above figures show the 555 timer connected as an astable multivibrator and its model graph. **Initially, when the output is high** :

Capacitor C starts charging toward Vcc through RA & RB. However, as soon as voltage across the capacitor equals 2/3 Vcc. Upper comparator triggers the FF & output switches low.

When the output becomes Low:

Capacitor C starts discharging through RB and transistor Q1, when the voltage across C equals 1/3 Vcc, lower comparator output triggers the FF & the output goes high. Then cycle repeats. The capacitor is periodically charged & discharged between 2/3 Vcc & 1/3 Vcc respectively. The time during which the capacitor charges from 1/3 Vcc to 2/3 Vcc equal to the time the output is high & is given by

tc = (RA+RB)C ln 2……(1) Where [ln 2 = 0.69]

= 0.69 (RA+RB) C

Where RA & RB are in ohms. And C is in farads.

Similarly, the time during which the capacitors discharges from 2/3 Vcc to 1/3 Vcc is equal to the time, the output is low and is given by,

tc = RB C ln 2

td = 0.69 RB C ……..(2) where RB is in ohms and C is in farads.

Thus the total period of the output waveform is

T = tc + td = 0.69 (RA+2RB) C …….(3)

This, in turn, gives the frequency of oscillation as,f 0 = 1/T = 1.45/(RA+2RB)C ……(4)

Equation 4 indicates that the frequency f 0 is independent of the supply voltage Vcc.

Often the term duty cycle is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time tc during which the output is high to the total time period T.

It is generally expressed as a percentage.

% duty cycle = (tc / T)* 100

% Duty Cycle = [(RA+RB)/ /(RA+2RB)] * 100

Linear Regulators

 All electronic circuits need a dc power supply for their operation. To obtain this dc voltage from 230 V ac mains supply, we need to use rectifier.

 Therefore the filters are used to obtain a "steady" dc voltage from the pulsating one.

 The filtered dc voltage is then applied to a regulator which will try to keep the dc output voltage constant in the event of voltage fluctuations or load variation.

The combination of rectifier & filter can produce a dc voltage. But the problem with this type of dc power supply is that its output voltage will not remain constant in the event of fluctuations in an AC input or changes in the load current(IL).

 The output of unregulated power supply is connected at the input of voltage regulator circuit.

 The voltage regulator is a specially designed circuit to keep the output voltage constant. It does not remain exactly constant. It changes slightly due to changes in certain parameters.

Factors affecting the output voltage:

i) IL (Load Current)

ii) VIN (Input Voltage)

iii) T (Temperature)

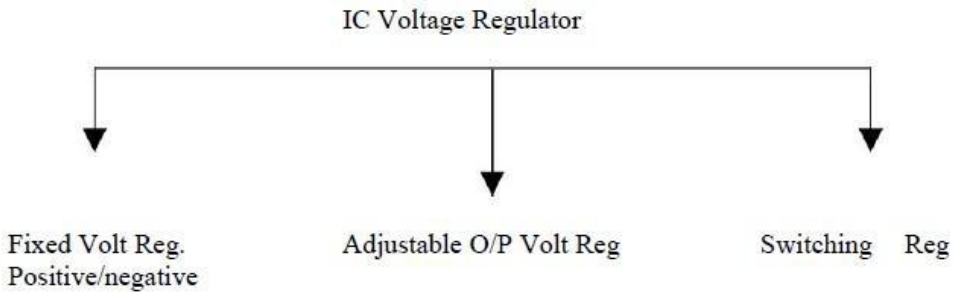
IC Voltage Regulators:

They are basically series regulators.

 Important features of IC Regulators:

1. Programmable output
2. Facility to boost the voltage/current
3. Internally provided short circuit current limiting
4. Thermal shutdown
5. Floating operation to facilitate higher voltage output

 Classifications of IC voltage regulators:



Fixed & Adjustable output Voltage Regulators are known as Linear Regulator. A series pass transistor is used and it operates always in its active region.

Switching Regulator:

1. Series Pass Transistor acts as a switch.
2. The amount of power dissipation in it decreases considerably.
3. Power saving result is higher efficiency compared to that of linear.

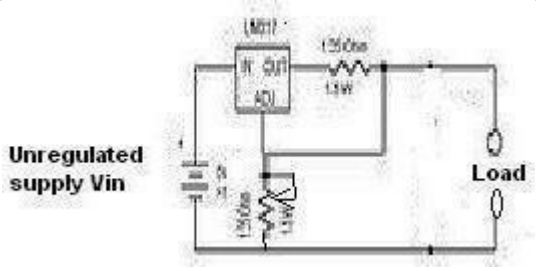
Adjustable Voltage Regulator:

Advantages of Adjustable Voltage Regulator over fixed voltage regulator are,

1. Adjustable output voltage from 1.2v to 57 v
2. Output current 0.10 to 1.5 A
3. Better load & line regulation
4. Improved overload protection
5. Improved reliability under the 100% thermal overloading

Adjustable Positive Voltage Regulator (LM317)

Explain the operation of positive voltage regulator LM317.



LM317 series adjustable 3 terminal positive voltage regulator, the three terminals are Vin, Vout & adjustment (ADJ).

- LM317 requires only 2 external resistors to set the output voltage.
- LM317 produces a voltage of 1.25v between its output & adjustment terminals. This voltage is called as Vref.
- Vref (Reference Voltage) is a constant, hence current I1 flows through R1 will also be constant. Because resistor R1 sets current I1. It is called "current set" or "program resistor".

 Resistor R2 is called as “Output set” resistors, hence current through this resistor is the sum of I1 & Iadj

 LM317 is designed in such as that Iadj is very small & constant with changes in line voltage & load current.

 The output voltage Vo is, Vo=R1I1+(I1+Iadj)R2 ---------- (1)

Where I1= Vref/R1

Vo = (Vref/R1) R1 + Vref/R1 + Iadj R2

= Vref + (Vref/R1) R2 + Iadj R2

Vo = Vref [1 + R2/R1] + Iadj R2 ---------- (2)

R1 = Current (I1) set resistor

R2 = output (Vo) set resistor.

Vref = 1.25v which is a constant voltage between output and ADJ terminals.

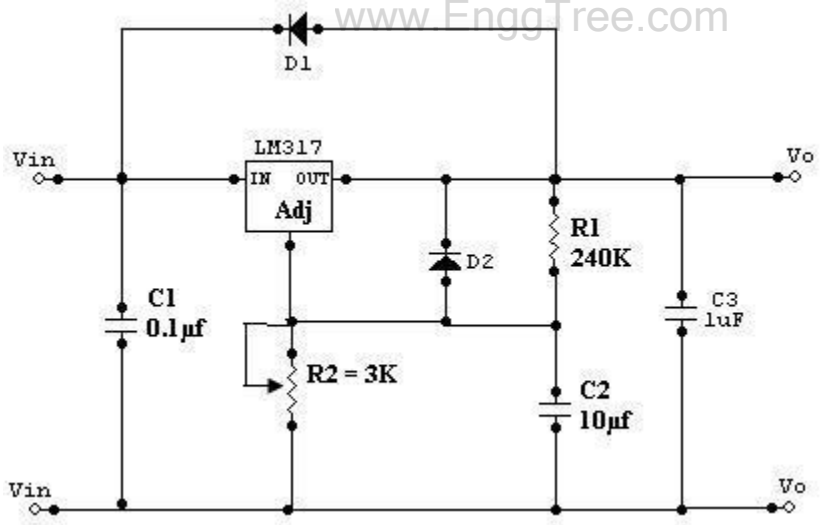
 Current Iadj is very small. Therefore the second term in (2) can be neglected.

 Thus the final expression for the output voltage is given by

Vo= 1.25v[1 + R2/R1] ---------- (3)

Eqn (3) indicates that we can vary the output voltage by varying the resistance R2. The value of R1 is normally kept constant at 240 ohms for all practical applications.

Practical Regulator using LM317



If LM317 is far away from the input power supply, then 0.1µf disc type or 1µf tantalum capacitor should be used at the input of LM317.

 The output capacitor Co is optional. Co should be in the range of 1 to 1000µf.

 The adjustment terminal is bypassed with a capacitor C2 this will improve the ripple rejection ratio as high as 80 dB is obtainable at any output level.

 When the filter capacitor is used, it is necessary to use the protective diodes.

 These diodes do not allow the capacitor C2 to discharge through the low current point of the regulator.

 These diodes are required only for high output voltages (above 25v) & for higher values of output capacitance 25μf and above.

IC 723 – General Purpose Regulator

Explain the basic operations of IC723 general purpose regulator. [Nov/Dec 2022]

 Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit
2. Output voltage is not adjustable

These limitations can be overcomes in IC723.

 Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (ILmax = 150mA).
4. With the additional transistor used, ILmax upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

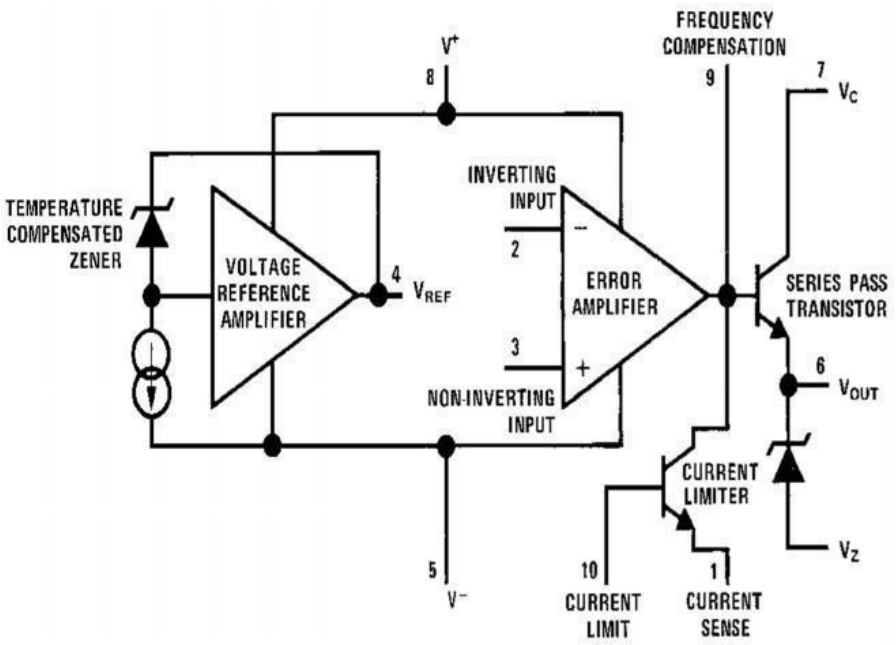
The simplified functional block diagram can be divided in to 4 blocks.

1. Reference Generating block:

The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Noninverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.



NC	1		14	NC
Current limit	2		13	Frequency compensation
Current sense	3		12	+Vcc
Inverting Input	4	IC723	11	Vc
Non-Inverting Input	5		10	Vo
Vref	6		9	Vz
-Vcc	7		8	NC

3. Series Pass Transistor:

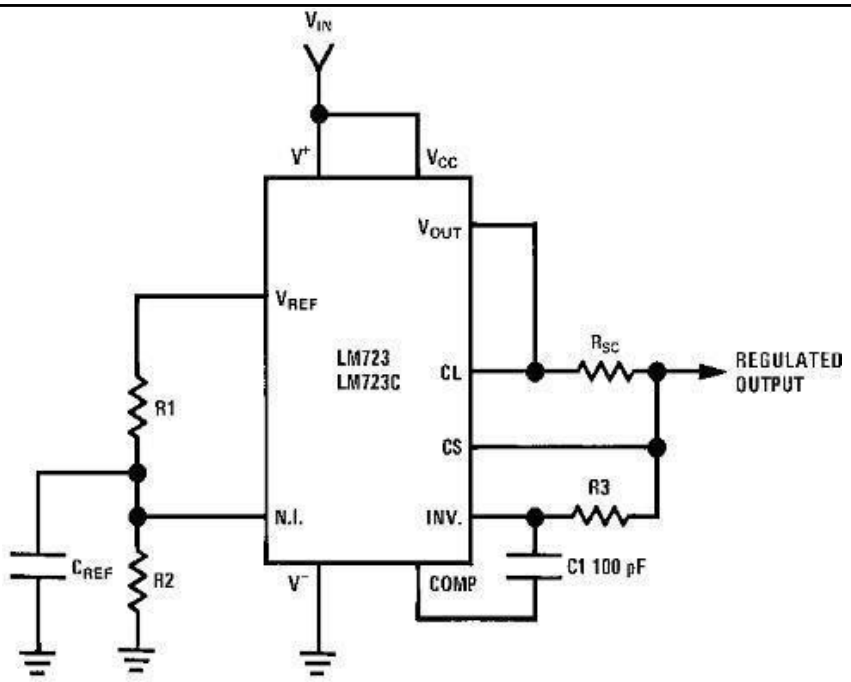
Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the IL exceeds a predetermined limit. Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts. Vload = 2 to 7V and Iload= 50mA

IC723 as a LOW voltage LOW current

Explain with neat circuit diagram, IC723 as low voltage regulator.



 The Voltage across R2 is connected to the Non – inverting terminal of the regulator IC

Vnon-inv = R2/(R1+R2) Vref

 Gain of the internal error amplifier is large Vnon-inv = Vin

 Therefore the Vo is connected to the Inverting terminal through R3 & RSC must also be equal to Vnon-inv

Vo = Vnon-inv =R2/(R1+R2) Vref

R1 & R2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

R3 = R1ll R2 =R1R2/(R1+R2)

Rsc (current sensing resistor) is connected between Cs & CL. The voltage drop across Rsc is proportional to the IL.

 This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.

 The current sourcing capacity is increased by including a transistor Q in the circuit.

 The output voltage , Vo =R2/(R1+R2) Vref

5.7.2 IC723 as a HIGH voltage LOW Current:

This circuit is capable of supplying a regulated output voltage between the ranges of 7 to 37 volts with a maximum load current of 150 mA.

 The Non – inverting terminal is now connected to Vref through resistance R3.

 The value of R1 & R2 is adjusted in order to get a voltage of Vref at the inverting terminal at the desired output.

Vin = Vref =R2 /(R1+R2) V0

Vo = [1+R1/R2] Vin

 Rsc is connected between CL & Cs terminals as before & it provides the short Circuit current limiting

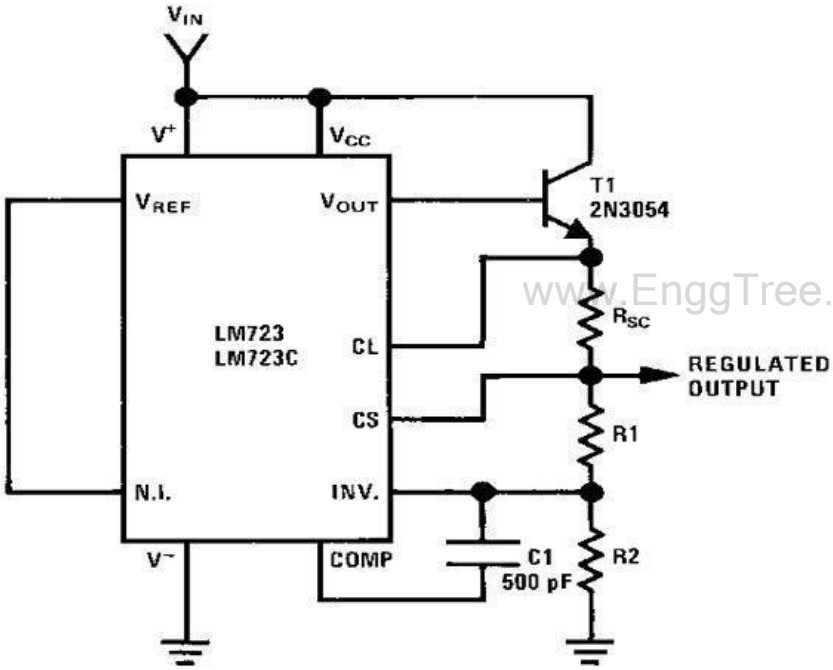
Rsc =0.6/Ilimit

 The value of resistors R3 is given by , R3= R1ll R2 =R1R2/(R1+R2)

IC723 as a HIGH voltage HIGH Current:

Explain with neat diagram IC723 as high voltage regulator.

 An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.



 For this circuit the output voltage varies between 7 & 37V.

 Transistor Q increase the current sourcing capacity thus IL (MAX) is greater than 150mA.

 The output voltage Vo is given by ,

V0= Vo = [1+R1/R2] Vin

Rsc =0.6/Ilimit

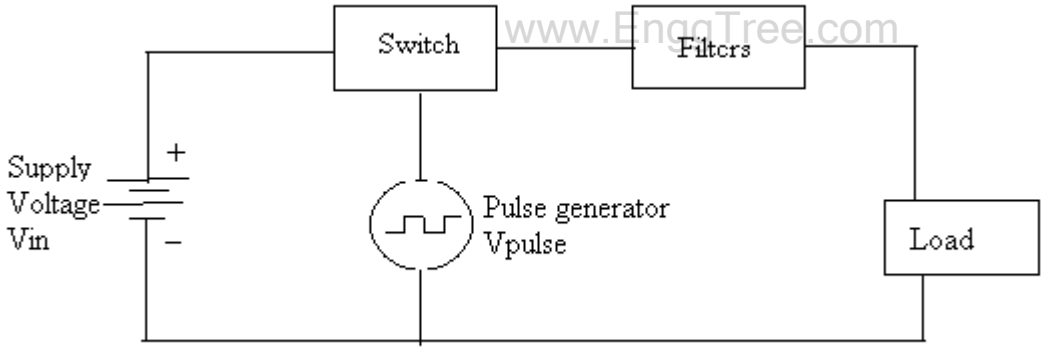
Switching Regulator:

Explain the basic operation of switching regulator.

An example of general purpose regulator is Motorola's MC1723. It can be used in many different ways, for example, as a fixed positive or negative output voltage regulator, variable regulator or switching regulator because of its flexibility.

To minimize the power dissipation during switching, the external transistor used must be a switching power transistor. To improve the efficiency of a regulator, the series pass transistor is used as a switch rather than as a variable resistor as in the linear mode.

- A regulator constructed to operate in this manner is called a series switching regulator. In such regulators the series pass transistor is switched between cut off & saturation at a high frequency which produces a pulse width modulated (PWM) square wave output.
- This output is filtered through a low pass LC filter to produce an average dc output voltage.
- Thus the output voltage is proportional to the pulse width and frequency.
- The efficiency of a series switching regulator is independent of the input & output differential & can approach 95%



A basic switching regulator consists of 4 major components,

1. Voltage source Vin
2. Switch S1
3. Pulse generator Vpulse
4. Filter F1

1. Voltage Source Vin:

It may be any dc supply – a battery or an unregulated or a regulated voltage. The voltage source must satisfy the following requirements.

- It must supply the required output power & the losses associated with the switching regulator.

 It must be large enough to supply sufficient dynamic range for line & load regulations.

 It must be sufficiently high to meet the minimum requirement of the regulator system to be designed.

 It may be required to store energy for a specified amount of time during power failures.

2. Switch S1:

It is typically a transistor or thyristor connected as a power switch & is operated in the saturated mode. The pulse generator output alternately turns the switch ON & OFF

3. Pulse generator Vpulse:

It provides an asymmetrical square wave varying in either frequency or pulse width called frequency modulation or pulse width modulation respectively. The most effective frequency range for the pulse generator for optimum efficiency 20 KHz. This frequency is inaudible to the human ear & also well within the switching speeds of most inexpensive transistors & diodes.

 The duty cycle of the pulse wave form determines the relationship between the input & output voltages. The duty cycle is the ratio of the on time ton, to the period T of the pulse waveform.

Duty cycle = ton/(ton+toff) = ton/T =ton.f

Where ton = On-time of the pulse waveform toff=off-time of the pulse wave form

T = time period = ton + toff

= 1/frequency or T = 1/f

 Typical operating frequencies of switching regulator range from 10 to 50 kHz.

 Lower operating frequency improve efficiency & reduce electrical noise, but require large filter components (inductors & capacitors).

4. Filter F1:

It converts the pulse waveform from the output of the switch into a dc voltage. Since this switching mechanism allows a conversion similar to transformers, the switching regulator is often referred to as a dc transformer.

The output voltage Vo of the switching regulator is a function of duty cycle & the input voltage Vin.

Vo is expressed as follows, Vo= ton Vin/T

 This equation indicates that, if time period T is constant, Vo is directly proportional to the ON-time, ton for a given value of Vin. This method of changing the output voltage by varying ton is referred to as a pulse width modulation.

 Similarly, if ton is held constant, the output voltage Vo is inversely proportional to the period T or directly proportional to the frequency of the pulse waveform. This method of varying the output voltage is referred to as frequency modulation (FM).

 Switching regulator can operate in any of 3 modes

i) Step – Down

ii) Step – Up

iii) Polarity inverting

Monolithic Switching Regulator [µa78s40]:

The µA78S40 consists of a temperature compensated voltage reference, duty cycle controllable oscillator with an active current limit circuit, a high gain comparator, a high- current, high voltage output switch, a power switching diode & an uncommitted op-amp.

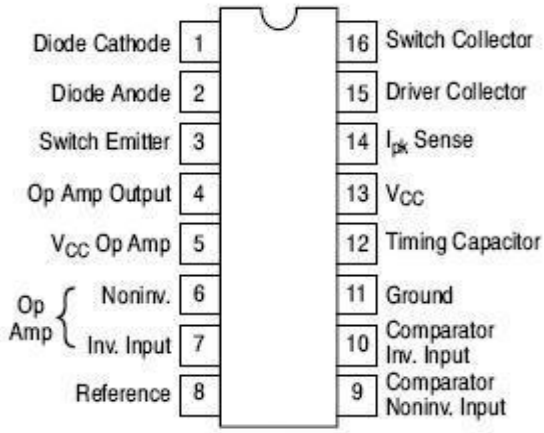
Important features of the µA78S40 switching regulators are:

- Step up, down & Inverting operation
- Operation from 2.5 to 40V input
- 80dB line & load regulations
- Output adjustable from 1.3 to 40V
- Peak current to 1.5A without external resistors
- Variable frequency, variable duty cycle device

The internal switching frequency is set by the timing capacitor CT, connected between pin12 & ground pin 11. The initial duty cycle is 6:1. The switching frequency & duty cycle can be modified by the current limit circuitry, IPK sense, pin14, 7 the comparator, pin9 & 10.

Comparator:

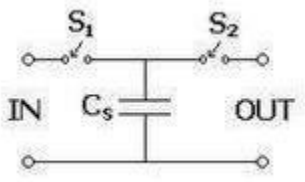
The comparator modifies the OFF time of the output switch transistor Q1 & Q2. In the step – up & step down modes, the non-inverting input(pin9) of the comparator is connected to the voltage reference of 1.3V (pin8) & the inverting input (pin10) is connected to the output terminal via the voltage divider network.



The Switched Capacitor Filter or MF10

Explain about switched capacitor filter circuits. [Nov/Dec 2021] [Nov/Dec 2022]

Basic Representation



The simplest switched capacitor (SC) circuit is the switched capacitor resistor, made of one capacitor C and two switches S1 and S2 which connect the capacitor with a given frequency alternately to the input and output of the SC. Each switching cycle transfers a charge *q* from the input to the output at the switching frequency *f*. Recall that the charge *q* on a capacitor *C* with a voltage *V* between the plates is given by: q=cv
where *V* is the voltage across the capacitor.

The SC resistor is used as a replacement for simple resistors in integrated circuits because it is easier to fabricate reliably with a wide range of values. It also has the benefit that its value can be adjusted by changing the switching frequency. See also: operational amplifier applications.

This same circuit can be used in discrete time systems (such as analog to digital converters) as a track and hold circuit. During the appropriate clock phase, the capacitor samples the analog voltage through switch one and in the second phase presents this held sampled value to an electronic circuit for processing.

Switched Capacitor Circuits:

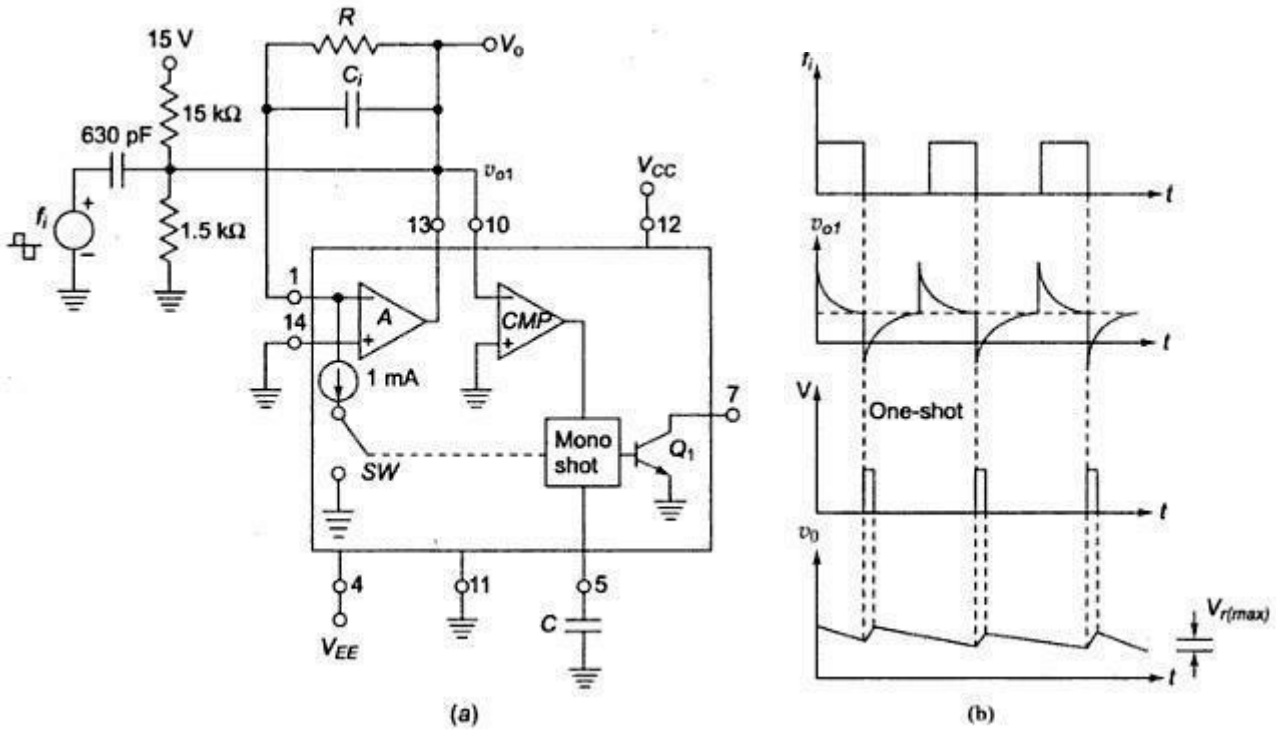
The switched capacitor filter allows for very sophisticated, accurate, and tuneable analog circuits to be manufactured without using resistors.

Advantages: resistors are hard to build on integrated circuits (they take up a lot of room), and the circuits can be made to depend on ratios of capacitor values (which can be set accurately), and not absolute values (which vary between manufacturing runs).

Frequency to Voltage (F-V) and voltage to frequency convertors (V-F)

Explain the basic operations of F-V and V-F converters.

- F-V convertors applications: Tachometer in motor speed control Rotational speed measurement.
- Two types of it: Pulse integrating Phase locked loop
- F-V convertor produces an output voltage whose amplitude is a function of input signal frequency.
- V0=kf fi kf is sensitivity of F-V convertor
- It is basically a FM discriminator.



Input frequency is applied to comparator A. Resistor R acts as feedback element.

Capacitor Ci enables charge-balancing, High pass network conditions input signal For negative spike of V01, comparator COMP triggers one shot multivibrator with threshold 7.5V The output of multivibrator closes the switch SW, for a time TH, this causes voltage Vo to build up and inject thru R and this continues until current out of summing input of opamp is equal to that injected by Vo through R continuously.

Vo=10-3 *TH *R*fi as TH =7.5 C /1X10-3

Ripple Voltage, Vr(max) =7.5 C /Ci

Voltage to frequency convertor

Principle: Charge balancing technique-the process of charging and discharging results in frequency proportional to input signal F0= k Vi

Operation: Op-amp A converts input Vi to current Ii = Vi/R into summing junction. When switch SW is open the current flows into capacitor Ci and charges it, and node voltage Vo1 produce ramp down.

When V01 =0 CMP triggers and sends a triggering signal to one shot multivibrator that closes the switch SW and turns transistor Q ON for time TH.

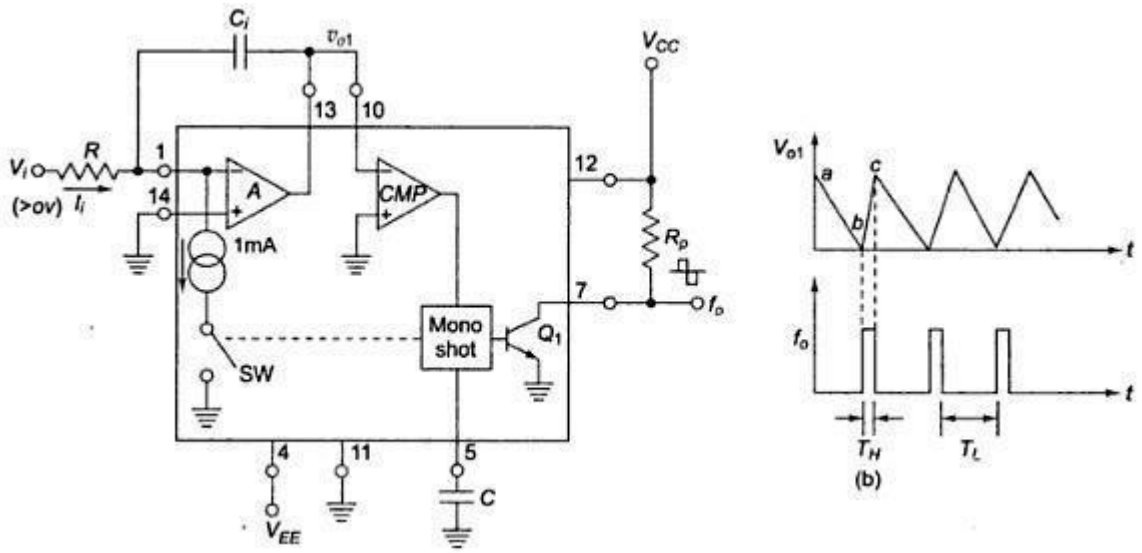
The threshold of mono shot = 7.5 V and TH= 7.5 C/10-3

During TH , V01 ramps upward by amount Δ 01=(1mA-Ii) TH /Ci

Time duration TL for vo1 to return to 0 is TL = CΔ 01/Ii

TL+TH = 1mA TH /Ii = T

F0=Vi/7.5 RC



Power Audio Amplifier IC LM 380

Explain the basic operation of LM380 power audio amplifier.

Introduction:

Small signal amplifiers are essentially voltage amplifier that supplies their loads with larger amplifier signal voltage.

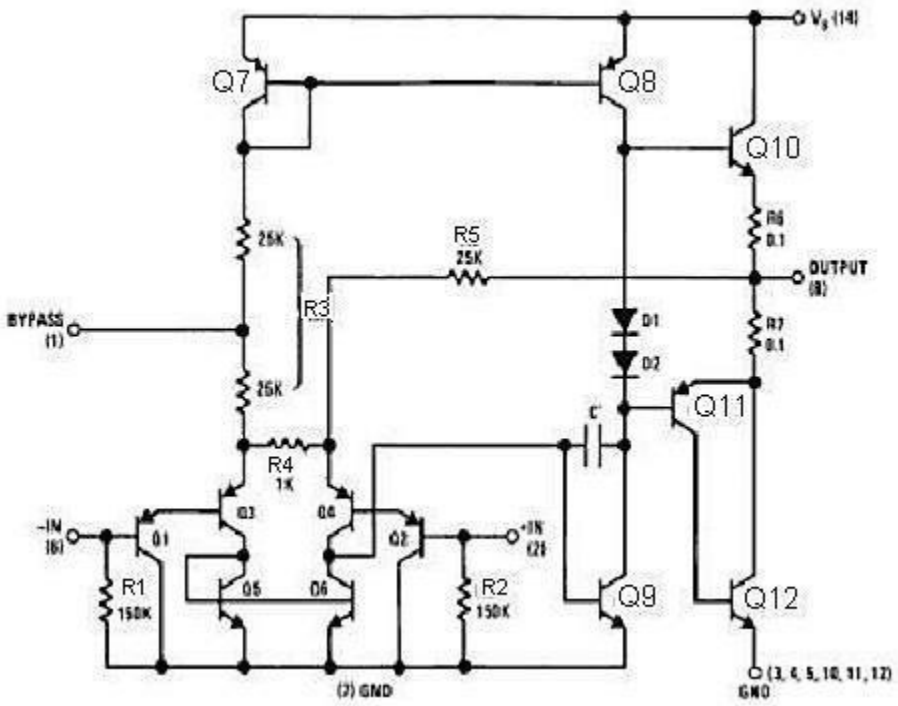
On the other hand, large signal or power amplifier supply a large signal current to current operated loads such as speakers & motors.

In audio applications, however, the amplifier called upon to deliver much higher current than that supplied by general purpose op-amps. This means that loads such as speakers & motors requiring substantial currents cannot be driven directly by the output of general purpose op-amps.

To handle it following is done

- To use discrete or monolithic power transistors called power boosters at the output of the op-amp
- To use specialized ICs designed as power amplifiers like LM 380.
- Features of LM380:

1. Internally fixed gain of 50 (34dB)
2. Output is automatically self centering to one half of the supply voltage.
3. Output is short circuit proof with internal thermal limiting.
4. Input stage allows the input to be ground referenced or ac
5. Supply voltage range (5 to 22V).
6. High peak current capability.
7. High impedance.



LM380 circuit description:

It is connected of 4 stages,

(i) PNP emitter follower

(ii) Different amplifier

(iii) Common emitter

(iv) Emitter follower

(i) PNP Emitter follower:

 The input stage is emitter follower composed of PNP transistors Q1 & Q2 which drives the PNP Q3-Q4 differential pair.

 The choice of PNP input transistors Q1 & Q2 allows the input to be referenced to ground i.e., the input can be direct coupled to either the inverting & non-inverting terminals of the amplifier.

(ii) Differential Amplifier:

 The current in the PNP differential pair Q3-Q4 is established by Q7, R3 & +V.

 The current mirror formed by transistor Q7, Q8 & associated resistors then establishes the collector current of Q9.

 Transistor Q5 & Q6 constitute of collector loads for the PNP differential pair.

 The output of the differential amplifier is taken at the junction of Q4 & Q6 transistors & is applied as an input to the common emitter voltage gain.

(iii) Common Emitter amplifier

 Common Emitter amplifier stage is formed by transistor Q9 with D1, D2 & Q8 as a current source load.

stage:

 The capacitor C between the base & collector of Q9 provides internal compensation & helps to establish the upper cutoff frequency of 100 KHz.

 Since Q7 & Q8 form a current mirror, the current through D1 & D2 is approximately the same as the current through R3.

 D1 & D2 are temperature compensating diodes for transistors Q10 & Q11 in that D1 & D2 have the same characteristics as the base-emitter junctions of Q11. Therefore the current through Q10 & (Q11-Q12) is approximately equal to the current through diodes D1 & D2.

(iv) (Output stage) - Emitter follower:

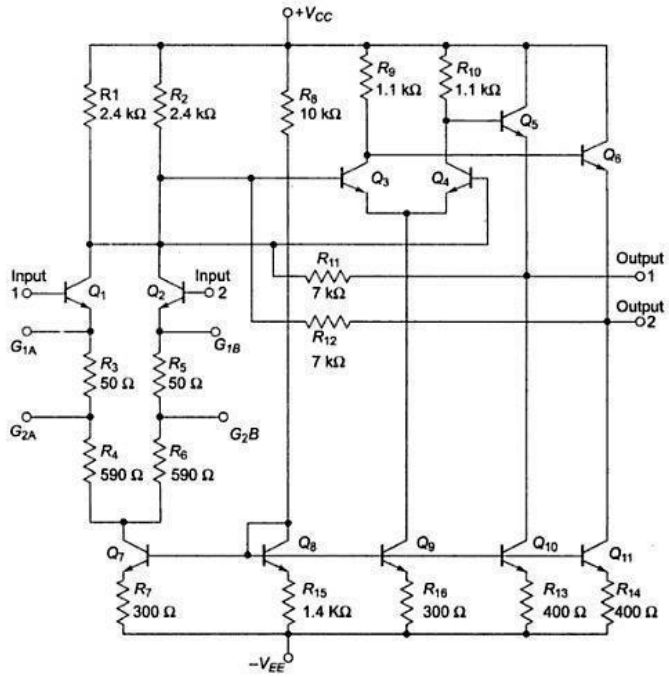
 Emitter follower formed by NPN transistor Q10 & Q11. The combination of PNP transistor Q11 & NPN transistor Q12 has the power capability of NPN transistors but the characteristics of a PNP transistor.

 The negative dc feedback applied through R5 balances the differential amplifier so that the dc output voltage is stabilized at +V/2;

 To decouple the input stage from the supply voltage +V, by pass capacitor in order of micro farad should be connected between the bypass terminal (pin 1) & ground (pin 7).

 The overall internal gain of the amplifier is fixed at 50. However gain can be increased by using positive feedback.

Monolithic video amplifier



Give the classifications of power amplifiers and explain. [Nov/Dec 2021]

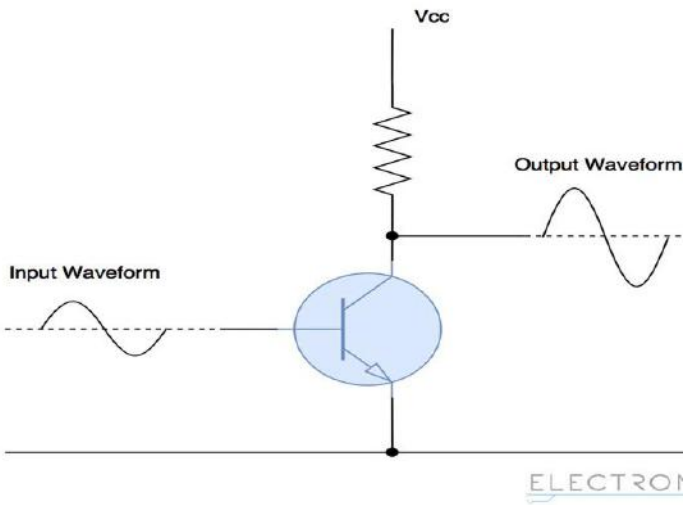
Power Amplifier Classes

- ✓ There are multiple ways of designing a power amplifier circuit.
- ✓ The operation and output characteristics of each of the circuit configurations differs from one another.
- ✓ To differentiate the characteristics and behavior of different power amplifier circuits, Power Amplifier Classes are used in which, letter symbols are assigned to identify the method of operation.
- ✓ They are broadly classified into two categories. Power amplifiers designed to amplify analog signals come under A, B, AB or C category.
- ✓ Power amplifiers designed to amplify Pulse Width Modulated (PWM) digital signals come under D, E, F etc.
- ✓ The most commonly used power amplifiers are the ones used in audio amplifier circuits and they come under classes A, B, AB or C. So, let's take a look at them in detail.

Class A Power Amplifier

- ✓ Analog waveforms are made up of positive highs and negative lows.
- ✓ In this class of amplifiers, the entire input waveform is used in the amplification process.
- ✓ A single transistor is used to amplify both the positive and negative halves of the waveform.
- ✓ This makes their design simple and makes class A amplifier the most commonly used type of power amplifiers.

- ✓ Although this class of power amplifiers are superseded by better designs, they are still popular among hobbyists.

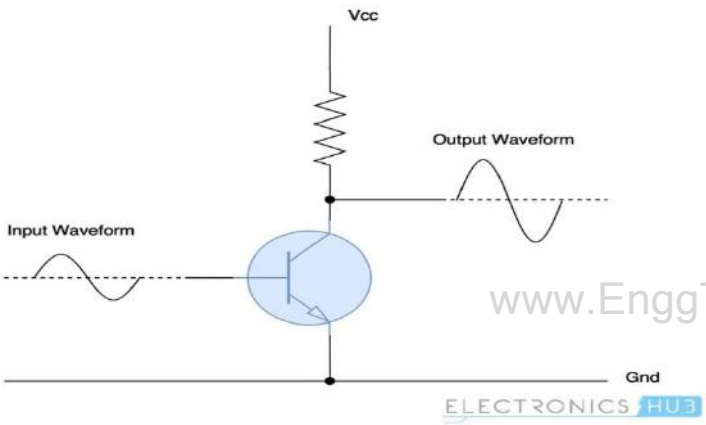


- ✓ In this class of amplifiers, the active element (the electronic component used for amplifying, which is transistor in this case) is in use all the time even if there is no input signal.
- ✓ This generates lot of heat and reduces the efficiency of class A amplifiers to 25% in case of normal configuration and 50% in case of transformer coupled configuration.

- ✓ The conduction angle (the portion of waveform used for amplification, out of 360°) for class A amplifiers is 360°.
- ✓ So, the signal distortion levels are very less allowing better high frequency performance.

Class B Power Amplifier

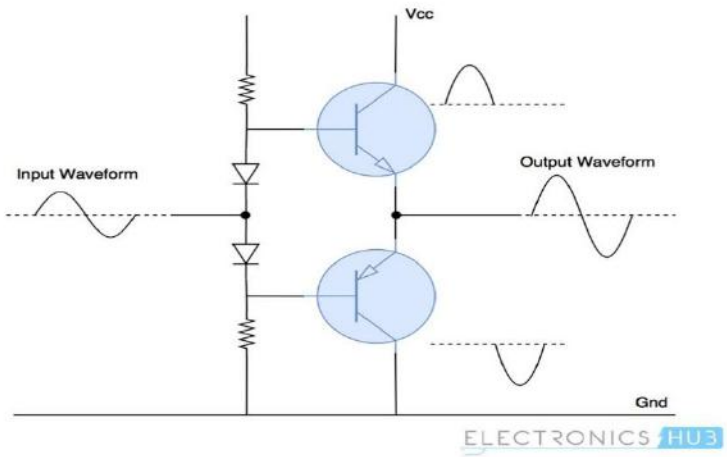
- ✓ Class B power amplifiers are designed to reduce the efficiency and heating problems present in the class A amplifier.
- ✓ Instead of a single transistor to amplify the entire waveform, this class of amplifiers use two complementary transistors.
- ✓ One transistor amplifies the positive half of the waveform and the other amplifies the negative half of the waveform.
- ✓ So, each active device conducts for one half (180°) of the waveform and two of them, when combined, amplify the entire signal.



- ✓ The efficiency of class B amplifiers is improved a lot over class A amplifiers because of two transistor design.
- ✓ They can reach a theoretical efficiency of about 75%.
- ✓ Power amplifiers of this class are used in battery operated devices like FM radios and transistor radios.
- ✓ Because of superposition of two halves of the waveform, there exists a small distortion at the crossover region.
- ✓ To reduce this signal distortion, class AB amplifiers are designed.

Class AB Power Amplifier

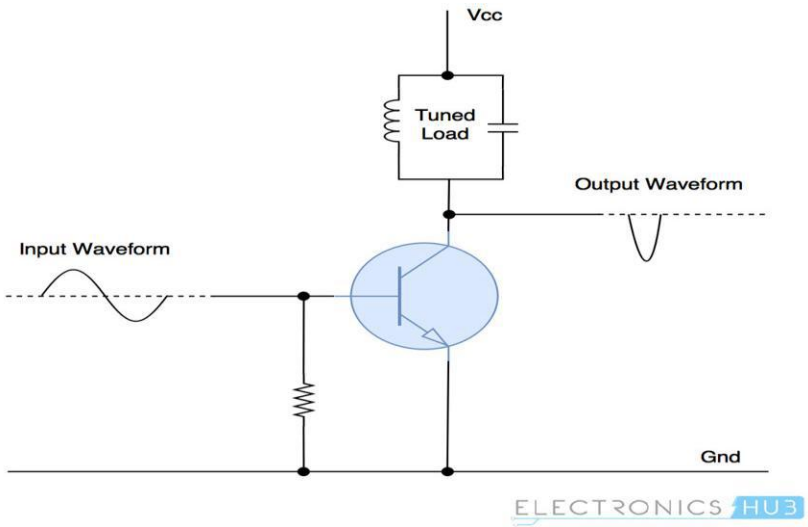
- ✓ Class AB amplifiers are a combination of class A and class B amplifiers.
- ✓ This class of amplifiers are designed to reduce the less efficiency problem of class A amplifiers and distortion of signal at crossover region in class B amplifiers.



- ✓ It maintains high frequency response like in class A amplifiers and good efficiency as in class B amplifiers.
- ✓ A combination of diodes and resistors are used to provide little bias voltage which reduces the distortion of waveform near the crossover region.
- ✓ There is a little drop in efficiency (60%) because of this.

Class C Power Amplifier

- ✓ The design of class C power amplifiers allows greater efficiencies but reduces the linearity/conduction angle, which is under 90°.
- ✓ In other words, it sacrifices quality of amplification for increase in efficiency.
- ✓ Lesser conduction angle implies greater distortion and so this class of amplifiers are not suited for audio amplification.
- ✓ They are used in high frequency oscillators and amplification of Radio Frequency signals.
- ✓ Class C amplifiers generally contain a tuned load which filters and amplifies input signals of certain frequency, and the waveforms of other frequencies are suppressed.



- ✓ In this type of power amplifier, the active element conducts only when the input voltage is above a certain threshold, which reduces power dissipation and increases efficiency.

Q.Describe the performance parameters of IC regulators. [Nov/Dec 2021]

- ✓ Depending on the application, other parameters may be important, such as output ripple voltage, load transient response, output noise, and efficiency.

1.Input Voltage and Output Voltage

The first step towards choosing a voltage regulator is knowing about the input voltage and output voltage that you will be working with. Linear voltage regulators need input voltage that is higher than the rated output voltage. If the input voltage is less than the desired output voltage, then it leads to the condition of insufficient voltage that causes the regulator to drop out and provide unregulated output.

2. Dropout Voltage

Dropout voltage is the difference between input and output voltage of the voltage regulator. For example, min. The input voltage for 7805 is 7V, and the output voltage is 5V, so it has a dropout voltage of 2V. If the input voltage goes below, the output voltage (5V) + dropout voltage (2V) will result in an unregulated output that can damage your device. So before selecting a voltage regulator, check the dropout voltage.

Dropout voltage varies with voltage regulators; for example, you can find a range of 5V regulators with different dropout voltage. Linear regulators can be extremely efficient when they are operated with a very low input dropout voltage. So if you are using a battery as a power source, then you can use LDO regulators for better efficiency.

3. Power Dissipation

Linear voltage regulators dissipate more power than switching voltage regulators. Excessive power dissipation can cause battery drain, overheating, or damage to the product. So if you are using a linear voltage regulator, first calculate the power dissipation. For linear regulators, power dissipation can be calculated by:

Power = (Input Voltage – Output Voltage) x Current

4. Efficiency

Efficiency is the ratio of output power to input power that is proportional to the ratio of the output voltage to the input voltage. So the efficiency of Voltage regulators is directly limited by the dropout voltage and quiescent current because of the higher the dropout voltage, the lower the efficiency.

For higher efficiency, drop out voltage and quiescent current must be minimized, and the voltage difference between input and output must be minimized.

5. Voltage Accuracy

The overall accuracy of a voltage regulator depends on line regulation, load regulation, reference voltage drift, error amplifier voltage drift, and temperature coefficient. Typical linear regulators usually have an output voltage specification that guarantees the regulated output will be within 5% of nominal. So if you are using the voltage regulator to power the digital ICs, then 5% tolerance is not a big concern.

6. Load Regulation

Load regulation is defined as the circuit's ability to maintain a specified output voltage under varying load conditions. Load regulation is expressed as:

Load Regulation = ΔVout/ ΔI_{out}

7. Line Regulation

Line regulation is defined as the circuit's ability to maintain the specified output voltage with the varying input voltage. Line regulation is expressed as:

Load Regulation = $\Delta V_{out} / \Delta V_{in}$

So for **selecting a proper voltage regulator for any application**, one should keep all the above factors in consideration,

Opto couplers/Opto Isolators and fibre optic IC

Explain the basics of opto copupler.

- Opto couplers or Opt isolators is a combination of light source & light detector in the same package.
- They are used to couple signal from one point to other optically, by providing a complete electric isolation between them. This kind of isolation is provided between a low power control circuit & high power output circuit, to protect the control circuit.

- Characteristics of opto coupler:

(i) Current Transfer Ratio:

It is defined as the ratio of output collector current (Ic) to the input forward current (If) CTR = Ic/If * 100%. Its value depends on the devices used as source & detector.

(ii) Isolation voltage between input & output:

It is the maximum voltage which can exist differentially between the input & output without affecting the electrical isolation voltage is specified in K Vrms with a relative humidity of 40 to 60%.

(iii) Response Time:

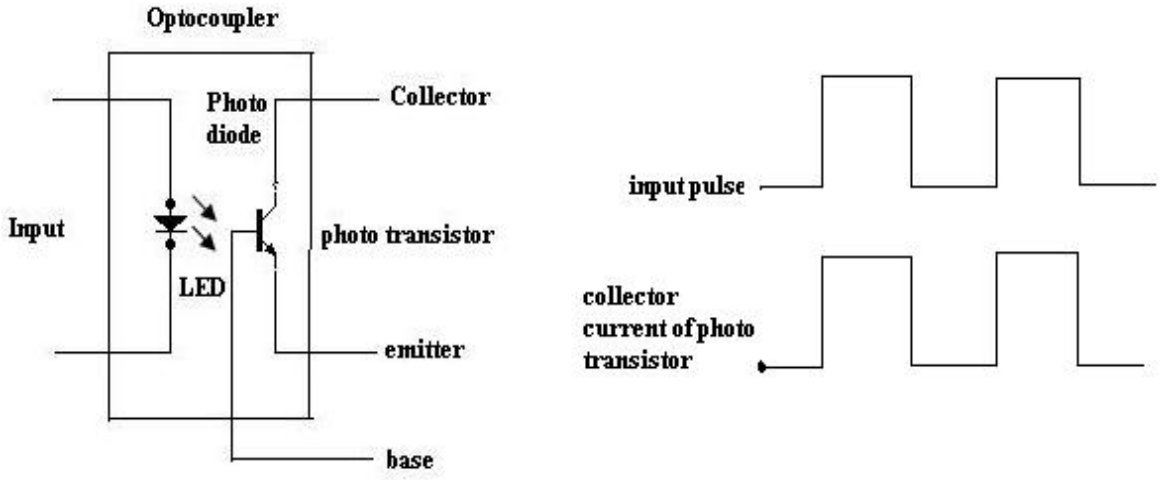
Response time indicates how fast an opto coupler can change its output state. Response time largely depends on the detector transistor, input current & load resistance.

(iv) Common mode Rejection:

Even though the opto couplers are electrically isolated for dc & low frequency signals, an impulsive input signal (the signal which changes suddenly) can give rise to a displacement current Ic= Cf*dv/dt. This current can flow between input & output due to the capacitance Cf existing between input & output. This allows the noise to appear in the output. Depending on the type of light source & detector used we can get a variety of opto couplers.

They are as follows,

(i) LED – Photodiode opto coupler:



 The LED phototransistor opto coupler shown in figure. An infrared LED acts as a light source and the phototransistor acts as a photo detector.

 This is the most popularly used opto coupler, because it does not need any additional amplification.

 When the pulse at the input goes high, the LED turns ON. The light emitted by the LED is focused on the CB junction of the phototransistor.

 In response to this light photocurrent starts flowing which acts as a base current for the phototransistor.

 The collector current of phototransistor starts flowing. As soon as the input pulse reduces to zero, the LED turns OFF & the collector current of phototransistor reduces to zero. Thus the pulse at the input is optically coupled to the output side.

 The input & output waveforms are 180º out of phase as the output is taken at the collector of the phototransistor

Advantages of Opto coupler:

 Control circuits are well protected due to electrical isolation.

 Wideband signal transmission is possible.

 Due to unidirectional signal transfer, noise from the output side does not get coupled to the input side.

 Interfacing with logic circuits is easily possible.

 It is small size & light weight device.

Disadvantages:

 Slow speed.

 Possibility of signal coupling for high power signals.

Applications:

Opto couplers are used basically to isolate low power circuits from high power circuits.

 At the same time the control signals are coupled from the control circuits to the high power circuits.

 Some of such applications are,

(i) AC to DC converters used for DC motor speed control

(ii) High power choppers

(iii) High power inverters

 One of the most important applications of an opto coupler is to couple the base driving signals to a power transistor connected in a DC-DC chopper.

Opto coupler IC

The optocouplers are available in the IC form MCT2E is the standard optocoupler IC which is used popularly in many electronic application.

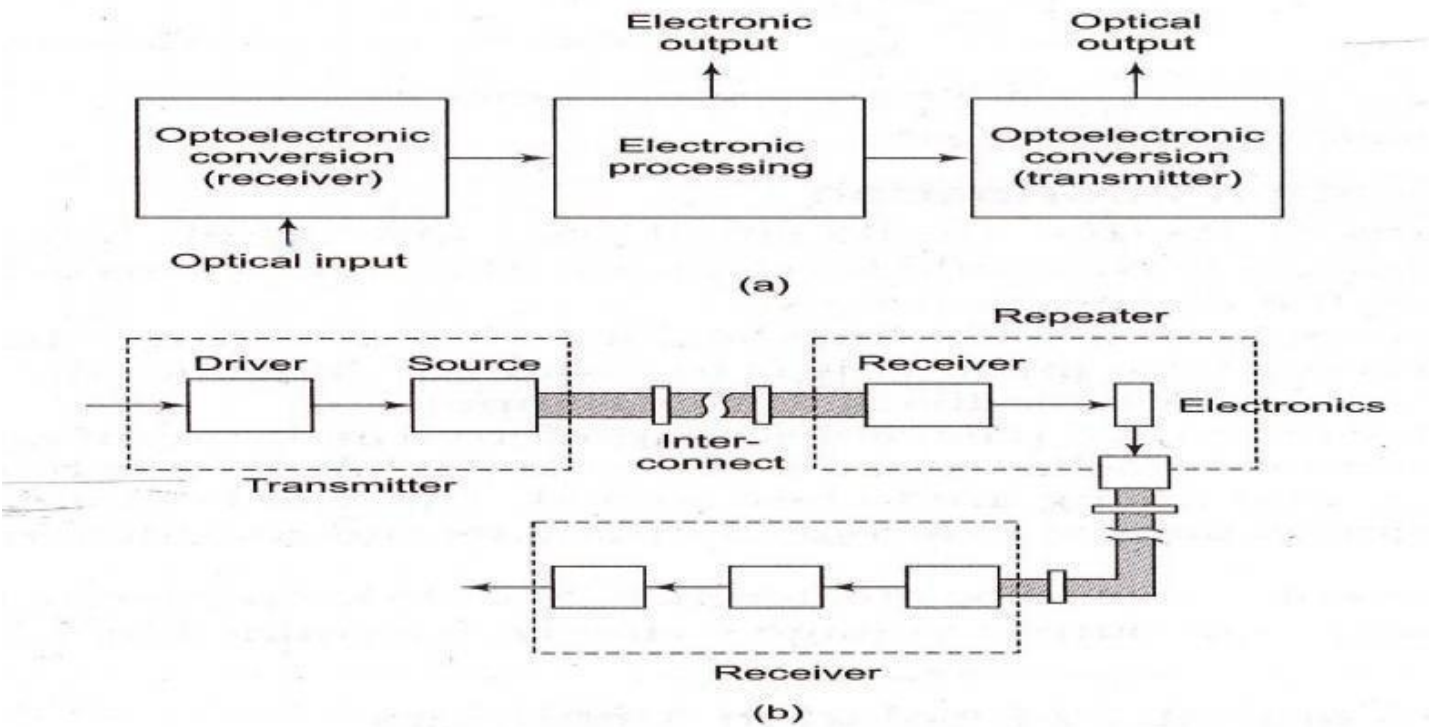
 This input is applied between pin 1& pin 2. An infrared light emitting diode is connected between these pins.

 The infrared radiation from the LED gets focused on the internal phototransistor.

 The base of the phototransistor is generally left open. But sometimes a high value pull down resistance is connected from the Base to ground to improve the sensitivity.

 The block diagram shows the opto-electronic-integrated circuit (OEIC) and the major components of a fiber-optic communication facility.

The block diagram shows the opto-electronic-integrated circuit (OEIC) and the major components of a fiber-optic communication facility.



Unit-5

Two Marks

1.**Mention any two audio frequency oscillators.**

- RC phase shift oscillator
- Wein bridge oscillator

2. What are the requirements of producing sustained oscillation in feedback circuits?

For sustained oscillations, The total phase shift around the loop must be zero at the desired frequency of oscillation fo. i.e , AB = 0 (or) 360°. At fo, the magnitude of the loop gain | A β | should be equal to unity

3. **What is a multivibrator?**

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator.

4. **What do you mean by monostable multivibrator?**

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi-stable state. An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state.

5.**What is an astable multivibrator?**

Astable multivibrator is a free running oscillator having two quasistable states. Thus, there is oscillations between these two states and no external signal are required to produce the change in state.

5.**What is a bistable multivibrator?**

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied . Thus, it requires two external triggers before it returns to its initial state.

6.Mention some applications of 555 timer:

 Oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, Traffic light control.

7. **List the applications of 555 timer in monostable mode of operation:**

 Missing pulse detector, Linear ramp generator, Frequency divider, Pulse width modulation.

8. **List the applications of 555 timer in Astable mode of operation:**

 FSK generator, Pulse-position modulator

9. **List the applications of 555 timer in monostable mode of operation:**

 Missing pulse detector, Linear ramp generator, Frequency divider, Pulse width modulation.

10. **List the applications of 555 timer in Astable mode of operation:**

 FSK generator, Pulse-position modulator

11. **What is a voltage regulator?**

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

12.**Give the classification of voltage regulators:**

 Series / Linear regulators, Switching regulators.

13. What is opto coupler?

An opto-isolator, also called an optocoupler, photocoupler, or optical isolator, is "an electronic device designed to transfer electrical signals by utilizing light waves to provide coupling with electrical isolation between its input and output". The main purpose of an opto-isolator is "to prevent voltages or rapidly changing voltages on one side of the circuit from damaging components or distorting transmissions on the other side

14.**What is a linear voltage regulator?** [Nov/Dec 2022]

Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region .The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.

14.**What is a switching regulator?**

Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulators.

15.What are the advantages of IC voltage regulators?

 Low cost, High reliability, Reduction in size, Excellent performance

16.**Give some examples of monolithic IC voltage regulators:**

 78XX series fixed output, positive voltage regulators, 79XX series fixed output, negative voltage regulators, 723 general purpose regulator.

17. **What is the purpose of having input and output capacitors in three terminal IC regulators?**

A capacitor connected between the input terminal and ground cancelsthe inductive effects due to long distribution lea ds. The output capacitor improvesthe transient response.

18. **Define line regulation.**

Line regulation is defined as the percentage change in the output voltage for a change in the input voltage. It is expressed in milli volts or as a percentage of the output voltage.

19.**Define load regulation.**

Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.

20.**What is meant by current limiting?**

Current limiting refers to the ability of a regulator to prevent the load currentfrom increasing above a preset value.

21.**Give the drawbacks of linear regulators:** [Nov/Dec 2022]

 The input step down transformer is bulky and expensive because of low line frequency.

 Because of low line frequency, large values of filter capacitors are required to decrease the ripple.

 Efficiency is reduced due to the continuous power dissipation by the transistor as it operates in the linear region.

21.**What is the advantage of switching regulators?**

Greater efficiency is achieved as the power transistor is made to operate as low impedance switch. Power transmitted across the transistor is in discrete pulses rather than as a steady current flow. By using suitable switching loss reduction technique, the switching frequency can be increased so as to reduce the size and weight of the inductors and capacitors.

22.**What is an opto-coupler IC? Give examples.**

Opto-coupler IC is a combined package of a photo-emitting device and aphoto- sensing device. Examples for opto-coupler circuit: LED and a photo diode, LED and photo transistor, LED and Darlington. Examples for opto-coupler IC: MCT 2F , MCT 2E .

23.**Mention the advantages of opto-couplers.**

 Better isolation between the two stages, Impedance problem between the stages is eliminated.

 Wide frequency response, Easily interfaced with digital circuit, Compact and light weight.

 Problems such as noise, transients, contact bounce, are eliminated.

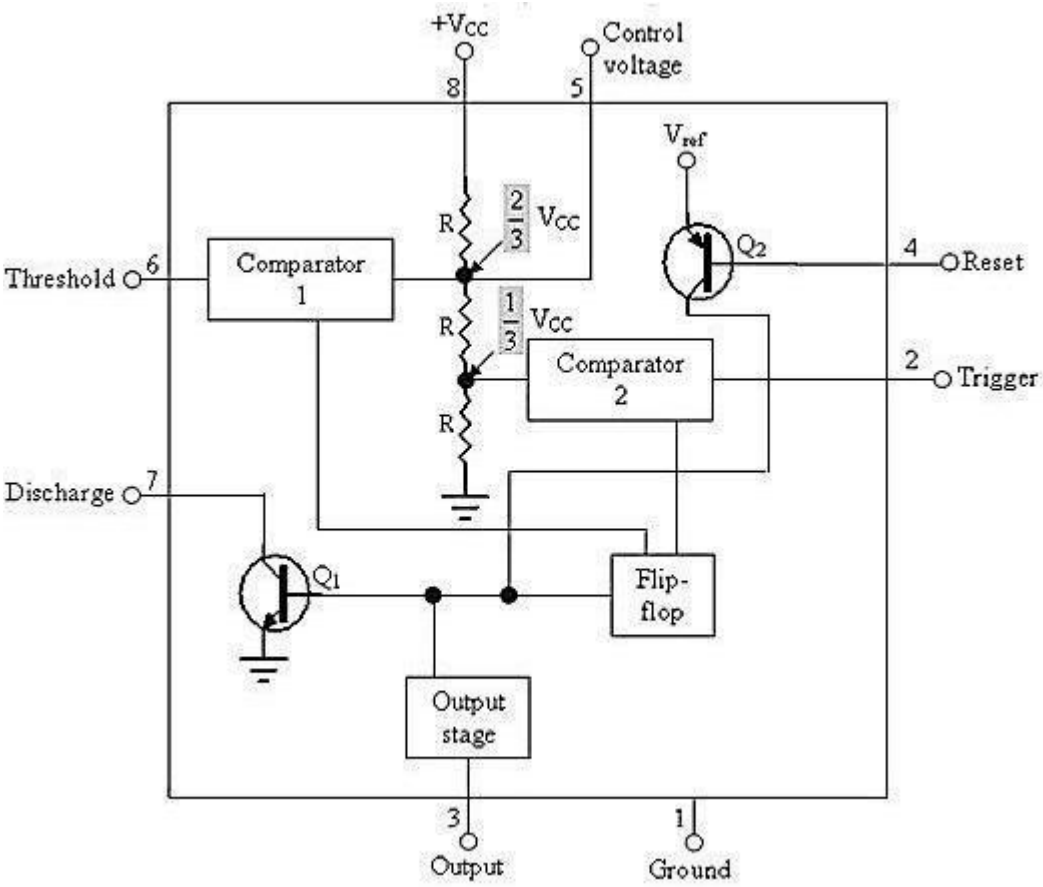
24.**What is an isolation amplifier?**

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

25.**What is the need for a tuned amplifier?**

In radio or TV receivers, it is necessary to select a particular channel among all other available channels. Hence some sort of frequency selective circuit is needed that will allow us to amplify the frequency band required and reject all the other unwanted signals and this function is provided by a tuned amplifier.

26. **Draw the functional block diagram of 555 timer. [Nov/Dec 2021]**



27. **State the principle used in voltage to frequency conversion. [Nov/Dec 2021]**

Principle: Charge balancing technique is the process of charging and discharging results in frequency proportional to input signal F0= k Vi

28. List the two modes of operation of 555 IC timer.[Nov/Dec 2022]

1. Astable mode operation
2. Monostable mode operation.

Low Drop Out (LDO) Regulators

Voltage regulators are used to provide a stable power supply voltage independent of load impedance, input-voltage variations, temperature, and time. Low-dropout regulators are distinguished by their ability to maintain regulation with small differences between supply voltage and load voltage. For example, as a lithium-ion battery drops from 4.2 V (fully charged) to 2.7 V (almost discharged), an LDO can maintain a constant 2.5 V at the load.

The increasing number of portable applications has thus led designers to consider LDOs to maintain the required system voltage independently of the state of battery charge. But portable systems are not the only kind of application that might benefit from LDOs. Any equipment that needs constant and stable voltage, while minimizing the upstream supply (or working with wide fluctuations in upstream supply), is a candidate for LDOs. Typical examples include circuitry with digital and RF loads.

A “linear” series voltage regulator (Figure 1) typically consists of a reference voltage, a means of scaling the output voltage and comparing it to the reference, a feedback amplifier, and a series pass transistor (bipolar or FET), whose voltage drop is controlled by the amplifier to maintain the output at the required value. If, for example, the load current decreases, causing the output to rise incrementally, the error voltage will increase, the amplifier output will rise, the voltage across the pass transistor will increase, and the output will return to its original value.

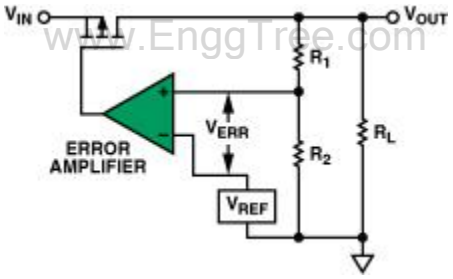


Figure 1. Basic enhancement-mode PMOS LDO.

In Figure 1, the error amplifier and PMOS transistor form a voltage-controlled current source. The output voltage, V_{OUT}, is scaled down by the voltage divider (R_1, R_2) and compared to the reference voltage (V_{REF}). The error amplifier's output controls an enhancement-mode PMOS transistor.

The *dropout voltage* is the difference between the output voltage and the input voltage at which the circuit quits regulation with further reductions in input voltage. It is usually considered to be reached when the output voltage has dropped to 100 mV below the nominal value. This key factor, which characterizes the regulator, depends on load current and junction temperature of the pass transistor.

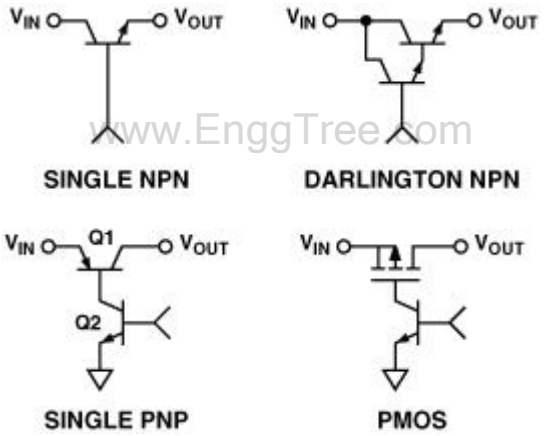
The source of the input voltage needs to be considered in order to choose a suitable category of LDO. In battery-powered applications, LDOs must maintain the required system voltage as the battery discharges. If the dc input voltage is provided from a rectified ac source, the dropout voltage may not be critical, so a standard regulator—which may be cheaper and can provide more load current—could be a better choice. But an LDO could be the right choice if lower power dissipation or a more precise output voltage is necessary.

The regulator should, of course, be able to provide enough current to the load with specified accuracy under worst-case conditions.

LDO Topologies

In Figure 1, the pass device is a PMOS transistor. However, a variety of pass devices are available, and LDOs can be classified depending on which type of pass device is used. Their differing structures and characteristics offer various advantages and drawbacks.

Examples of four types of pass devices are shown in Figure 3, including NPN and PNP bipolar transistors, Darlington circuits, and PMOS transistors.



For a given supply voltage, the bipolar pass devices can deliver the highest output current. A PNP is preferred to an NPN, because the base of the PNP can be pulled to ground, fully saturating the transistor if necessary. The base of the NPN can only be pulled as high as the supply voltage, limiting the minimum voltage drop to one V_{BE}. Therefore, NPN and Darlington pass devices can't provide dropout voltages below 1 V. They can be valuable, however, where wide bandwidth and immunity to capacitive loading are necessary (thanks to their characteristically low Z_{OUT}).

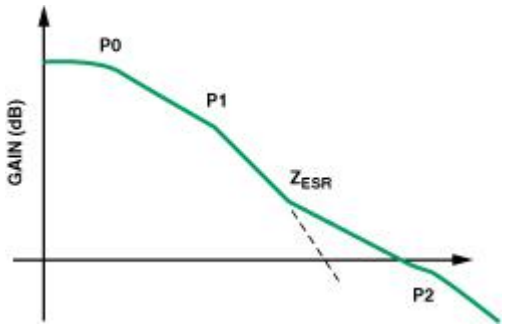
PMOS and PNP transistors can be effectively saturated, minimizing the voltage loss and the power dissipated by the pass device, thus allowing low dropout, high-efficiency voltage regulators. PMOS pass devices can provide the lowest possible dropout voltage drop, approximately $R_{DS(ON)} \times I_L$. They also allow the quiescent current flow to be minimized.

The main drawback is that the MOS transistor is often an external component—especially for controlling high currents—thus making the IC a *controller*, rather than a complete self-contained regulator.

The power loss in a complete regulator is

$$P_D = (V_{IN} - V_{OUT})\, I_L + V_{IN}\, I_{GND}$$

The first part of this relationship is the dissipation of the pass device; the second part is the power consumption of the controller portion of the circuit. The ground current in some regulators, especially those using saturable bipolar transistors as pass devices, can peak during power-up.



LDO frequency amplitude response.

PART B

1. Write note on optocoupler. [Nov/Dec 2022]

Opto-coupler is an electronic component that transfers electrical signals between two isolated circuits. Optocoupler also called Opto-isolator, photo coupler or optical isolator.

Optocoupler is used to isolate circuitry to prevent electrical collision chances or to exclude unwanted noises.

In present commercial market, we can buy Opto-coupler with 10 kV to 20 kV input to output withstand voltage capacity, with a specification of 25 kV / uS voltage transients.

Types of Optocouplers

There are many different types of Optocouplers are available commercially based on their needs and switching capabilities. Depending on the use there are mainly four types of optocouplers are available.

1. Opto-coupler which use Photo Transistor.
2. Opto-coupler which use Photo Darlington Transistor.
3. Opto-coupler which use Photo TRIAC.
4. Opto-coupler which use Photo SCR.

Photo-Transistor Optocoupler

In the upper image the internal construction is shown inside a Photo-transistor Optocoupler. The Transistor type can be anything whether PNP or NPN.

Photo-Transistor can be further of two types depending on the output pin availability. On the second image on the left, there is additional pin out which is internally connected with transistor's base. This pin 6 is used to control the sensitivity of the photo-transistor. Often the pin is used to connect with ground or negative using a high value resistor. In this configuration, false triggering due to noise or electrical transients can be controlled effectively.

Also, before using Photo-transistor based optocoupler, the user must know the maximum rating of the transistor. PC816, PC817, LTV817, K847PH are few widely used photo-transistor based optocoupler. Photo – Transistor based opto-coupler is used in DC circuit related isolation.

Photo-Darlington Transistor Optocoupler

Darlington Transistor is two transistor pair, where one transistor controls other transistor base. In this configuration the Darlington Transistor provide high gain ability. As usual the LED emits infrared led and controls the base of the pair transistor.

This type of opto-coupler also used in DC circuit related area for the isolation. The 6th pin which is internally connected to the base of the transistor, used to control the sensitivity of the transistor as discussed previously in photo-transistor description. 4N32, 4N33, H21B1, H21B2, H21B3 are few photo-Darlington based opto-coupler example.

Photo-TRIAC Optocoupler

TRIAC is mainly used where AC based control or switching is needed. The led can be controlled using DC, and the TRIAC used to control AC. Opto-coupler provide excellent isolation in this case too. Here is one Triac Application. The photo-TRIAC based opto-coupler examples areIL420, 4N35 etc are example of TRIAC based opto-coupler.

Photo-SCR based Optocoupler

SCR stand for Silicon controlled rectifier, SCR also referred as Thyristor. Same as like other opto-coupler the LED emit Infrared. The SCR is controlled by the intensity of the LED. Photo-SCR based Opto-coupler used in AC related circuitry. Learn more about Thyristor here.

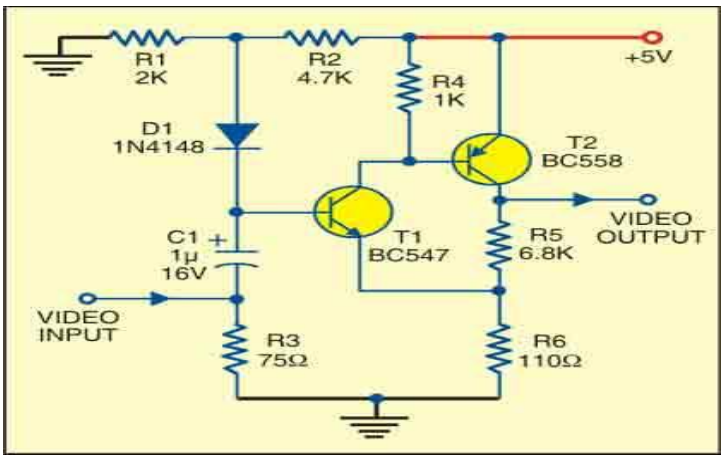
Few Examples of photo-SCR based opto-couplers are:- MOC3071, IL400, MOC3072 etc.

Applications of Optocoupler

Opto-coupler can be used for AC detection, DC control related operations. Let's see few applications of Opto-transistors.

2. Write note on video amplifier. [Nov/Dec 2022]

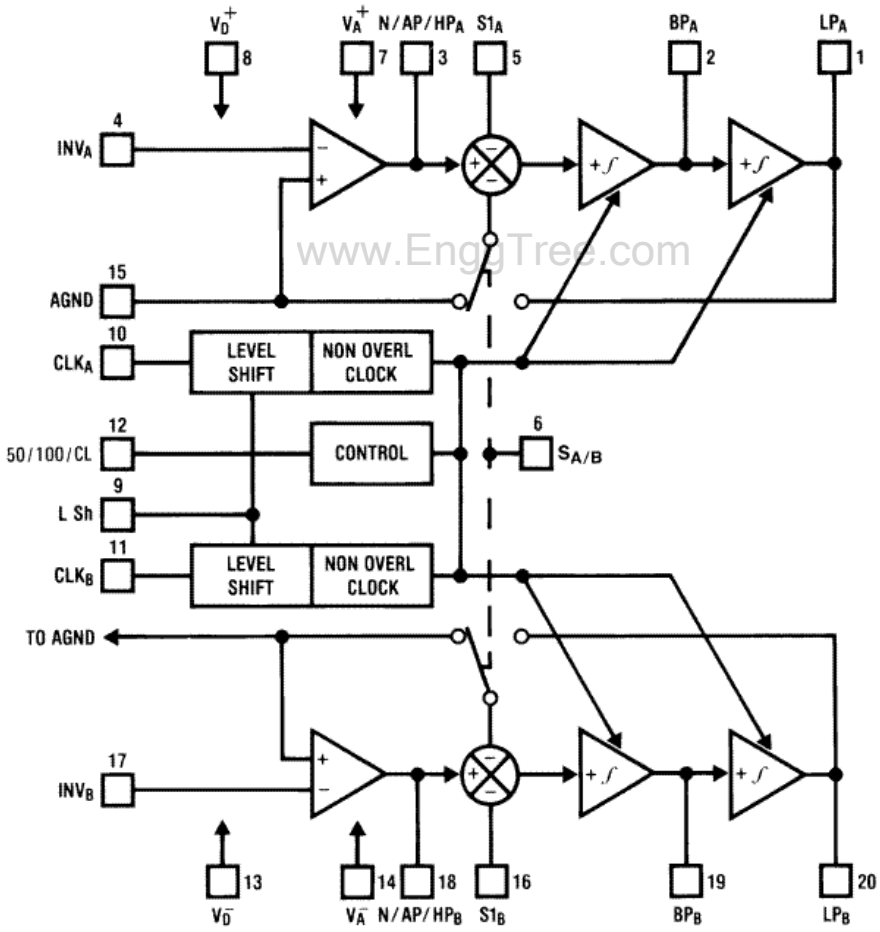
A video amplifier is a device or module that amplifies buffers and filters analog video signals to maintain signal fidelity across 75W cabling. Typical applications include video cable extension, video recording systems, floppy disk head amplifiers, pulsed amplifiers in communications.



The R1-R2 divider network adjusts the DC level of the video, while the R5-R6 divider network adjusts the gain. You may replace both the dividers with two 4.7-kilo-ohm (or 5-kilo-ohm) trimpots for proper adjustment of the DC level and the gain. The 75-ohm resistor (R3) may be discarded if you feed the video from a high-output-impedance stage.

Although the resistive load in the collector of the transistor provides reasonably good bandwidth, a peaking coil of 20 to 30 uH can be added in series with R4 to improve its performance at higher frequencies. With 1VPk-Pk signal as the input, the given circuit outputs 3.5VPk-Pk maximum amplitude at 6.25 MHz without the peaking coil.

3. Draw the functional block diagram of MF 10. [Nov/Dec 2022]



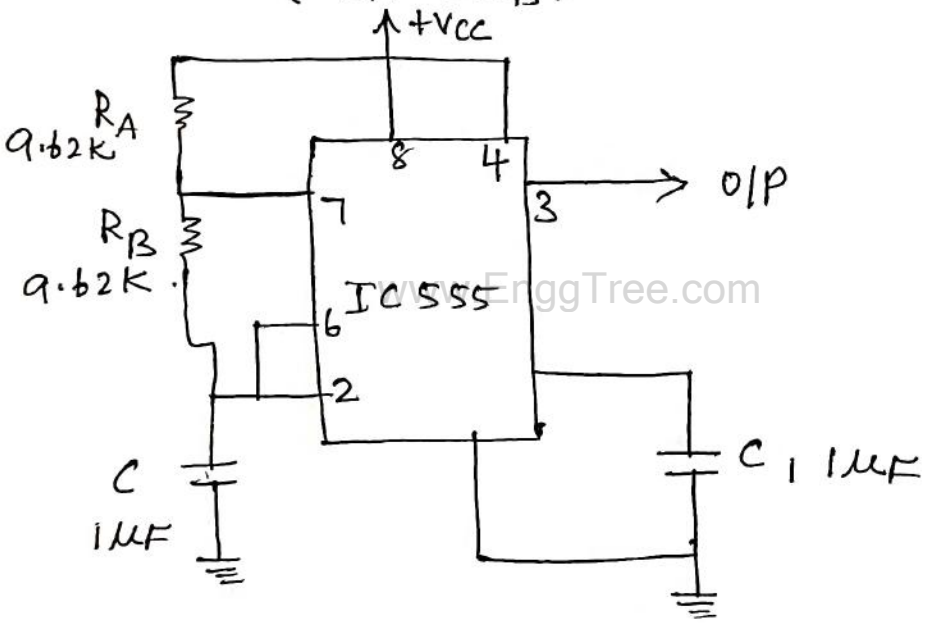
UNIT-5

PART B

1) Design an astable multivibrator using IC 555 IC with duty cycle 75% and $f_0 = 50kHz$. Assume $C = 1\mu F$? [NOV/Dec 2022]

$$T = 0.693 (R_A + 2R_B) C$$

$$D = \left(\frac{R_A + R_B}{R_A + 2R_B} \right) \times 100$$



$$f = \frac{1}{T} \Rightarrow T = \frac{1}{f} = \frac{1}{50 \times 10^3}$$

$C = 1\mu F$

Assume $R_A = R_B$

$$D = 75 = \frac{2R_A}{3R_A} = \frac{2}{3}$$

$$20 = 0.693 (3R_A) \times 1$$

$$R_A = R_B = 9.62 k\Omega.$$

1.9 JFET OPERATIONAL AMPLIFIER

LF155 JFET OP-AMP

The input impedance of the op-amp increased by using JFET differential amplifier as its input stage**.** It is the first monolithic JFET which uses well matched high voltage JFETs on the same chip with standard bipolar transistors. It has offset adjust feature due to which drifts and CMRR do not degrade.

FEATURES

- Guaranteed Offset Voltage Drift on All Grades.
- Guaranteed Slew Rate on All Grades.
- Guaranteed Low Input Offset Current 10pA Max.
- Guaranteed Low Input Bias Current 50pA Max.
- Guaranteed High Slew Rate (156A/356A) 10V/µs Min.
- Fast Settling to 0.01% 1.5µS.

INTERNAL SCHEMATIC

Figure 1.9.1 and Figure1.9.2 shown the schematic diagram and pin diagram of LF155

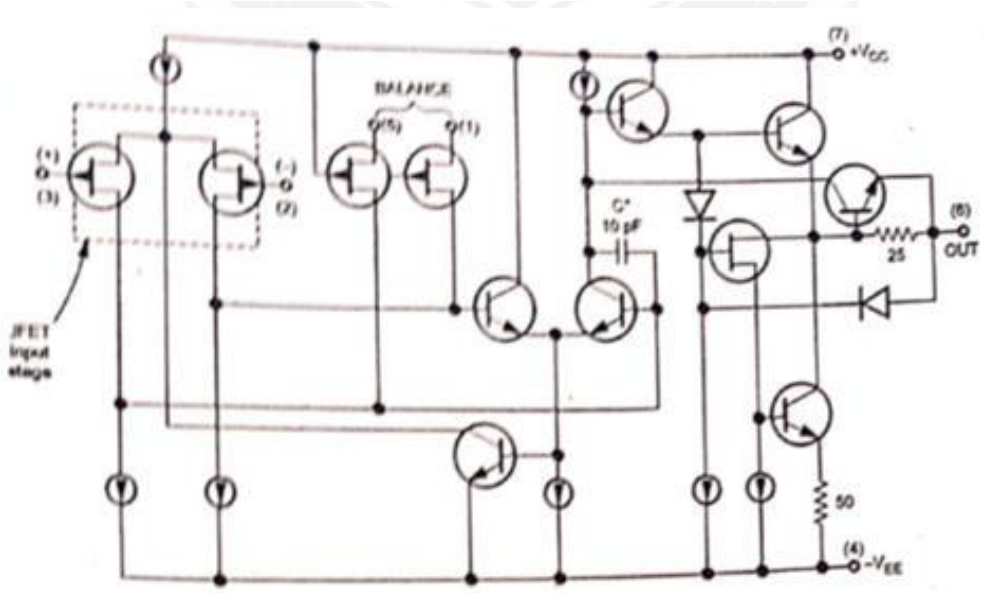


Figure 1.9.1 Schematic Diagram of LF155

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-27]

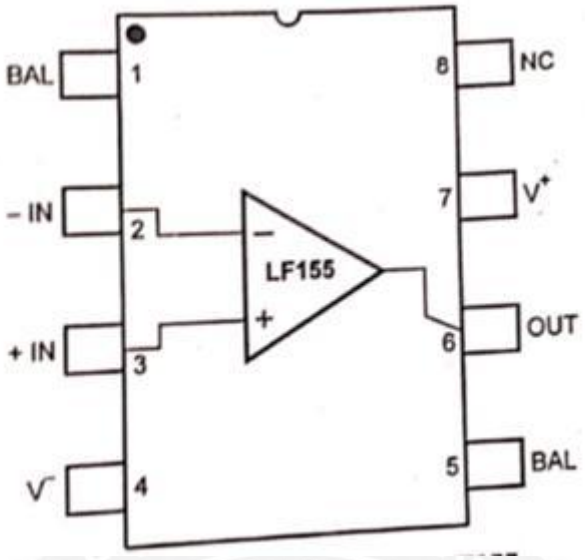


Figure1.9.2.Pin Diagram of LF155

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-27]

Applications:

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

TL082 JFET OP-AMP

The op-amp TL082 is low cost, high speed, dual JFET input op-amp with an internally trimmed input offset voltage.JFET has large reverse breakdown voltages from gate to source and drain hence clamping across the inputs is not required. This large differential input voltages can easily be accommodated without the need of large supply current.This op-amp requires low supply current and still maintain high slew rate and large gain bandwidth product. Due to JFET input stage, the input bias current and offset current is very low. Figure 1.9.3 and Figure 1.9.4 shows the pin diagram and internal schematic diagram of TL082.

FEATURES

- Internally Trimmed Offset Voltage: 15 mV
- Low Input Bias Current: 50 pA

- Low Input Noise Voltage: 16nV/√Hz
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 4 MHz
- High Slew Rate: 13 V/μs
- Low Supply Current: 3.6 mA
- High Input Impedance: 1012Ω
- Low Total Harmonic Distortion: ≤0.02%
- Low 1/f Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 μs

INTERNAL SCHEMATIC

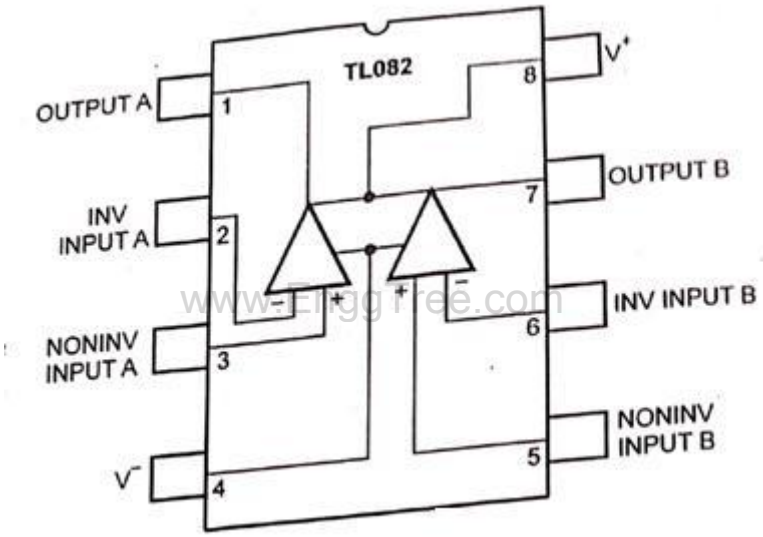


Figure 1.9.3 pin diagram of TL082

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-28]

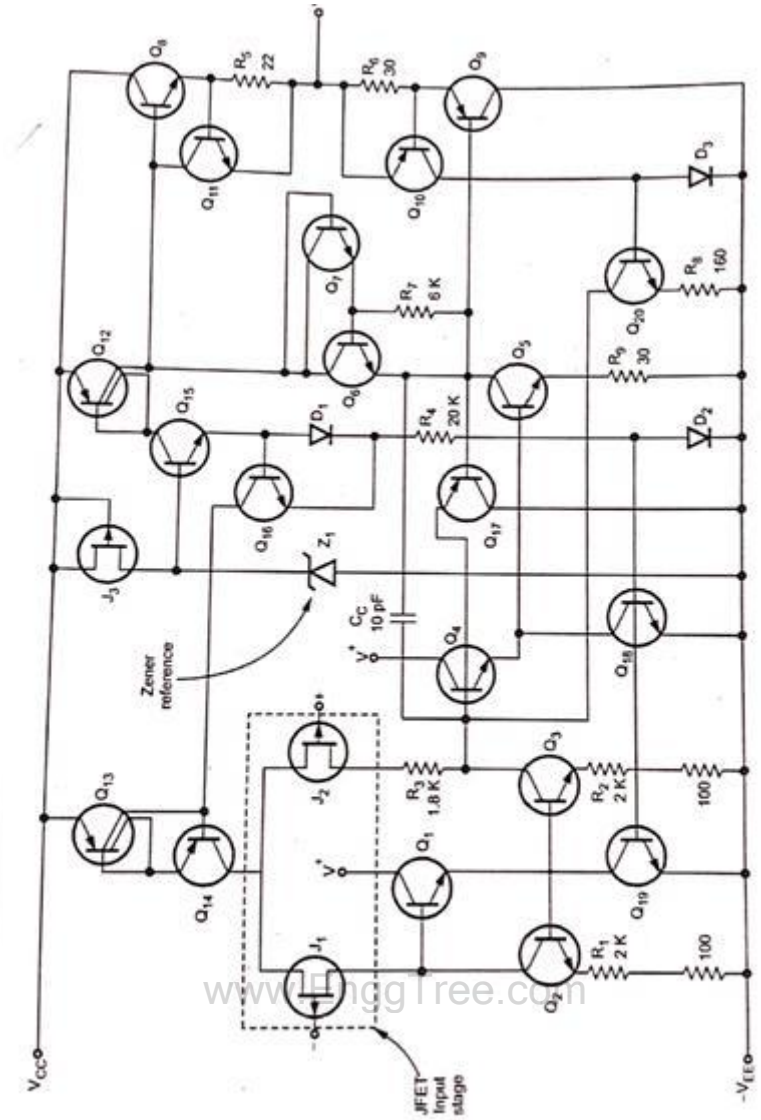


Figure 1.9.4 Internal Schematic of TL082

[source: "Linear Integrated Circuits, by U.A.Bakshi, A.P.Godse, Page-S-29]