UNIT-1

PN JUNCTION DEVICES.

PN Junction diode - structure, operation and V-I characteristics diffusion and Transition capacitance - Rectifiers - Half wave and Full wave Rectifier - Display devices - LED, Laser diode, Zener diode characteristics - Zener as Reverse characteristics Zener as Regulator.

SEMICONDUCTOR:

A semiconductor is a material which has electrical conductivity to a degree between that of metal (copper) and Insulator (Glass). Semiconductor are the foundation of modern electronics, LED, solar cells.

DIODE ⇒ Di + ode.

Di - Two.

ode - electrode.

Review of Intrinsic & Extrinsic Semiconductors.

INTRINSIC SEMICONDUCTOR:-

→ An Intrinsic semiconductor is one, which is pure enough that impurities do not appreciably affect its electrical behaviour.

EXTRINSIC SEMICONDUCTOR:-

→ It is one that has been doped with impurities to modify the number and type of free charge carriers That has been doped and giving electrical properties

Two Types of Extrinsic Semiconductor are

N-Type Semiconductor

P-Type semiconductor.

*N Type Semiconductor With larger electron Concentration than hole concentration are called N-Type semiconductor.

Ex: Arsenic

*P Type semiconductor have a larger hole concentration than electron concentration.

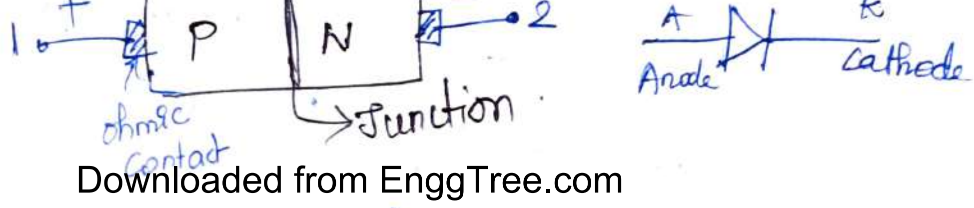
Ex: Gallium.

PN JUNCTION DIODE

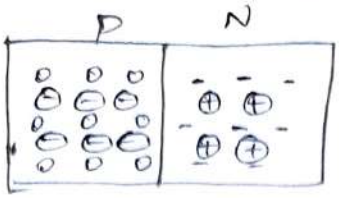
Introduction:-

*If we join a piece of p-type to a piece of N Type semiconductor such that the crystal structure continuous at the boundary, a PN Junction is formed. Such a PN Junction forms a very useful device and is called Semiconductor diode, PN Junction diode (or) crystal diode

*All semiconductor device contains atleast one PN Junction. therefore it has wide application in electron, and it is very important to know characteristics of PN Junction, when connected in electric circuits



FORMATION OF DEPLETION REGION :-



* P-region has holes (majority carrier) and negatively charged Impurity atoms called negative ions (acceptor atom).
* N-region has electrons (majority carrier) and positively charged impurity atoms called positive ions (donor atom) both are in equal numbers.
* In both regions the minority carriers are not shown in fig. In a PN Junction there exists a concentration gradient near the junction. There are large number of holes on P-side while very small no. of holes on n side near the junction. Thus holes starts moving p side to n side. i.e) higher concentration area towards lower concentration area.

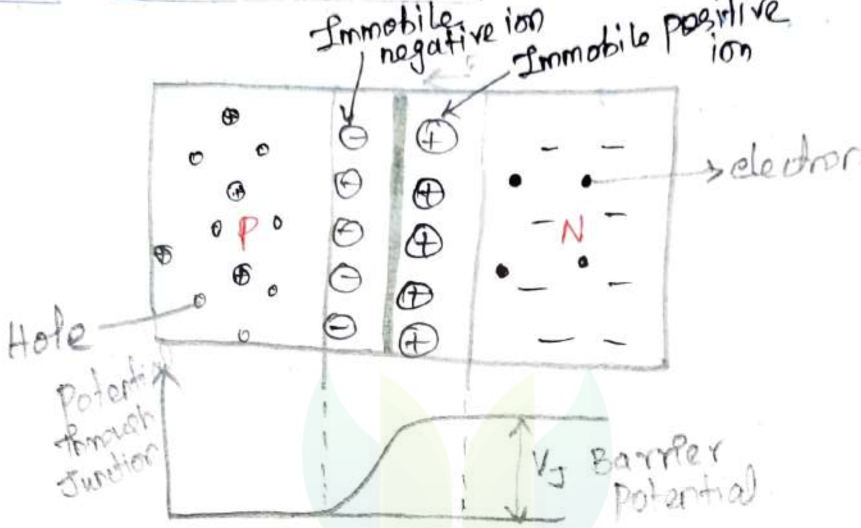
* So holes from pside to n side
 electrons from nside to pside

* In equilibrium condition, the region near the junction, there exists a wall of negative immobile charges on Pside and wall of positive immobile charges on n side. In this region, there are no mobile charge carriers. such a region is depleted of free mobile charge carriers and hence called depletion region (or) space charge region.

(*) So no further electron (or) holes can cross the junction. It act as barrier.

What is Barrier Potential:-

→ Due to immobile positive charges on n side and negative charges on p side exist an electric field across the junction. This creates the potential difference across the junction which is called barrier potential, junction potential, built in potential (or) cut in voltage.



Barrier potential for Si = 0.7V
Barrier potential for Ge = 0.3V

PN Diode ohmic contact:-

→ The contact between a metal and a heavily doped semiconductor is called ohmic contact.

Characteristics:-

i) It conducts current equally in both direction

ii) Drop across the contact is very small, which doesn't affect the performance of diode.

BIASING:-

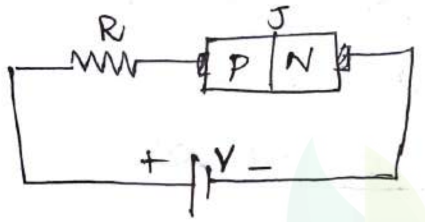
→ Applying external DC voltage to electric device is called Biasing.

1 FORWARD BIAS 2 REVERSE BIAS

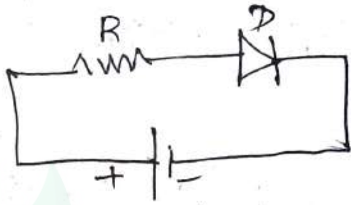
FORWARD BIASING OF PN JUNCTION DIODE :-

If an external DC voltage is connected in such a way that the p-region terminal is connected to (+) of DC voltage and n region is connected to the negative (−) region of DC voltage. This biasing condition is called "forward biasing"

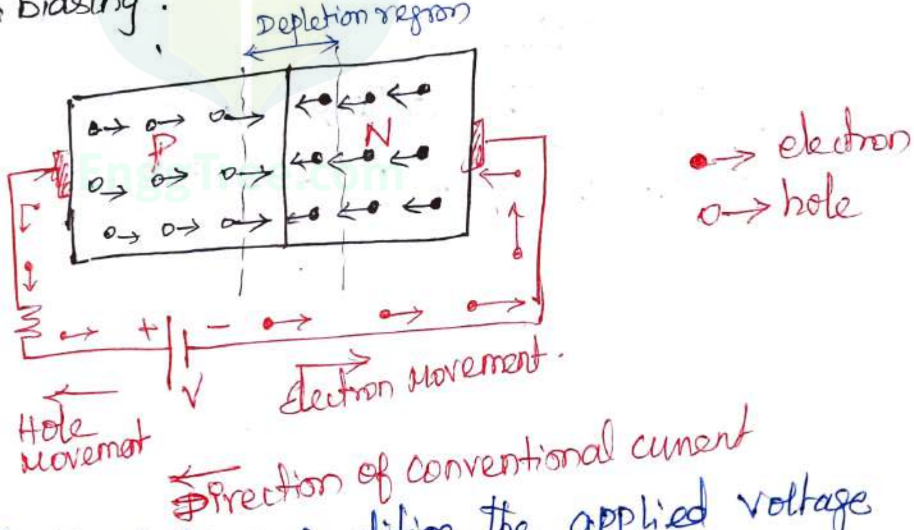
operation of forward biased diode :-



Forward biasing.



symbolic representation



→ Under the forward bias condition the applied voltage i.e) Positive potential repels the holes in P region towards the junction

→ Similarly the applied negative potential repels the electrons in n-region towards the junction

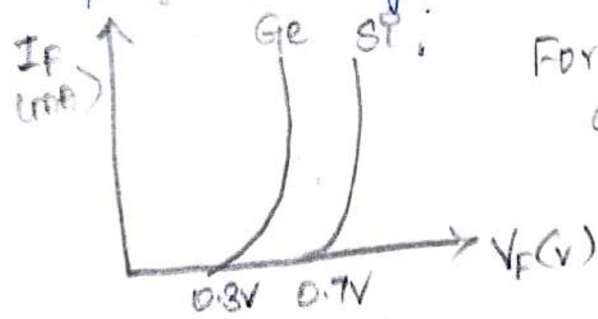
→ Due to this the number of negative ions in P-region and Positive ions in N-region decreases. Therefore width of depletion layer is reduced

→ If the applied voltage is more than barrier potential than the depletion region as well as the barrier field decreases and becomes narrow.

→ Hence the applied voltage is increased at a particular value of the depletion region becomes very much narrow after that disappears.

→ Such that large number of majority carrier can cross the junction because the junction resistance almost becomes zero. Therefore the forward current flow through the pn junction diode and becomes a conductor.

→ Direction of current flow from negative to positive of the battery, while the direction of conventional current is from positive to negative of battery.



Forward curve.

The polarities of voltage drop across the pn junction in forward biased condition are opposite to that of barrier potential. but the value is almost equal to barrier potential.

FORWARD RESISTANCE OF DIODE

i) Static forward Resistance

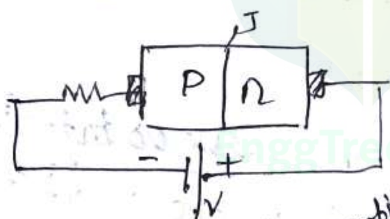
$$\boxed{R_f = \frac{\text{Forward DC voltage}}{\text{Forward DC current}}}$$

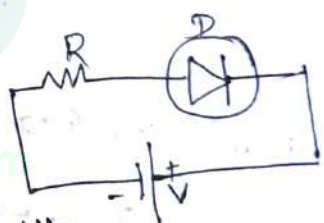
ii) Dynamic forward Resistance

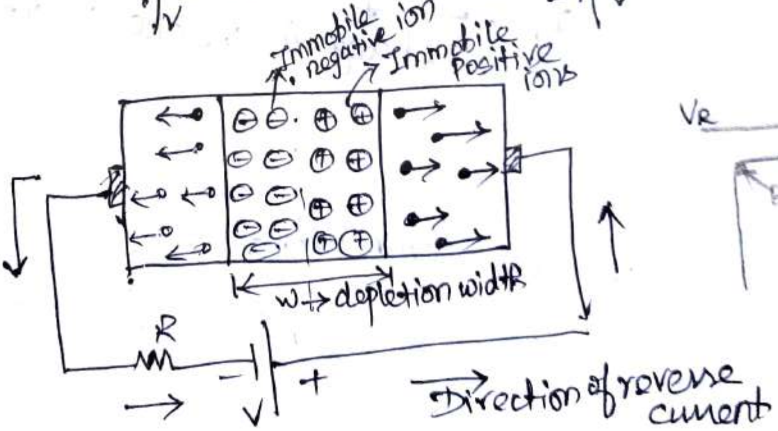
$$\boxed{r_f = \frac{\Delta V_f}{\Delta I_f}}$$

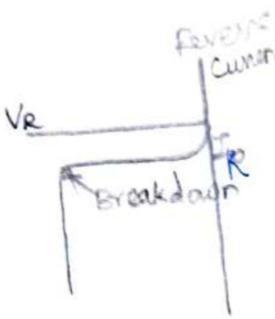
REVERSE BIASING OF PN JUNCTION DIODE

If an external DC voltage is connected in such a way that P-region terminal of P-n junction connected to negative of battery and n-region terminal of P-n connected to positive of battery. ⇒ REVERSE BIASING.









→ The reverse voltage across the diode is V_R while the current flowing is reverse current I_R flowing due to minority charge carrier.

→ The polarity of reverse voltage applied is opposite to that of forward voltage. The reverse saturation current is due to minority carriers and is opposite to forward current.

→ As the reverse voltage is increased, reverse current increases initially but after a certain voltage, the current remains constant equal to reverse saturation current I_0 through reverse voltage is increased where breakdown occurs and reverse current increases rapidly is called knee of reverse characteristics:-

Reverse Resistance of diode.

i) Static Resistance (DC)

$$R_r = \frac{\text{Applied reverse voltage}}{\text{Reverse saturation current}}$$

ii) Dynamic Resistance:(AC)

$$r_r = \frac{\text{change in reverse voltage (V)}}{\text{change in reverse current (I)}} \Rightarrow \frac{\Delta V_R}{\Delta I_R}$$

EFFECT OF TEMPERATURE ON PN JUNCTION DIODE.

→ As the temperature increases the generation of electron hole pairs in semiconductors increases their conductivity.

→ Thus the current through PN junction diode increases with temperature as given by diode current equation,

$$\boxed{I = I_0 \left[e^{V/\eta V_T} - 1 \right]}$$

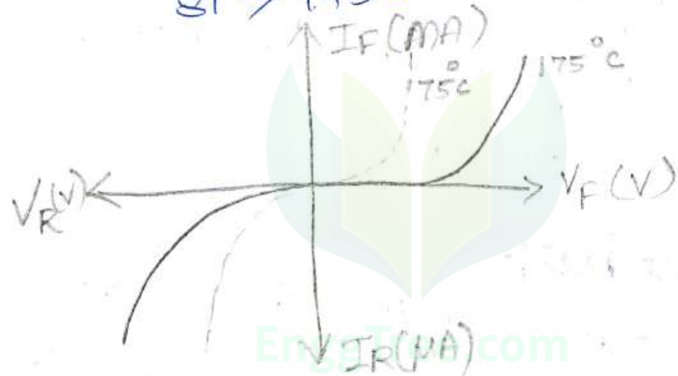
→ The reverse saturation current (I_o) of diode increases 7%/°c for both Germanium & silicon

→ The Reverse saturation current I_o of diode doubles for every 10°c rise in Temperature.

→ Thus the Temperature increases at fixed voltage, current also Increases

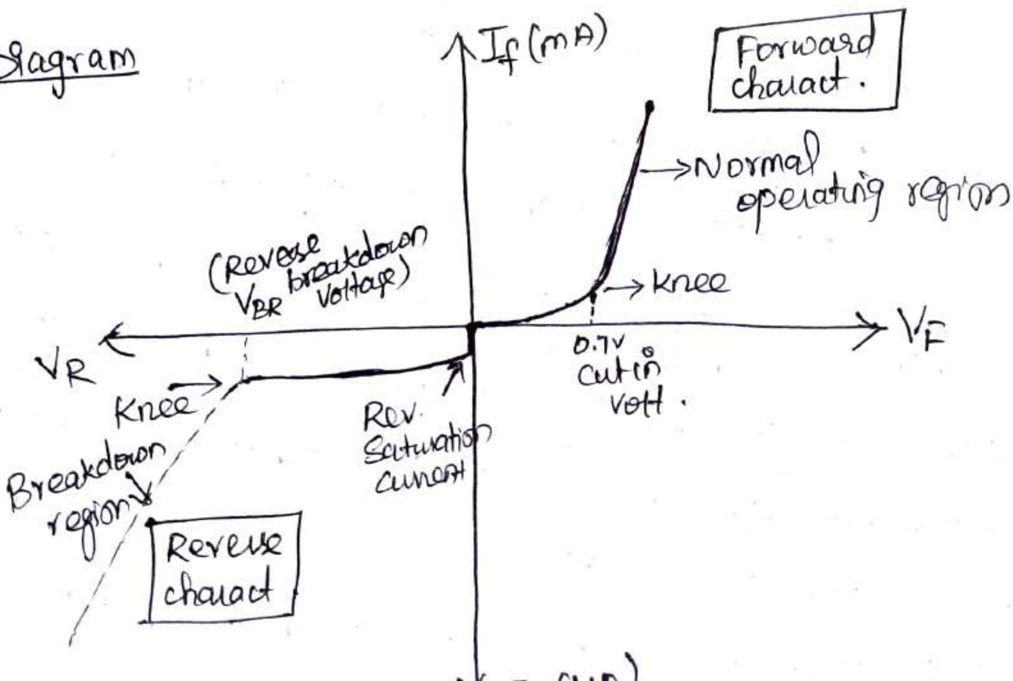
→ The barrier voltage is Temperature dependent and it decreases by 2mv/°c for both Si & Ge

Ge ⇒ 75°C
Si ⇒ 175°C



VI characteristics of PN Diode [N/D '15]

Diagram



Under forward bias:-

→ In forward bias condition when the forward voltage V_F increased, but V_F is less than barrier potential V_b.

→ Thus forward current I_F is almost zero because the barrier potential prevents the recombination of holes in P-region and electrons in N-region.

→ when forward bias voltage V_F is greater than V_b the barrier potential at junction disappears and thus e^- from N region and holes from P-region cross the junction and large current produced.

Cutin voltage / Threshold voltage	Si = 0.7 Ge = 0.3

Under Reverse bias:-

→ In Reverse bias condition the current is depending only on minority charge carriers and it depends only on Thermal energy.

→ The Thermally generated holes and electrons cross the N and P-region and a small current produced called Reverse Saturation Current. It depends only on Temperature

→ when we apply large reverse bias, the electrons will acquire enough energy to release other electrons from semiconductor. These e^- release other e^- thus produce large reverse current.

→ This Reverse voltage at which the junction break down is called breakdown voltage.

DIODE CURRENT EQUATION:- [VI characteristics derivation]

→ The mathematical representation of VI characteristic of diode is VI charact. equation or diode current equation

P_p = Hole concentration in p type at edge of depletion region

n_n = Electron concentration in n type at edge of depletion

P_n = Hole concentration in n type at edge of depletion

n_p = Electron concentration in p type at edge of depletion

Case i:-

Under unbiased cdn, holes move from p side to N side

$$P_p = P_n \cdot e^{V_J/V_T} \longrightarrow (1)$$

V_J → Barrier potential or Junction Potential

$$P_{p_0} = P_n(0)\, e^{(V_J - V)/V_T} \longrightarrow (2)$$

As holes cross the junction, this concentration becomes $P_n(0)$ which is concentration of holes on n side just near the junction. & V_J becomes $V_J - V$.

Unbiased PN diode $\boxed{V=0}$.

$$P_{p_0} = P_{n_0} e^{V_J/V_T} \longrightarrow (3)$$

P_{n0} → concentration of holes on n side.

equating (2) & (3).

$$P_n(0)\, e^{V_J - V/V_T} = P_{n_0} e^{V_J/V_T}$$

ie, $P_n(0) = P_{n_0} e^{V/V_T} \longrightarrow (4)$.

Case (ii)

Thus, $n_p(0) = n_{p_0} e^{V/V_T} \longrightarrow (5)$

$$P_n(0) = P_n(0) - P_{n_0} \longrightarrow (6)$$

$$P_n(0) = P_{n_0} e^{V/V_T} - P_{n_0}$$

$$\boxed{P_n(0) = P_{n_0}(e^{V/V_T} - 1) \longrightarrow (7)}$$

$$N_p(0) = n_{p_0}(e^{V/V_T} - 1) \longrightarrow (8)$$

Case :3

Hole current from p side to n side,

$$I_{pn}(0) = \frac{Aq D_p P_n(0)}{L_p} \longrightarrow (9)$$

Electron current from n side to P side,

$$I_{np}(0) = \frac{Aq D_n N_p(0)}{L_n} \longrightarrow (10)$$

$A \rightarrow$ Area of junction
$D_p \rightarrow$ Diffusion constant for holes
$D_n \rightarrow$ Diffusion Constant for electrons
$L_n \rightarrow$ length of e^-
$L_p \rightarrow$ length of holes

Adding (9) & (10)

$$I = I_{pn}(0) + I_{np}(0)$$

$$= \underbrace{\left[\frac{Aq D_p P_n(0)}{L_p} + \frac{Aq D_n n_{po}}{L_n}\right]}_{I_0} (e^{V/V_T} - 1)$$

$$\boxed{I = I_0 (e^{V/V_T} - 1)}$$

$I_0 \rightarrow$ Reverse saturation Current

$$I = I_0 \left[e^{V/\eta V_T} - 1\right].$$

$\eta = 1$ Ge diode $= 2$ Si diode.	Identity factor

$V_T \rightarrow$ Voltage equivalent of Temperature

$$\boxed{V_T = KT} \longrightarrow (I)$$

K – Boltzman constant (8.625×10^{-5} eV/k)

$$V_T = \frac{T}{1/K} = \frac{T}{\frac{1}{8.625 \times 10^{-5}}} = \frac{T}{11600}$$

if $T = 300k$ $\boxed{V_T = 26mV}$

Unbias:-

$V=0,$

$I=I_0(e^0-1)=0\,Amp$

Forward bias

V is +ve. & I is +ve.

$I=I_0(e^{V/\eta V_T}-1)\,Amp.$

Reverse Bias.

V is -ve & I is also -ve

$I=I_0(e^{-V/\eta V_T}-1)\,Amps$

~~ZENER~~ DIODE:- CONDUCTIVITY OF SEMICONDUCTOR.

→ In a pure semiconductor no. of holes = no. of electrons

→ Each $\bar{e}$ hole pair creates two charge carrying particles

→ one is free $\bar{e}$ with -ve polarity mobility μ_n & holes μ_p

Total current density $\boxed{J=J_n+J_p}$

$J=qn\mu_nE+qp\mu_pE$

$=qE[n\mu_n+p\mu_p].$

$\sigma=[n\mu_n+p\mu_p]q.$

$\boxed{J=\sigma E}$

σ → conductivity.

J_n → $\bar{e}$ drift current density

J_p → hole drift current density.

n → no. of $\bar{e}$, p → no. of holes.

E → Applied Electric field

q → charge of $\bar{e}$ & holes.

Advantage of PN Diode.

1. Long life.
2. used as on-off switch
3. Compact & Portable.
4. cheap & Reliable

Disadvantages.

1) Noise level is high.
2) Temperature sensitive
3) Delay in switching is more.

Applications

1. In Voltage multiplier circuit
2. In Rectifier
3. In clipper and clamper circuit.

ZENER DIODE:

Introduction:-

→ The zener diode is a silicon PN junction semiconductor diode which is also operated in reverse breakdown region.

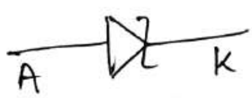
→ when a junction is reverse biased there is only a very small reverse saturation current

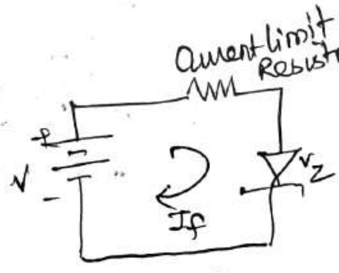
→ when the reverse voltage is sufficiently increased the junction breaks down and large reverse current flows.

→ If the reverse current is limited by means of suitable series connected resistor. The power dissipation in the device can be kept to a level that will not destroy the device.

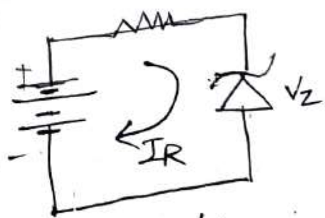
→ The zener diode have breakdown voltage range from 3V to 200V.

Symbol.





Forward



Reverse bias

Operation:

→ In forward biased condition, the normal Rectifier diode and the zener diode operate similar.

→ But the zener diode designed to be operated in reverse biased condition.

→ In reverse bias condition the diode carries reverse saturation current till the reverse voltage less than reverse breakdown voltage. when the reverse voltage exceeds reverse breakdown voltage, the current through it changes drastically but the voltage across it remains almost constant.

→ The change in low value to large value of current is very sharp and it is called Zener knee curve.

→ The reverse bias at which breakdown occur is called Zener breakdown voltage.

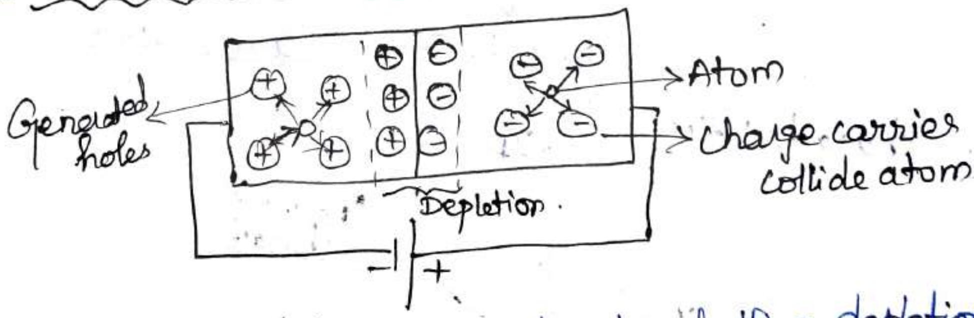
BREAKDOWN MECHANISM IN ZENER:-

i) Zener breakdown.

ii) Avalanche breakdown.

The reverse saturation current is not depend on applied Voltage.

ZENER BREAKDOWN EFFECT:-



i) when pn junction is heavily doped then depletion region is narrow, So under reverse bias condition, the electric field across depletion region very intense.

ii) The high intensity electric field causes electrons to breakdown away from atoms converting depletion region from insulating to conducting material.

iii) It occurs when reverse bias voltage is <4V

AVALANCHE EFFECT:-

→ It occurs in wide depletion region

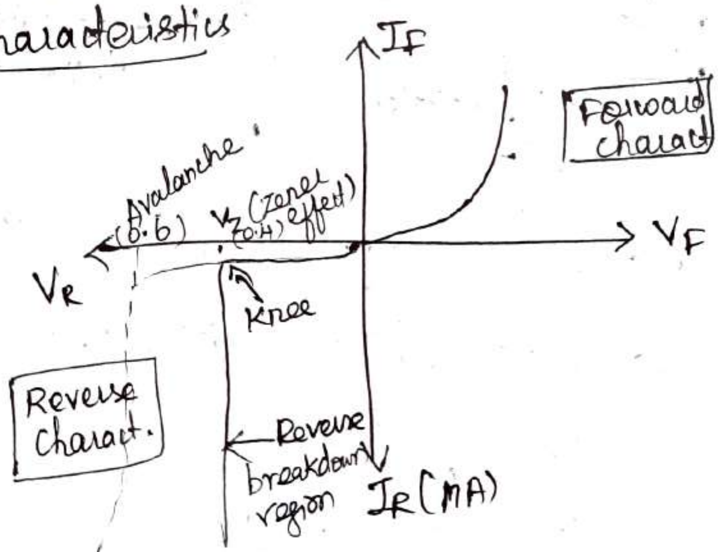
→ It occurs when reverse bias voltage is more than 6V

→ In reverse bias condition, the diode carries reverse saturation current till the reverse voltage applied is less than reverse breakdown voltage.

→ The electrons released by light doping of impurities and it collide with other atoms to produce free electrons is an avalanche effect.

→ As reverse voltage increases minority carrier get accelerated and strikes the atoms hence more and more minority carrier generated. This is called "Carrier multiplication (or) Impact Ionization". Hence large number of minority carrier give rise to very high reverse current. It is called avalanche effect.

VI characteristics



Application:
1. As a voltage regulating element in voltage regulator
2. In various protection circuit
3. In zener limiters & clipping circuits

Specification of Zener diode:-

i) Nominal Zener voltage V_Z (or) V_{ZT} [Tolerance ±10%.]

ii) Zener current I_Z

iii) Maximum Zener Current & Minimum Zener current I_{Zmin} & I_{Zmax}.

iv) Maximum Power dissipation.

Application:-

i) As voltage Regulator

ii) As used in Protection circuits

iii) clipping circuits & wave shapper circuit

ZENER DIODE ACT AS VOLTAGE REGULATOR:-

→ The most important application of zener diode is in DC voltage Regulator circuit

→ The Zener diode under reverse bias condition the current through the diode is very small in order of few μA upto certain limit.

→ when the sufficient reverse bias is applied, electrical breakdown of Zener diode occur.

→ The large amount of current flows through the zener diode. Such a breakdown occurs at Zener voltage (V_Z)

→ Under this condition the voltage across the Zener diode is Constant and equal to V_Z.

→ The large current due to breakdown is limited by connecting the resistance in circuit.

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→ Under this condition the voltage across the Zener is constant and equal to V_Z.

→ The large amount of current due to breakdown is limited by connecting the resistance in circuit.

→ As the voltage across the Zener diode remains constant V_Z is connected across load and hence load voltage (V_o) equals to Zener voltage V_Z. Thus the zener diode act as ideal voltage source which maintains a constant load voltage independent of current

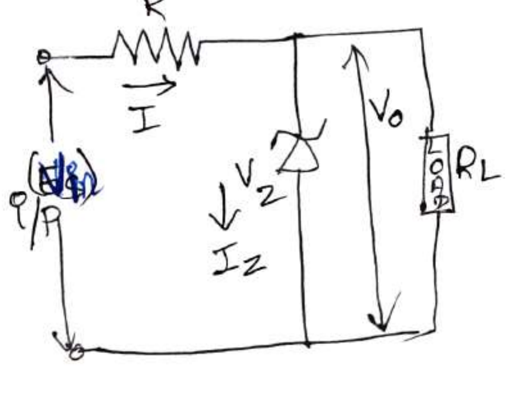
Case (i)

Taking R_L = Constant

V_{in} = Vary

$$I_L = \frac{V_o}{R_L} = \frac{V_F}{R_L}$$

Since $\boxed{V_o = V_F}$



Current $I = I_Z + I_L$

→ As $V_{in}\uparrow$, $I\uparrow$. But I_L is constant & R_L is constant

→ Zener current I_Z should increase between I_{Zmin} & I_{Zmax} and I increases.

→ As $V_{in}\downarrow$, $I\downarrow$, I_L is constant

→ So I_Z should decrease from I_{Zmin} to I_{Zmax}. $I\downarrow$.

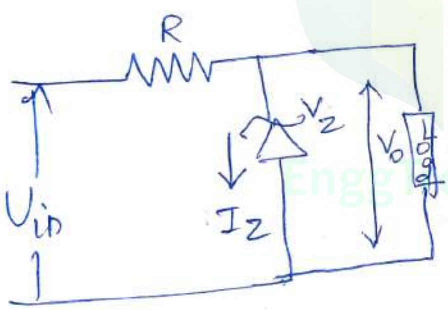
Case(ii)

Taking R_L as varying & V_{in} constant,

$$\boxed{I = \frac{V_{in} - V_Z}{R_L}} \qquad I_Z + I_L = I.$$

→ To make current as constant, then R_L increases or decreases I_Z should be increased.

→ when I_L is decreased and I_Z should be decreased



DRIFT CURRENT :-

→ when an electric field is applied across a semiconductor material, the charge carriers attain a certain drift velocity Vd which is equal to the product of the mobility of the charge carriers and applied electric field intensity E

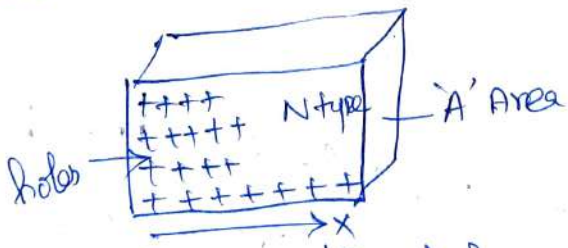
→ The holes move towards -Ve Terminal of battery and electrons move towards +Ve Terminal of battery. This combined movement of charge carriers constitute current known as Drift current

$$\boxed{\begin{aligned} J_n &= qn\mu_n E \\ J_p &= qn\mu_p E \end{aligned}}$$

DIFFUSION CURRENT :-

→ If a concentration gradient exist in a semiconductor then it is possible for an electric current to flow even in the absence of applied voltage.

→ In a semiconductor material, the charge carrier have the tendency to move from the region of higher concentration to lower concentration. This movement is called Diffusion Current.



$$J_p = -qD_p \frac{dp}{dx} \ A/cm^2 .$$

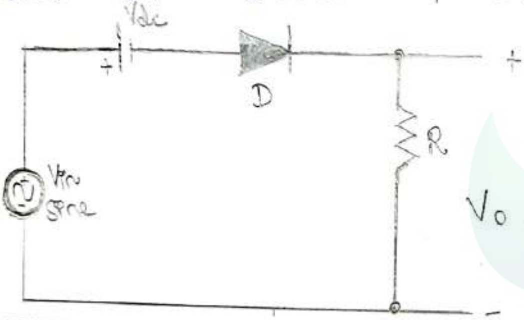
$$J_n = qD_n \frac{dn}{dx} \ A/cm^2 .$$

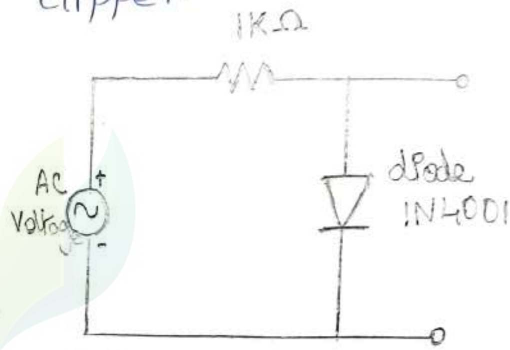
Clippers circuits:

The circuit which are used to clip off unwanted portions of the waveform without distrubing the remaining part of the waveform are called clipper's or clipper circuit or slicers

Eg: Half wave Rectifier.

When a diode is connected in series with the load such ckt are called series clipper. When the diode is connected in parallel or branch to the load, such ckt are called parallel clipper.



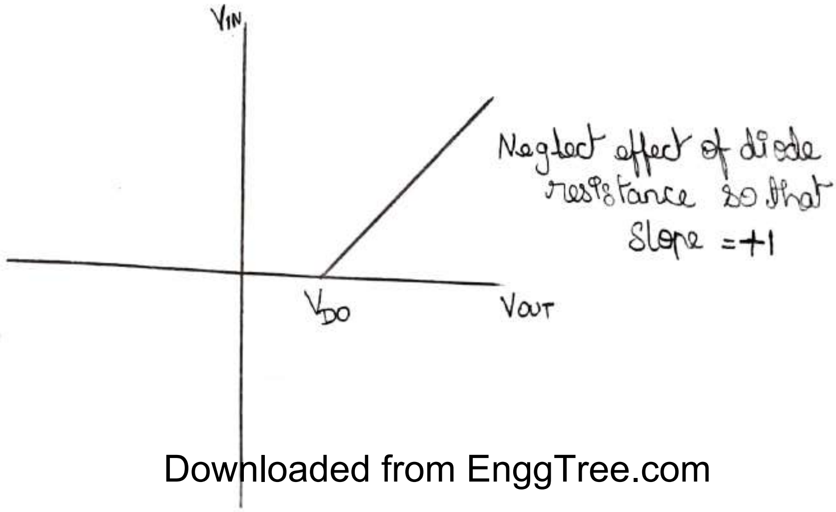


Transfer characteristics: ~~Transfer~~

Plots the output against input.

→ The graph of O/P variable against I/P variable of the circuit is called Transfer chara

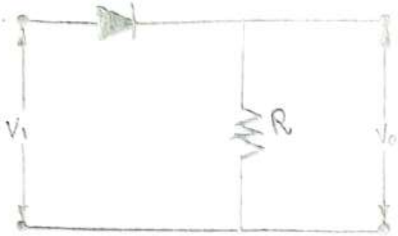
→ Here we use V_o (O/P voltage) V_s V_i (I/P Voltage

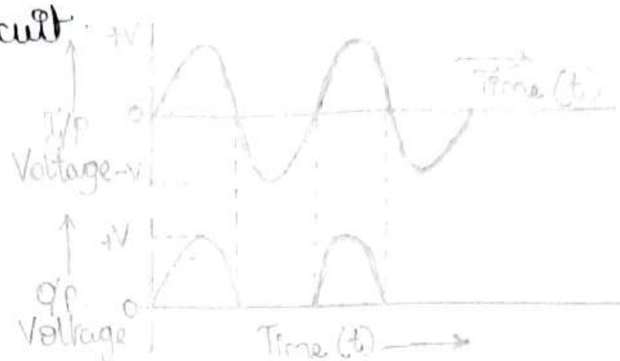


Clipper Types:

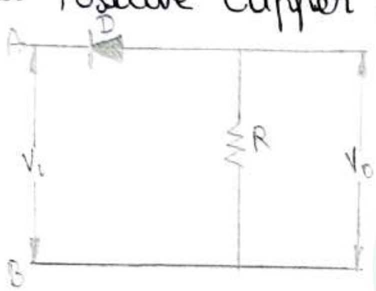
1. Series clippers
2. Parallel clippers

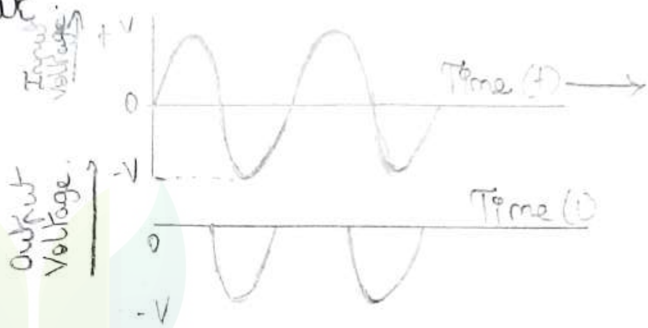
Series negative clippers circuit



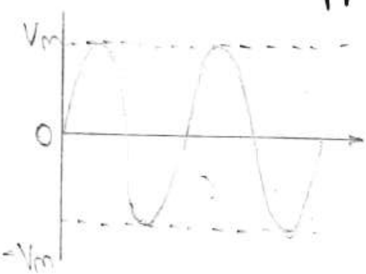


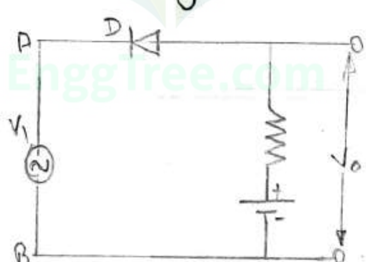
Series Positive Clipper Circuit



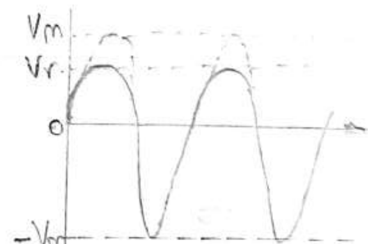


Series Positive clipper above voltage VR



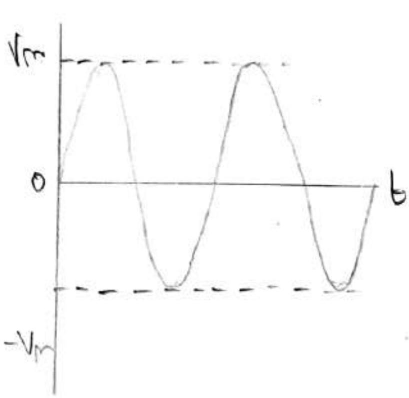


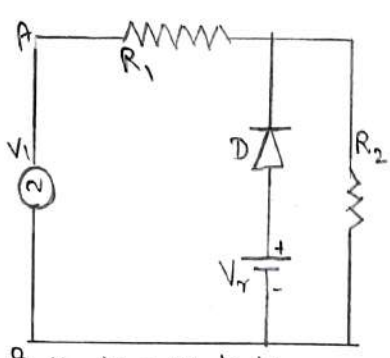
Positive Series Clipper with positive V_r



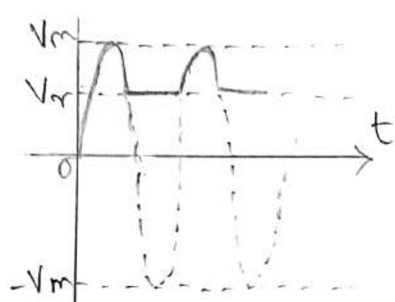
Practical Output Waveform

Negative Shunt Clipper with positive VR





Negative Shunt clipper with positive V_r



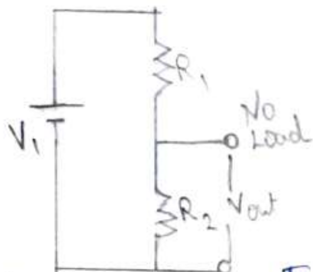
practical Output Waveform

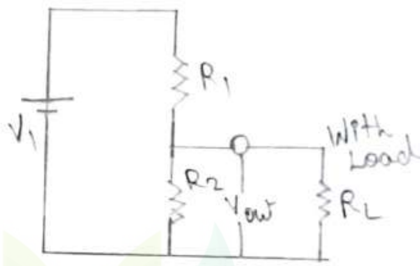
Parallel Clippers:

→ Here the diode is connected across the load terminals. It can be used to clip or limit the +ve or −ve part of the I/P signal as per the requirement.

→ Here we uses a R_1 resistance for controlling the current in the circuit.

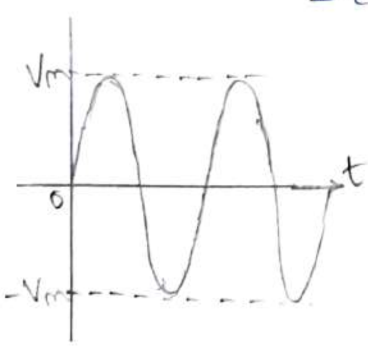
→ Using potential divider rule we get,

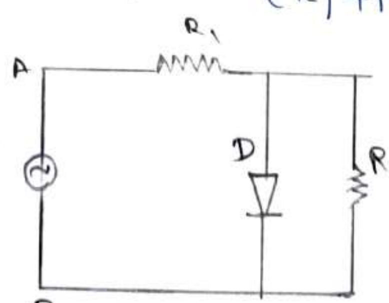




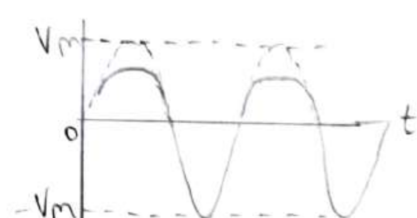
$$V_{out} = V_1 \frac{IR_2}{I(R_1+R_2)} = \frac{V_1 R_2}{(R_1+R_2)}$$

$$V_{out} = V_1 \frac{IR_2}{I(R_1+R_2)} = \frac{V_1 (R_2 || R_L)}{(R_1 + R_2 || R_L)}$$



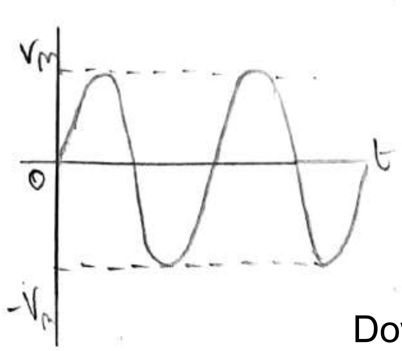


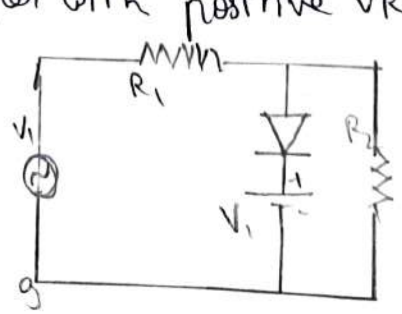
Positive Shunt Clipper

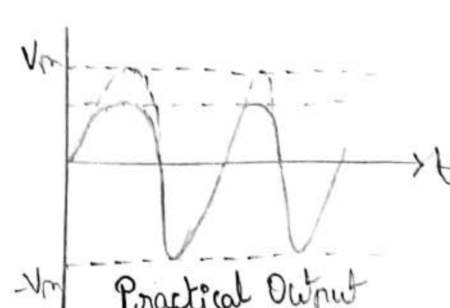


Practical Output Waveform.

Positive Shunt Clipper with positive VR.

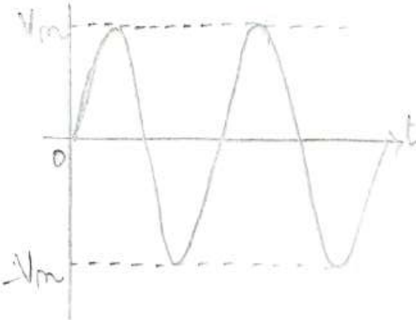


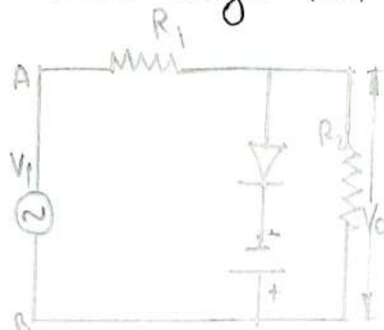




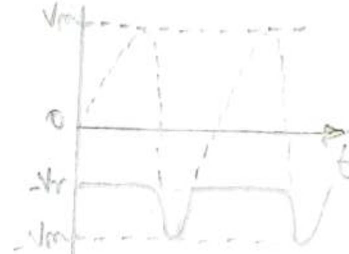
Practical Output Waveform

Positive Shunt Clipper with negative:



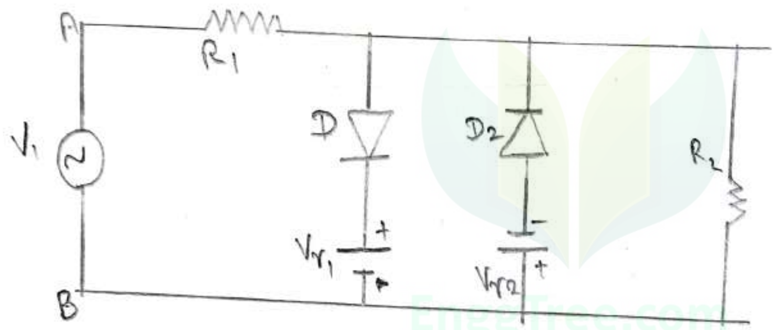


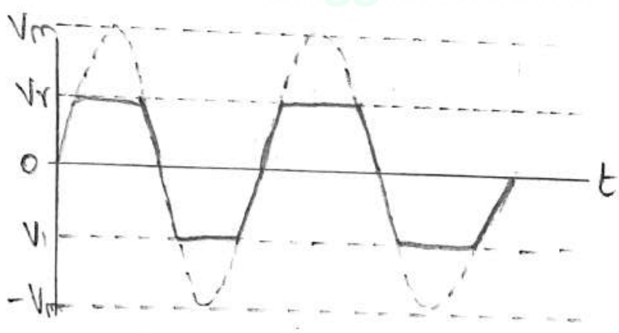
Positive Shunt clipper with negative V_r



Practical Output Wave form.

Two-way Clipper:





Output Waveform

Clamper Circuits:

They are used to add a DC level as per the requirements to the AC output signal.

→ The capacitor, diode and resistance are the three basic elements of a clamper circuit.

→ Also called DC Restorer or DC inserter circuits.

→ Depending upon the shift +ve and -ve clampers are clampers are classified as negative clampers and positive clampers.

Positive clamper circuit:

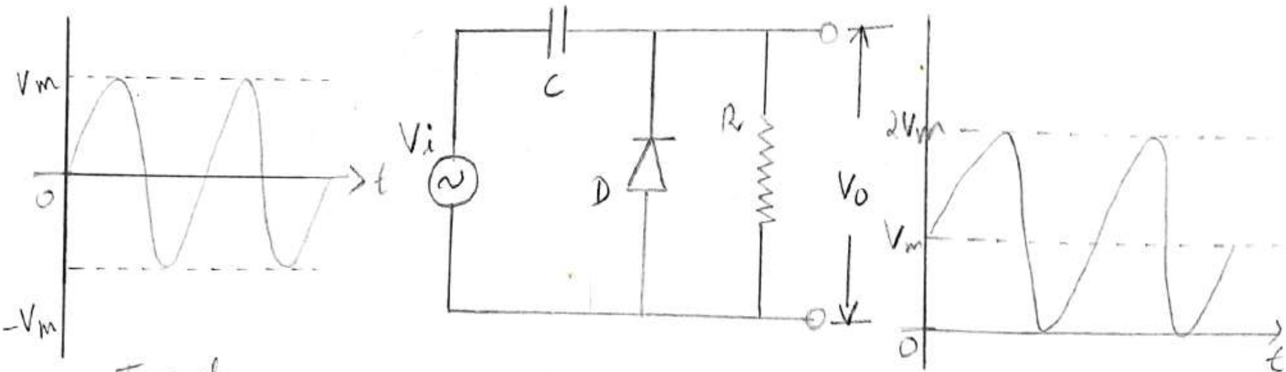
→ shifts the output signal to the positive portion of the input signal.

→ Initially, when the input is given, the capacitor is not yet charged and the diode is reverse biased. The output is not considered at this point of time.

→ During the -ve half cycle, at the peak value, the capacitor gets charged with negative on one plate and positive on other.

→ During next +ve half cycle, the capacitor is charged to positive V_m while the diode gets reverse biased and gets open circuited.

→ $V_0 = V_i + V_m$



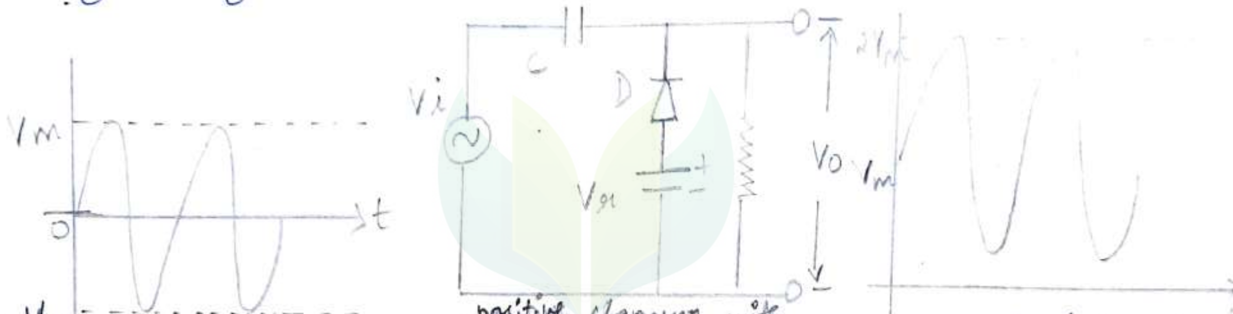
Input waveform

output waveform

Positive clamper with positive V_r.

→ During the positive half cycle, reference voltage is applied through diode at output and as input voltage increases, the cathode voltage of the diode increases with respect to anode voltage and hence it stops conducting.

→ During the negative half cycle, diode gets forward biases and starts conducting. The voltage across the capacitor and the reference voltage together maintain the output voltage level.

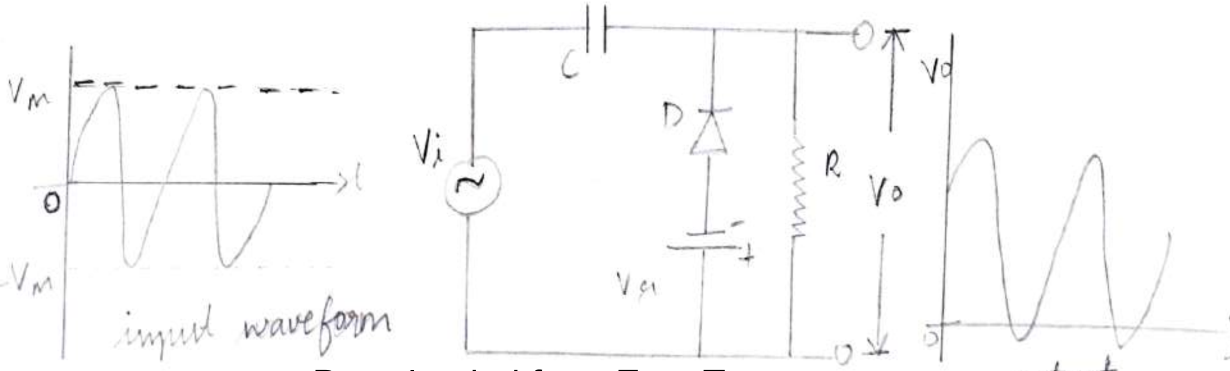


input waveform · positive clamper with positive reference Vr · output waveform

Positive clamper with negative V_r.

→ During the positive half cycle, the voltage across the capacitor and the reference voltage together to maintain output voltage level.

→ During the negative half-cyle the diode conducts when the cathode voltage gets less than the anode voltage.



input waveform · output waveform

Negative clamper:

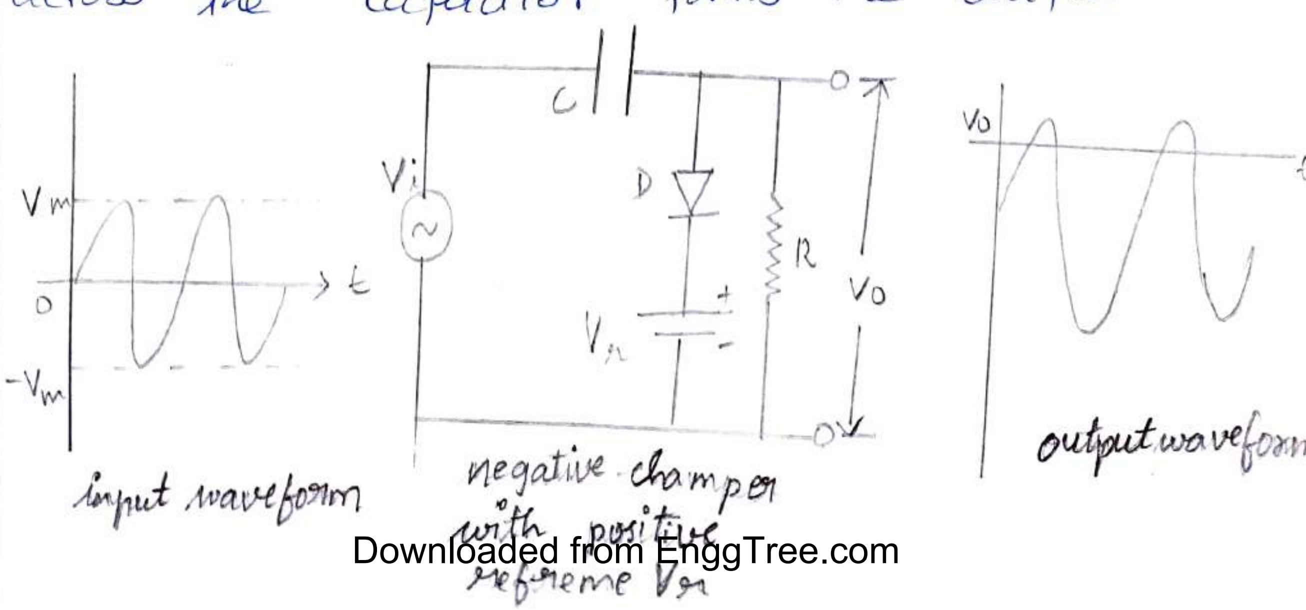
→ During the positive half cycle, the capacitor gets charged to its peak value V_m. The diode is forward biased and conducts.

→ During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be $V_0 = V_i + V_m$.

Negative clamper with positive V_r.

→ During the positive half-cycle, the diode conducts, but the output equals the positive reference voltage applied.

→ During the negative half-cycle, the diode acts as open circuited and the voltage across the capacitor forms the output.

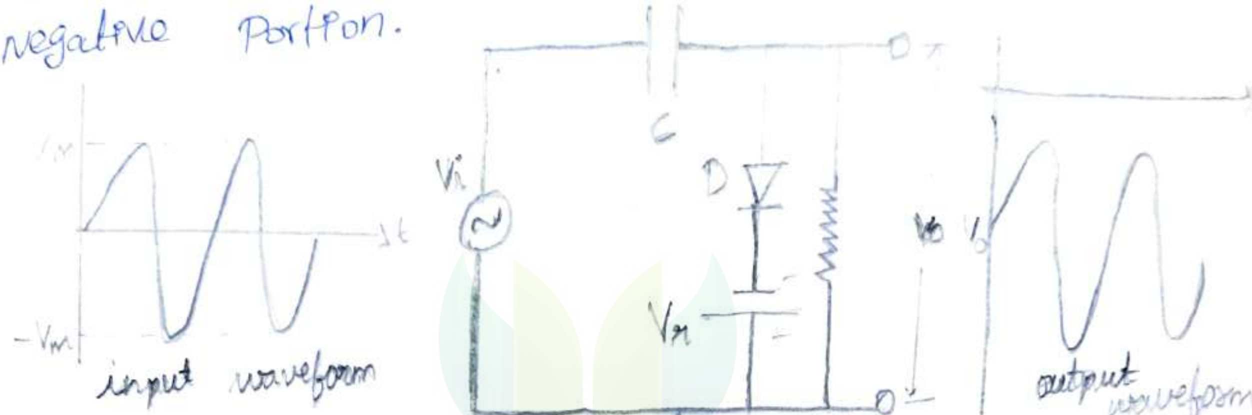


Negative clamper with negative V_r

→ The cathode of the diode is connected with a negative reference voltage.

→ During positive half cycle before the zero voltage level.

→ During the negative half cycle, the voltage across the capacitor appears at the output. thus the waveform is clamped towards the negative portion.



negative clamper with negative reference V_r

Applications:

They are many applications for both clippers and clampers such as.

Clippers:

1. used in FM transmitters
2. used in television circuits
3. used as voltage limiters.
4. used for amplitude restorers
5. used for Protection of circuits for spikes.
6. used for generation and Shaping of waveforms.

Clampers:

1. used as direct current restorers.
2. used to remove distortions.
3. used as voltage multipliers.
4. used as test equipment.
5. used as base-line stabilizer.
6. used for the protection of amplifiers.

RECTIFIER:

Rectifier is an electronic device or circuit which converts alternating voltage or current into unidirectional DC voltage or current.

There are 2 types of Rectifier

i) Halfwave Rectifier

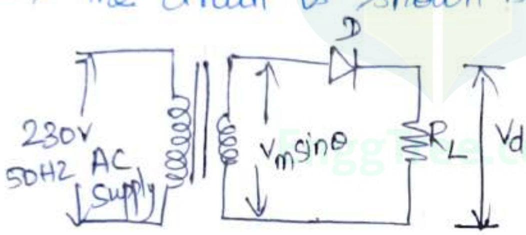
ii) Full wave Rectifier

- → center Tapped Transformer Rectifier
- → Bridge Rectifier

Half wave Rectifier:-

→ The half wave rectifier delivers power to load only during one half cycle of AC supply voltage.

→ The circuit is shown below



Construction:-

→ The half wave rectifier consist of a stepdown transformer which reduced the AC supply to required value. The diode D conducts and convert AC to DC.

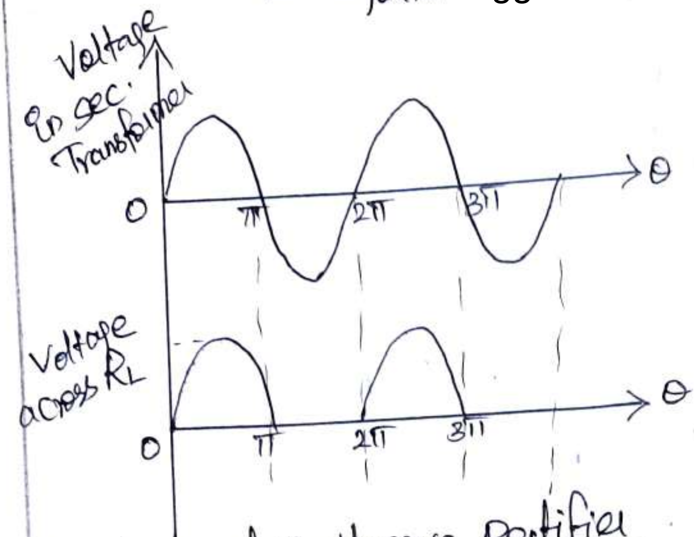
Operation:-

→ During Positive +Ve half cycle of i/p AC supply, the diode D is forward bias. So current flows through R_L.

→ During Negative half cycle of input AC supply, the diode D is reverse biased. So no current flows to RL.

→ Since rectifier deliver power to load only during one half cycle of AC supply voltage. It is called Half wave rectifier.

Waveform



Analysis of Halfwave Rectifier

The performance of Halfwave rectifier is analyzed from the following.

1) DC Load voltage
2) DC Load current
3) RMS load voltage
4) RMS load current
5) Ripple factor
6) Rectification Efficiency
7) Transformer Utility factor.
8) Regulation.
9) Peak Inverse voltage (PIV)

1) DC Load Voltage.

The average DC value of Load voltage is,

$$V_{dc} = \frac{\text{Area under Curve over full cycle}}{\text{Base (period)}}$$

$$V_{dc} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin\theta \, d\theta + \int_{\pi}^{2\pi} \cancel{V_m \sin\theta \, d\theta}\right]$$

(0)

$$= \frac{V_m}{2\pi}\left[-\cos\theta\right]_0^{\pi}$$

$$= \frac{V_m}{2\pi}\left[-\cos\pi - (-\cos 0)\right] = \frac{2V_m}{2\pi}$$

$$\boxed{V_{dc} = \frac{V_m}{\pi}}$$

2) DC Load current (I_{dc})

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi R_L} = \frac{I_m}{R_L}.$$

where $\frac{V_m}{R_L} = I_m$ & $I_m = \frac{V_m}{R_s + R_f + R_L}$

$R_s \rightarrow$ Transformer Secondary Resistance.
$R_f \rightarrow$ Diode forward Resistance
$R_L \rightarrow$ Load Resistance

3) RMS value of Load Voltage (V_{rms})

$$V_{rms} = \sqrt{\frac{\text{Area under the squared value}}{\text{Base}}}$$

$$= \sqrt{\frac{\int_0^{\pi} V_m^2 \sin^2\theta \, d\theta}{2\pi}}$$

$$= \sqrt{\frac{V_m^2}{2\pi}\int_0^{\pi}\left[\frac{1-\cos 2\theta}{2}\right] d\theta}.$$

$$= \sqrt{\frac{V_m^2}{4\pi}\left[\theta - \frac{\sin 2\theta}{2}\right]_0^{\pi}}$$

$$= \frac{V_m}{2}\sqrt{\frac{1}{\pi}\left[\pi - \frac{\sin 2\pi}{2}\right]}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

4) RMS value of Load current

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{2R_L} = \frac{I_m}{2}.$$

5) Ripple Factor (γ)

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

Ratio of RMS value of AC component to DC component in o/p is called Ripple factor.

$$\gamma = \sqrt{\left(\frac{V_m/2}{V_m/\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m^2}{4} \times \frac{\pi^2}{V_m^2}\right) - 1} \quad \gamma = \sqrt{\frac{\pi^2}{4} - 1} \Rightarrow \boxed{\gamma = 1.21}$$

6) **% Rectification efficiency η**

The ratio of DC o/p Power to AC i/p Power is AC i/p Power is called Rectifier efficiency η.

$$\eta = \frac{\text{DC o/p Power}}{\text{AC i/p Power}} = \frac{P_{dc}}{P_{AC}}$$

$$\eta = \frac{\frac{V_{dc}^2}{R_L}}{\frac{V_{rms}^2}{R_L}} \Rightarrow \frac{\frac{V_m^2}{\pi^2}}{\frac{V_m^2}{4}} = \frac{4}{\pi^2} \times 100$$

$$\boxed{\eta = 40.6\%}$$

7) **Transformer Utilization Factor (TUF)**

$$TUF = \frac{\text{DC Power delivered to Load}}{\text{AC Power rating of Transformer Secondary}}$$

$$= \frac{P_{dc}}{P_{AC\ rating}} \Rightarrow \frac{V_{dc}^2 / R_L}{V_{rms(rating)}\, I_{rms}}$$

$$V_{rms} \to \frac{V_m}{\sqrt{2}}$$

$$= \frac{\frac{V_m^2}{\pi^2 R_L}}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2}} \Rightarrow \frac{\frac{V_m^2}{\pi^2 R_L}}{\frac{V_m}{\sqrt{2}} \frac{V_m}{2R_L}} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

$$\boxed{TUF = 28.7\%}$$

8) **Regulation:-**

Regulation is the ratio of voltage drop to full load Voltage.

$$\text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}}$$

$$\%\ \text{Regulation} = \frac{R_f + R_s}{R_L} \times 100$$

9) **PIV:-** The maximum reverse voltage that diode can withstand without breaking down is Peak Inverse Voltage.

$$\boxed{PIV = V_m}$$

10) Form factor = $\frac{\text{RMS value of o/p voltage}}{\text{Average DC component o/p voltage}}$

$$= \frac{V_m/2}{V_m/\pi} = \pi/2 = \boxed{1.57}$$

11) Peak factor :- = $\frac{\text{Peak value}}{\text{RMS value}}$

$$= \frac{V_m}{V_m/2} = 2$$

Advantage :-

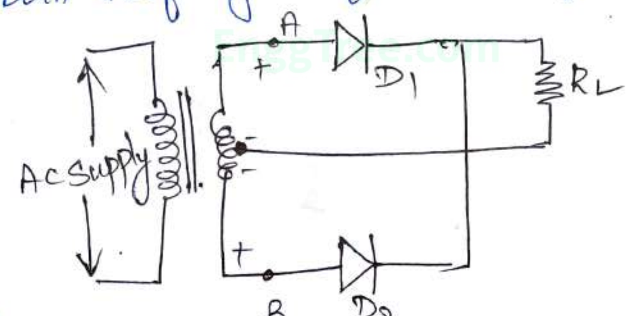
1) Simple circuit
2) Less cost

Disadvantage

1) Ripple factor is high.
2) Efficiency is Low.
3) Large filters required.

FULL WAVE RECTIFIER :-

→ The full wave Rectifier delivers power to load during both half cycles of Ac supply voltage.

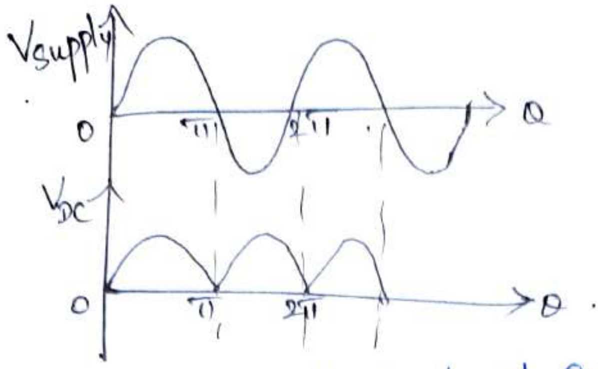


Construction :-

The full wave rectifier consist of center tapped step down Transformer which decreases Ac supply to the required value. The diode D_1 & D_2 converts Ac to DC voltage. The o/p is measured across R_L (Load Resistor)

Operation :-

→ During positive half cycle of i/p Ac supply the diode D_1 is forward biased and conducts. So the current flows through the R_L and back through secondary of transformer. The diode D_2 is reverse biased. So no current flows through it.



→ During negative half cycle of input AC supply D_2 is forward biased, So once again current flows through R_L. The diode D_1 is reverse biased. So no current flow through it. Hence current flows for both cycles of i/p signal.

Analysis:-

1) Dc Load voltage (V_{dc})

$$V_{dc} = \frac{\text{Area under curve over cycle}}{\text{Base}}$$

$$V_{dc} = \frac{1}{\pi}\left[\int_0^{\pi} V_m \sin\theta \, d\theta + \int_{\pi}^{2\pi} V_m \sin\theta \, d\theta\right]$$

$$= \frac{V_m}{\pi}\left[-\cos\pi - (-\cos 0)\right]$$

$$\boxed{V_{dc} = \frac{2V_m}{\pi}}$$

2) Dc Load Current I_{dc}

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \boxed{\frac{2I_m}{\pi}}$$

3) RMS Value of Ac Voltage.

$$V_{rms} = \sqrt{\int_0^{\pi} \frac{V_m^2 \sin^2\theta \, d\theta}{\pi}}$$

$$= \sqrt{\frac{V_m^2}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\theta}{2}\right)d\theta} \Rightarrow \sqrt{\frac{V_m^2}{2\pi}\left(\theta - \frac{\sin 2\theta}{2}\right)_0^{\pi}}$$

$$= \sqrt{\frac{V_m^2}{2\pi}[\pi - 0]}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

4) RMS Current,

$$I_{rms} = \frac{V_{rms}}{R_L} = \frac{V_m}{\sqrt{2}R_L} = \frac{I_m}{\sqrt{2}}$$

5) Ripple factor:-

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{V_m/\sqrt{2}}{2V_m/\pi}\right)^2 - 1} \Rightarrow \sqrt{\left(\frac{V_m^2/2}{\frac{4V_m^2}{\pi^2}}\right) - 1}$$

$$= \sqrt{\pi^2/8 - 1}$$

$$\boxed{\gamma = 0.4821}$$

6) Rectification Efficiency (η).

$$\eta = \frac{V_{dc}^2/R_L}{V_{rms}^2/R_L}$$

$$= \frac{\left(\frac{2V_m}{\pi}\right)^2}{\left(\frac{V_m}{\sqrt{2}}\right)^2} \times 100$$

$$= \frac{\frac{4V_m^2}{\pi^2}}{\frac{V_m^2}{2}}$$

$$= 8/\pi^2 \times 100$$

$$\boxed{\eta = 81.2\%}$$

7) Transformer Utilization Factor (TUF)

$$T_{UF} = \frac{V_{dc} I_{dc}}{V_{rms} \cdot I_{rms}}$$

for secondary.

$$T_{UF} = \frac{\frac{2V_m}{\pi} \cdot \frac{2I_m}{\pi}}{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}} = \frac{8}{\pi^2} = 0.812$$

TUF for primary winding = 2 × TUF of Halfwave Rectifier

= 2 × 0.286

= 0.572

Average of Fullwave ⇒ $\frac{0.572 + 0.812}{2} = 0.693$

$$\boxed{TUF = 69.3\%}$$

8) Regulation = $\frac{V_{NL} - V_{FL}}{V_{FL}}$ (and) $\frac{R_f + R_s}{R_L} \times 100\%$

9) Form factor = $\frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}} = \boxed{1.11}$

↓

$\frac{\text{Vrms value of o/p voltage}}{\text{Average DC Value}}$

10) Peak factor = $\frac{\text{Peak value of o/p Voltage}}{\text{RMS value of o/p voltage}} = \boxed{\frac{V_m}{V_m/\sqrt{2}}}$

= 1.414.

Advantages

1) η is twice of Halfwave Rectifier
2) Ripple is less.
3) Better TUF.
4) o/p is twice than Half wave Rectifier

Disadvantage.

1. PIV of diodes used is twice that of diodes
2. center tap is must.

BRIDGE RECTIFIER :-

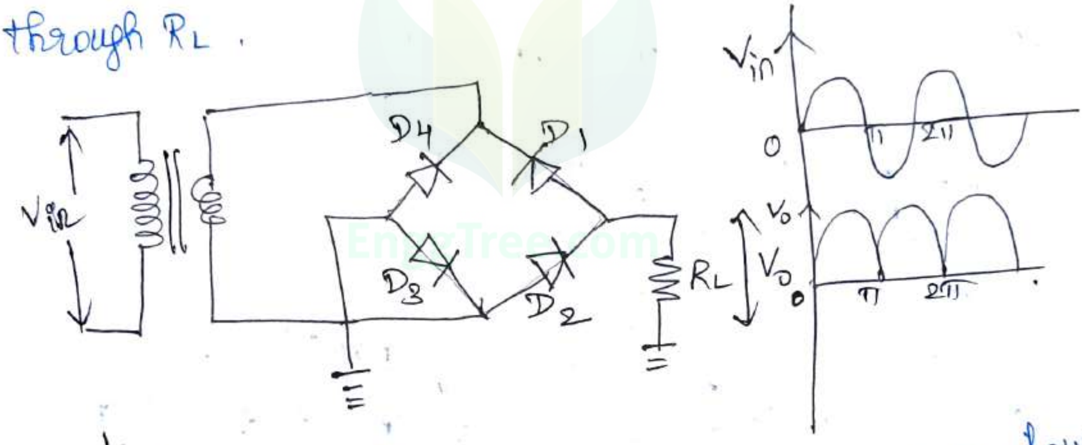
→ The need of centre tapped Transformer in full wave rectifier is replaced by bridge rectifier.

→ It has 4 diodes connected in the form of bridge.

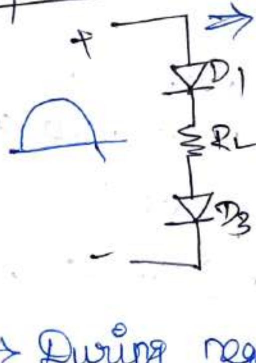
→ The AC i/p voltage is applied to diagonally opposite ends of bridge.

→ A load resistance is connected between other two ends of bridge.

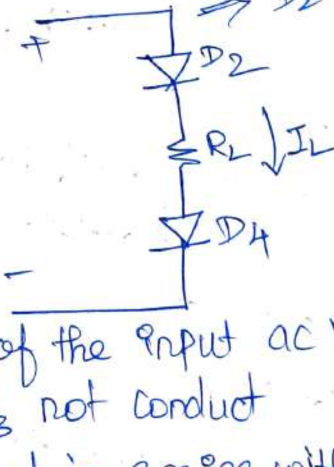
→ For positive half cycle diodes D_1 & D_3 conduct whereas diodes D_2 & D_4 not conduct, the load current flows through R_L.



Operation



→ D_1 & D_3 Forward bias for + half cycle



→ D_2 & D_4 forward biased for negative half cycle.

→ During negative half cycle of the input ac voltage diodes D_2 & D_4 conduct & D_1, D_3 not conduct

→ when D_2 & D_4 connect conduct in series with load R_L, the current flows through R_L in same direction as previous half cycle

→ The bridge rectifier has two forward biased diodes in series with supply voltage & load.

→ Maximum efficiency of bridge rectifier is 81.2% & Ripple factor of 0.48.

Advantages:-

i) Bridge Rectifier replace the bulky center Tapped Transformer type rectifier.

ii) TUF is 0.812

iii) used in application where no o/p Terminal is Grounded.

LASER DIODE.

→ Laser (Light Amplification by stimulated Emission of Radiation) emits a beam of single wavelength (or) very narrow band of wavelength. (1 μm to 100 μm)

→ Thus the emitted light has a single colour (mono-chromatic) and used in fiber optic communication.

→ PN Junction is formed by two Arsenide layers

Application:-

i) Compact Disc

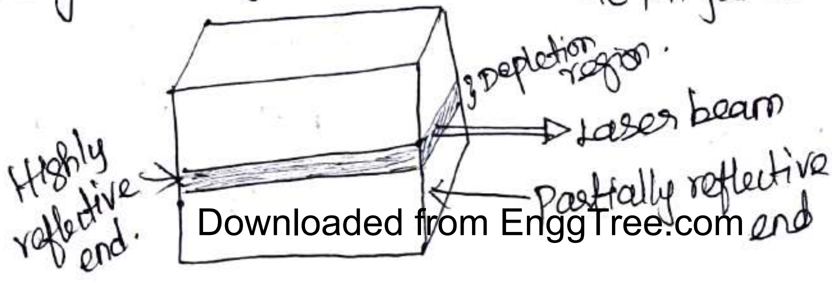
ii) Bar codes

iii) Fiber optic Communication.

Types of LASER:-

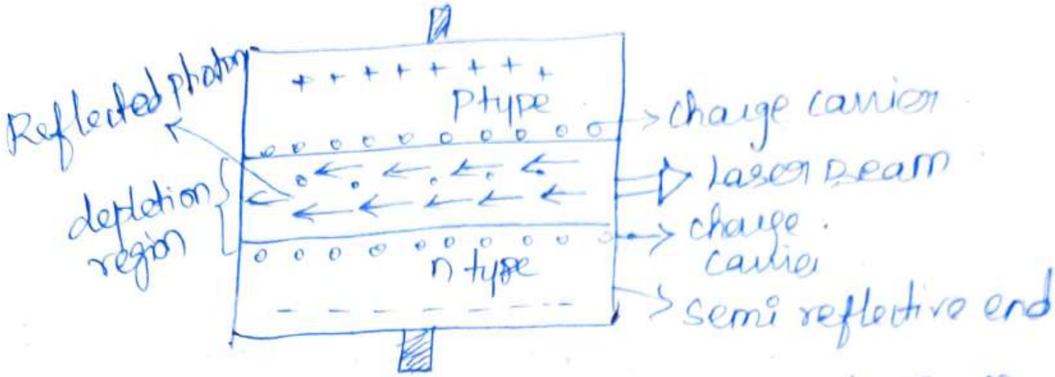
i) surface emitting LASER diode → emit light in perpendicular to pn junction

ii) Edge emitting Laser diode → Emit light in direction Parallel to pn junction



Operation :-

→ An PN Junction of Gallium arsenide (GaAs) or Combined with other materials manufactured with precisely defined length (L). The ends of junction polished to a mirror surface and usually have an additional reflective coating.



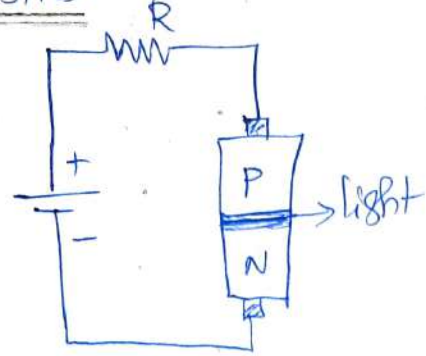
→ Consider the effect of charge carriers entering the depletion region of forward biased junction. The charge carriers excite the atoms, they strike, causing random emission of photons of energy as electrons are raised to higher energy level and fall back to lower level.

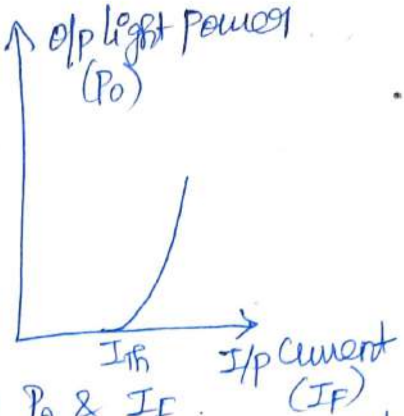
→ Eventually several photons strike one of reflective ends of junction perpendicularly. So that they are reflected back along their original path.

→ These reflected photons are then reflected back again from the other end of junction. So photons increase in number as they cause other similar photons to be emitted from atoms.

→ The beam of coherent light emerges from the partially reflective end of junction. So high energy density, laser beam can be quite dangerous.

Characteristics :-





→ The characteristics are between P_0 & I_F.

→ The o/p power doesnot increase significantly until I_F exceeds the Threshold current I_{Th}, which is level of forward current at which lasing commences at current level below the threshold. Laser diodes are very Temperature sensitive that causes Thermal runaway.

→ The maximum o/p of low power laser diode of 2mw to 10mw Current rating 30mA to 60mA

→ The forward voltage drop operating voltage from 1.2V to 2.4V

Advantages :-

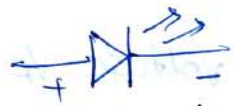
i) very compact ii) Efficient Compared to laser. iii) Long life

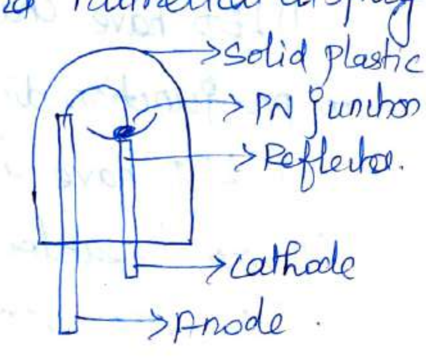
Disadvantages

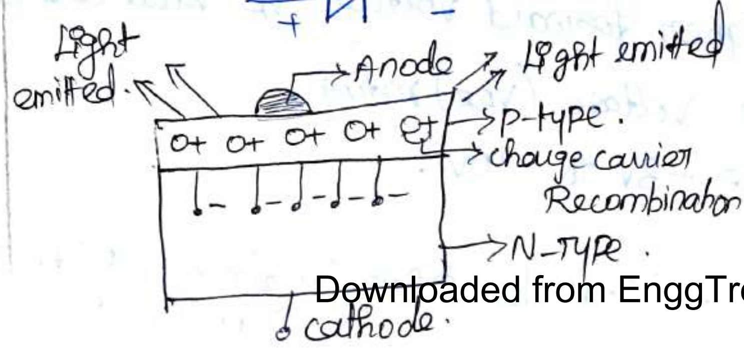
1. optical Performance is not equal to other laser types

LIGHT EMITTING DIODE (LED) (N/D' 2017)

→ Light emitting diodes (LED) Produce light and are generally used as indicating Lamps and numerical display.







Component	Forward voltage V_f	Colour Emitted
GaAs	1.5V	Infrared (visible)
AlGaAs	1.8V	Red
Gap.	2.4V	Green

→ In Gallium, phosphide the energy liberated in the form of Photons to create visible light source. LED resistance = 1k or 1.5k

Emission of Light :-

→ When LED is forwardbias. The electron from N side & holes from P-side crosses the junction and recombination takes place.

→ As a result of this the electrons lying in the conduction band of N region fall into the holes lying in valence band of P region.

→ The difference of energy between the conduction band and the valance band is radiated in the form of light energy. Light is generated by recombination of $\bar{e}$ and holes and excess energy transfered to emitted photon. Forward voltage 1.4 to 3.6V ~~forward voltage~~

→ When reverse biased LED emit no light, to operate from 1.5 to 3.3V with current 10mA, Power required 10 to 150mW.

LED characteristics :-

i) LED have characteristic curve that are very similar to pn junction diode.

ii) LED have higher forward voltage V_F value and lower reverse breakdown voltage (V_{BR}) rating.

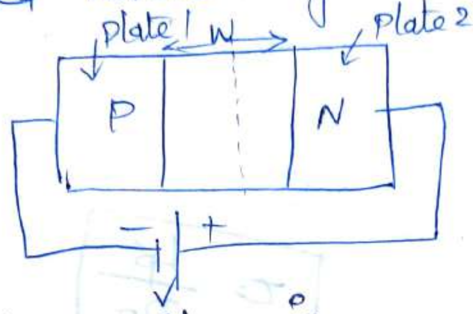
iii) Reverse voltage −3V to −10V.

Application

1) Power Indicator, level Indicator 2) Burglar alarm 3) Picture phone 4) Multimeters

JUNCTION CAPACITANCE [N/D'16]

→ under reverse bias condition, bias increases depletion layers width is also increases. As the charge particles moves away from the junction there exists a change in charge with respect to applied reverse voltage.



The Types of capacitance is,

* Diffusion capacitance
* Transition capacitance

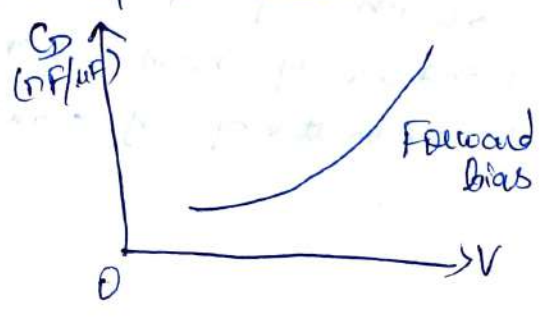
Diffusion capacitance (or) storage capacitance (C_D)

→ The capacitance that exists in forward biased junction is called diffusion capacitance. In this case charge is stored on both side of the junction and varies with applied potential.

→ It is also defined as rate of change of injected charge with applied voltage.

$$\boxed{C_D = \frac{dQ}{dV}} \rightarrow (1)$$

* The value of C_D is greater than transition capacitance C_T that exists in reverse bias.



It is defined as the ratio of change of injection charge when voltage is applied.

$dQ \rightarrow$ The change in charge.

$dv \rightarrow$ Applied voltage across the junction.

→ As applied voltage increases concentration of injected charged particles also increases.

→ Diffusion capacitance is determined by,

$$\boxed{C_D = \frac{\tau I}{\eta V_T}} \qquad \boxed{\tau = \frac{L_p^2}{D_p}}$$

where, $\tau \rightarrow$ Mean life time of holes & electrons

$I \rightarrow$ Forward bias diode current.

$V_T \rightarrow$ Voltage equivalent of temperature.

$\eta \rightarrow$ constant. $1 \rightarrow Ge$, $2 \rightarrow Si$.

→ Diffusion capacitance is directly proportional to current. In forward biased condition (C_D) is in parallel with forward resistance.

$$\boxed{C_D = \tau g} \quad g \rightarrow \text{Transconductance.}$$

$$\boxed{C_D \propto I}$$

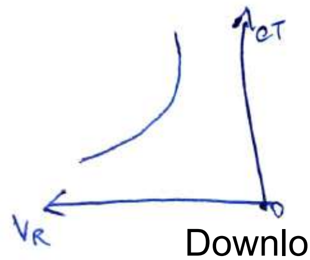
The value of $C_D = 10$ to $1000pF$. Hence diode carries large current

---

$C_T = \frac{\varepsilon A}{W}$ where $W \rightarrow$ width of depletion region.

$A \rightarrow$ Area of cross section of junction

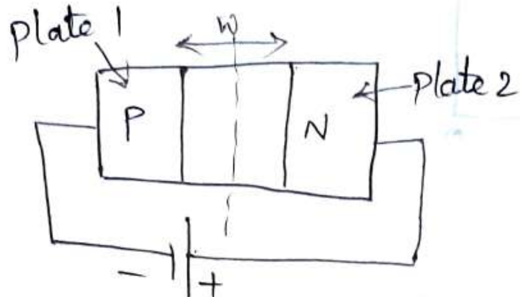
$\varepsilon \rightarrow$ permittivity of semiconductor



Continuation →

TRANSITION CAPACITANCE (C_T) (or) JUNCTION CAPACITANCE

→ Under reverse bias condition, increases in depletion width, As the charge particles move away from the junction there exists a change in charge w.r to the applied reverse voltage.



→ This capacitance is smaller when compared to diffusion capacitance (C_D)

→ The width of depletion increases with reverse voltage. The immobile ions is large in depletion layer form the capacitance C_T.

$$C_T = \frac{dQ}{dV} \longrightarrow (1)$$

dQ → Increase in charge by applying dv
dv → change in voltage at time.

→ It is also called space-charge capacitance, barrier capacitance (or) depletion layer capacitance.

→ consider the PN junction diode, two sides are not equally doped. (ie) Impurity added to one side is more than other p side is lightly doped compared with n-side then the relation between potential and charge density is given by poison equation,

$$\frac{d^2V}{dx^2} = \frac{q \cdot N_A}{\varepsilon}$$

→ If n side lightly doped compared with p-type.

$$\frac{d^2V}{dx^2} = \frac{q \cdot N_D}{\varepsilon}$$

$$I = \frac{dQ}{dt} \qquad \therefore \boxed{I = C_T \frac{dV}{dt}}$$

Verified
M. [signature] 13/9/19
(Dr. M. Ettappan)

P-n Junction Diode.

Problems based on p-n junction diode:

1. The reverse saturation current of a silicon PN Junction diode is 10μA. Calculate the diode current for the forward-bias voltage of 0.6V at 25°c. [AU/ECE - May 2007]

Solution:

Given:

$V_f = 0.6V$ $\quad T = 25 + 273$

$I_0 = 10 \mu A$ $\quad T = 298 K$

$\eta = 2$ (For silicon)

$K = 8.61 \times 10^{-5} eV$

$V_T = KT$

$= 8.61 \times 10^{-5} \times 298$

$V_T = 25.6 mV$

$$I = I_0 \left(e^{\frac{V_f}{\eta V_T}} - 1 \right)$$

$$= 10 \times 10^{-6} \left(e^{\frac{0.6}{2 \times 25.6 \times 10^{-3}}} - 1 \right)$$

$\boxed{I = 1.174 A}$

2. A p-n junction diode has at a temperature of 125°c, a reverse saturation current of 30μA. Find the dynamic resistance for 0.2V bias in forward and reverse direction.

Solution

(a) Forward direction:

$125°c = (273 + 125) = 398 K$

$V_T = KT$

$= 8.61 \times 10^{-5} \times 398$

$= 0.0343$ volt.

For Ge $\eta = 1$:

hence $I = I_C\left(e^{V/V_T} - 1\right)$ at $125^\circ C$

Differentiating the above equation with respect to v, we get,

$$g = \frac{1}{r} = \frac{dI}{dv} = I_0\left(\frac{e^{V/V_T}}{V_T}\right)$$

$$= \frac{30 \times 10^{-6}}{0.0343}\left(e^{\frac{0.2}{0.0343}}\right)$$

$$= 0.297\ \mho$$

Thus the dynamic resistance in forward direction is

$$r = \frac{1}{g} = \frac{1}{0.297} = 3.36\,\Omega$$

(b) Similarly for reverse direction.

$$g = \frac{1}{r} = \frac{I_0}{V_T}\left(e^{-V/V_T}\right)$$

$$= \frac{30 \times 10^{-6}}{0.0343}\left(e^{-5.830}\right)$$

$$= 2.55 \times 10^{-6}\ \mho$$

Hence $r = \frac{1}{g} = \frac{1}{2.55 \times 10^{-6}} = 391\,K\Omega$

3. A Ge diode has a saturation current of $10\mu A$ at $300^\circ K$. Find the saturation current at $400^\circ K$.

The Saturation current at $400^\circ K$.

$I_1 = 10\mu A$ $\quad I_2 = ?$

$T_1 = 300K$ $\quad T_2 = 400K$

(in terms of c) $\quad$ (in terms of c) $= 127^\circ c$

$T_1 = 27^\circ c$

$$I_2 = I_1 \times 2^{(T_2 - T_1)/10}$$

$$I_2 = 10 \times 10^{-6} \times 2^{(127-27)/10}$$

$$\boxed{I_2 = 10.24 mA}$$

Problems based on Full wave rectifier:

1. In a fullwave rectifier a signal of 300 volts at 50 Hz is applied at the input. Each diode has an internal resistance of 800 Ω. If the load is 2000 Ω then calculate

(i) peak value of current in the output

(ii) Output dc current

(iii) Efficiency of power transfer.

Solution:

Given data:

$V_{rms} = 300V$ $f = 50 Hz$ $R_f = 800 \Omega$

$R_L = 2000 \Omega$

We know,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad (\text{or}) \quad V_m = \sqrt{2} \times V_{rms}$$

$$= 424.2 \text{ volts.}$$

(i) $I_m = \dfrac{V_m}{R_F + R_L} = \dfrac{424.2}{800 + 2000}$

$= 151.52 mA$

(ii) $I_{dc} = \dfrac{2I_m}{\pi} = \dfrac{2 \times 151.52 \times 10^{-3}}{\pi} = 96.46 mA$

(iii) Efficiency: $= \dfrac{P_{dc}}{P_{ac}} \times 100$

$P_{dc} = I_{dc}^2 R_L$

$= (96.46 \times 10^{-3})^2 \times 2000$

$= 18.61$ Watts

$P_{ac} = I_{rms}^2 (R_F + R_L) = \left(\frac{151.52 \times 10^{-3}}{\sqrt{2}} \right)^2 \times 2800$

$= 32.141$ Watts

Efficiency $= \frac{18.61}{32.141} \times 100$

$= 57.9\%$

2. A FW diode rectifier has $V_i = 100 \sin \omega t$, $R_L = 900\,\Omega$ and $R_f = 100\,\Omega$ calculate.

(a) The Peak load current (I_m)
(b) The dc load current I_{dc}
(c) AC load current (I_{rms})
(d) DC load voltage V_{dc}
(e) The peak instantaneous diode current I_{dp}
(f) The PIV on the diode
(g) AC input power
(h) The dc output power
(i) Rectification efficiency.

Solution:

$V_i = 100 \sin \omega t \quad V_m = 100 \quad R_L = 900\,\Omega \quad R_F = 100\,\Omega$

(a) Peak load current $I_m = \frac{V_m}{R_F + R_L} = \frac{100}{900+100} = 0.1$ Amps

(b) DC load current $I_{dc} = \frac{2 I_m}{\pi} = \frac{2 \times 0.1}{\pi} = 0.0636$ Amps

(c) AC load current $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{0.1}{\sqrt{2}} = 0.0707$ Amps

(d) DC load voltage $V_{dc} = I_{dc} R_L$

$= 0.0636 \times 900$ Vdc

$V_{dc} = 57.29$ Volts

(e) Peak instantaneous diode current

$i_{dp} = I_m = 0.1\,A$

(f) PIV of the diode $PIV = 2V_m$

$= 2 \times 100$

$= 200V$

(g) The AC input power.

AC input power $= I^2_{rms}(R_F + R_L)$

$= (0.0707)^2 \times (900 + 100)$

$= 5W$

(h) The dc output power

DC output power $= I^2_{dc} R_L$

$= (0.0636)^2 \times (900)$

$= 3.64W$

(i) Rectification efficiency

$$\eta = \frac{81.0}{1 + \left(\frac{R_F}{R_L}\right)} = \frac{81}{1 + \left(\frac{100}{900}\right)} = 72.9\%$$

(or)

$$\%\,\eta = \frac{\text{output power}}{\text{input power}} = \frac{3.64}{5} = 72.8\%$$

Problems based on zener diode.

1. Determine the value of series resistor (R_s) and the maximum zener diode current for a regulator which is required to provide a load current at 10mA

stabilized at 12 v dc supply which varies from 24V to 20V. Assume that the minimum zener diode current is 2mA $r_z = 0\,\Omega$.

Given data: V_S = supply voltage

$V_{S(min)} = 24V$

$I_{S max}$ $V_z = 12V$

$I_{Lmax} = 10mA$; $I_{zmin} = 2mA$

$$R_{S max} = \frac{V_{S min} - V_z}{I_{zmax} + I_{Lmax}} = \frac{24-12}{(2+10)mA}$$

$$= 1K\Omega$$

$$I_{zmax} = \frac{V_{Smax} - V_z - (I_L R_S)_{max}}{R_S}$$

$$= \frac{30 - 12 - (10mA)(1K\Omega)}{1K\Omega}$$

$$= \frac{8}{1K\Omega}$$

$$\boxed{I_{zmax} = 18\,mA}$$

2. Determine the series resistor (R_S) required for a zener diode regulator with an output vatage of 5.6V, if the supply voltage (V_S) varies from 10 v to 50 V. The minimum zener current is 3mA. Determine also the maximum zener current and the power dissipation.

Given data:

$V_z = 5.6V$ $V_{Smin} = 10V$; $V_S max = 50V$;

$I_{zmin} = 3mA$

$$R_S = \frac{V_{smin} - V_z}{I_{zmin}} = \frac{\quad}{3} = 1.46k\Omega$$

$$I_{zmax} = \frac{V_{smax} - V_z}{R_S} = \frac{50-5.6}{1.46\,k\Omega} = 30mA$$

Power dissipation

$$P_z = V_{smax} \cdot I_{zmax}$$

$$= (30mA)(5.6v)$$

$$\boxed{P_{z_{diss}} = 168mW}$$

Problems based on Half wave rectifier.

1. A half wave rectifier has $V_i(t) = 100\sin\omega t$ and $R_L = 900\Omega$, $R_F = 100\Omega$. Calculate (i) Peak load current
(ii) DC load current
(iii) AC load current (I_{rms})
(iv) DC load voltage
(v) PIV
(vi) Dc output power
(vii) AC input power
(viii) Efficiency (η)

(i) Peak load current

$$\boxed{I_m = \frac{V_m}{R_f + R_L}}$$

$V_i(t) = 100\sin\omega t$: ($V_m \sin\omega t$)

$\therefore V_m = 100v$

$$\therefore I_m = \frac{100}{100+900} = \frac{100}{1000}$$

$$I_m = 0.1A$$

(ii) DC load current:

$$\boxed{I_{dc} = \frac{I_m}{\pi}} = \frac{0.1}{\pi}$$

$$I_{dc} = 0.03A$$

(iii) AC load current (I_{rms})

$$I_{rms} = \frac{I_m}{2} = \frac{0.1}{2}$$

$$= 0.05A$$

(iv) DC load voltage:

$$\boxed{V_{dc} = \frac{I_m R_L}{\pi}}$$

$$= \frac{0.1 \times 900}{\pi} = 28.64V$$

(v) $\boxed{PIV = V_m}$ $\therefore V_m = 100V$

(vi) DC output power:

$$\boxed{P_{dc} = I_{dc}^2 R_L}$$

$$= (0.03)^2 \times 900$$

$$P_{dc} = 0.81W$$

(vii) AC input power:

$$P_{AC} = I_{rms}^2 (R_F + R_L)$$

$$= (0.05)^2 (100 + 900)$$

$$P_{AC} = 2.5W$$

(viii) Efficiency

$$= \frac{DC\ o/p\ power}{AC\ o/p\ power} = \frac{0.81}{2.5} = 0.324$$

In terms of % = 32.4%.

2. A Half wave rectifier is supplied from 230V, 50Hz, supply with a step down ratio of 3:1 to resistive load of 10KΩ. The diode forward resistance is 75Ω, while transformer secondary resistance is 10Ω. calculate the maximum, average, RMS value of current dc output voltage efficiency & ripple factor

solution:

$V_{in} = 230V$; $f = 50Hz$; $R_L = 10K\Omega$

$R_f = 75\Omega$ $R_s = 10\Omega$

the given transformer is step down transformer with ratio = 3:1 thus the secondary voltage

$$V_{rms} = V_s = \frac{V_{in}}{3} = \frac{230}{3} = 76.67 \text{ volts}$$

∴ we know $V_{rms} = \frac{V_{max}}{\sqrt{2}}$ for sine wave

thus $V_{max} = \sqrt{2} V_{rms}$

$= \sqrt{2}(76.67)$

$= 108.42$ volt

(i) $I_m = \frac{V_m}{R_f + R_s + R_L} = \frac{108.42}{10K + 10 + 75} = 0.0107$ Amp

$= 10.7 mA$

(ii) $I_{dc} = I_{av} = \frac{I_m}{\pi} = \frac{10.7 mA}{\pi} = 3.422 mA$

(iii) $I_{rms} = \frac{I_m}{2} = \frac{10.7mA}{2} = 5.375 mA$

(iv) $V_{dc} = I_{dc} \cdot R_L$

$= 3.422 mA (10k\Omega)$

$= 34.2$ volt.

(v) % efficiency $= \frac{P_{dc}}{P_{ac}} \times 100$

$P_{dc} = I^2_{dc} \cdot R_L = (3.422 \times 10^{-3})^2 \times 10 \times 10^3$

$= 0.117$ Watts

$P_{ac} = I^2_{rms} (R_f + R_L)$

$= (5.375 \times 10^{-3})^2 (10.075 \times 10^3)$

$= 0.2910$ watts

% Efficiency $= \frac{P_{dc}}{P_{ac}} \times 100 = \frac{0.117}{0.291} \times 100$

$= 40.19\%$

(vi) Ripple factor:

$= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

$= \sqrt{\left(\frac{5.375}{3.422}\right)^2 - 1}$

$= 1.21$

Verified

M. [signature] 13.9.19

UNIT- II

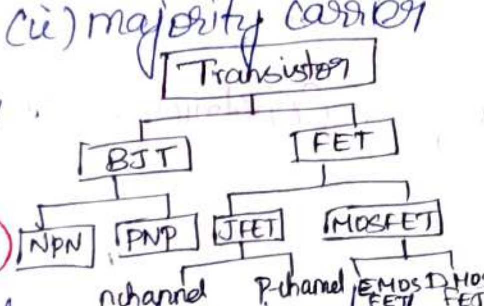
TRANSISTORS & THYRISTORS

The term transistor derived from the word TRANSFER+RESIS-TOR This term was adopted because it is best describe the operation of transistor which is the transfer of I/p signal current from a low resistance circuit to high resistance circuit.

Types:- (i) Bipolar (ii) Unipolar.

Bipolar:- The current conduction in bipolar transistor takes place due to both electron and holes. eg:- BJT - Bipolar Junction Transistor.

Unipolar:- The current conduction in unipolar transistor takes place due to only one type of carrier (ie) majority carrier than the transistor is called unipolar.
Eg: FET (Field effect Transistor).



BIPOLAR JUNCTION TRANSISTOR:- (BJT)

→ Bipolar Junction Transistor has 3 layers of semiconductor material

→ They are arranged in npn and pnp sequence with 3 terminals. It has 2 junctions. Its operation is same as that of PN Junction.

→ The current that flow through transistor are similar to those that flow across a single PN Junction.

→ It is used for current amplication and controls the current at central region terminal, ie larger current flow through device

Three Terminals:-

i) Emitter:-

→ It is heavily doped than collector and Base

→ Its main function is to supply majority charge carrier to Base.

ii) Base:-

→ It is the middle section of Transistor.

→ It is very thin compared to emitter & base also it is lightly doped.

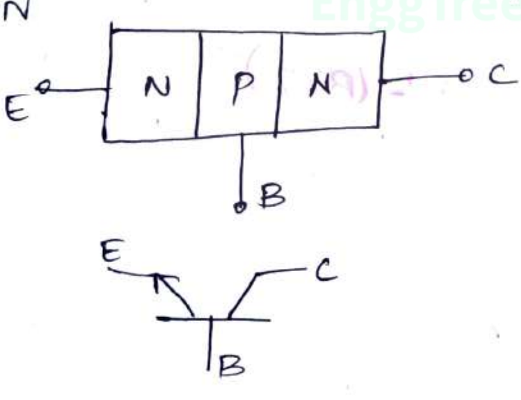
iii) Collector:-

→ It forms the right hand side of transistor. The main function is to collect majority charge carriers from emitter and pass to base.

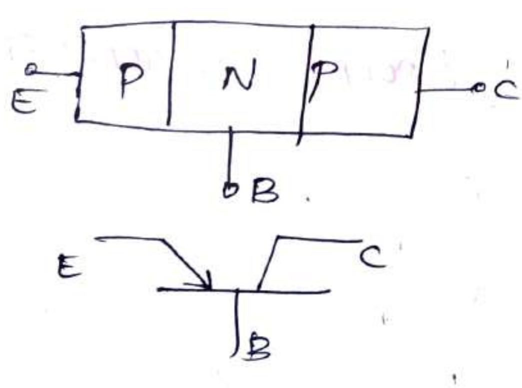
Mode	EB	CB
Active region	FB	RB
Saturation	FB	FB
Cutoff	RB	RB

Construction of BJT

NPN



PNP.



OPERATION:-

NPN TRANSISTOR:-

→ The NPN Transistor has two junctions Emitter base junction and collector base junction.

→ The Emitter base junction is forward biased and the collector base junction is reverse biased

→ The electron charge carriers from emitter flow through base but since only few electrons are present in base, only a few percentage of charge carriers flow out of base.

→ 98% of charge carriers flow from emitter to collector Terminal.

→ Since the base emitter junction is forward biased it has the forward characteristics of diode.

→ The cut in voltage for Ge is 0.3V and Si is 0.7V

→ A small change in forward bias voltage in base emitter junction controls the emitter and collector current.

→ If forward bias voltage is increased or decreased, the forward current is also increased or decreased.

→ If forward bias voltage is cutoff or reversed cuts the current completely. Thus BJT is called current controlled device

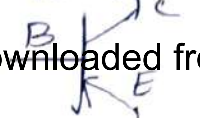
$$I_E = I_C + I_B$$

$$\boxed{I_E = I_C} \qquad I_B \simeq 0$$

PNP TRANSISTOR :-

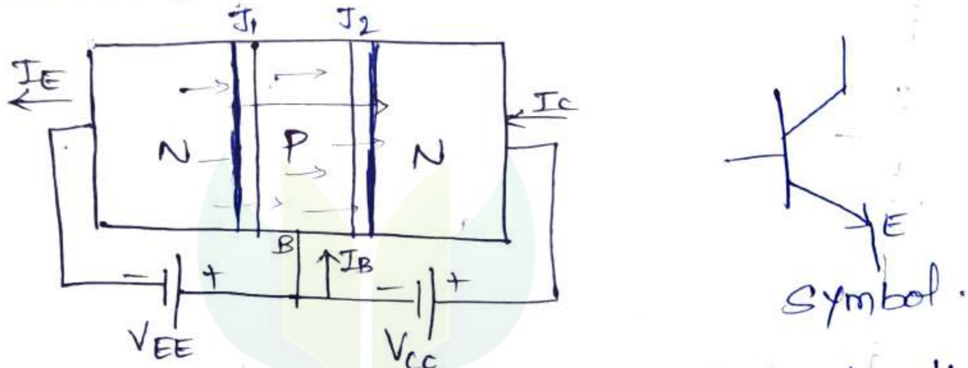
→ The PNP Transistor consist of Emitter base junction which is forward biased and Collector base junction is reverse biased.

→ In Emitter base junction, it is forward biased, the P-type Semiconductor is connected to positive terminal and Negative Terminal connected to N Type Semiconductor.



→ When the collector base junction is reverse biased, the electrons are flowing away from the collector junction towards the positive terminal.

→ The forward biased emitter junction causes electrons to be injected from the emitter in to the base region since the base is very thin, the injected electrons travels across the base region and arrive at reverse biased collector juction.

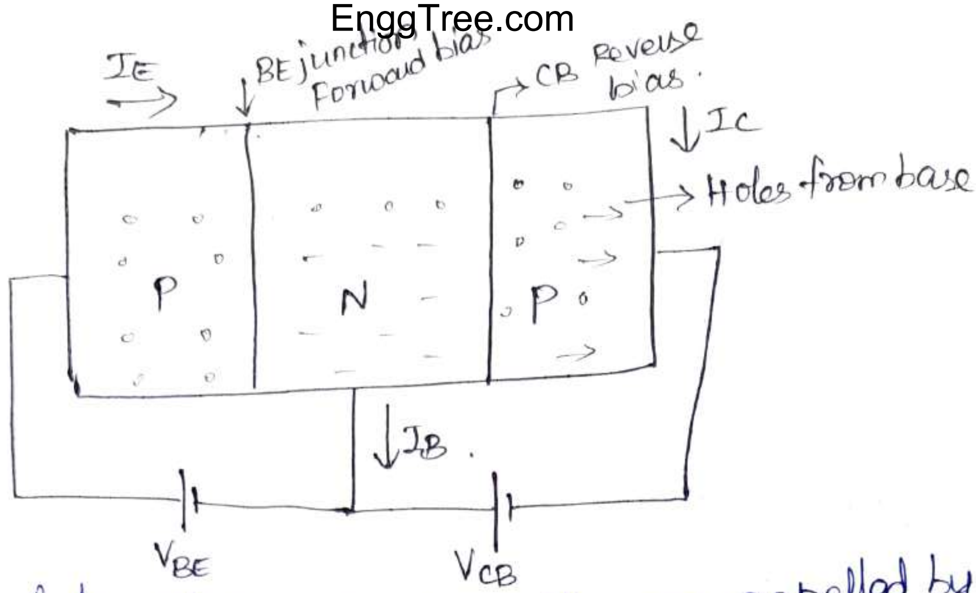


→ In forward bias condition at base emitter junction the barrier voltage is reduced and thus the electrons flow from emitter to base region.

→ Holes also flow from base to emitter ~~bet~~ because the base is very much lightly doped than collector almost all the current flowing from emitter to base consists of electrons.

→ Thus the majority charge carrier in npn device is electrons.

→ In Reverse bias junction, at collector base, the depletion region is very large and thus the base region becomes smaller.



→ The holes of P-region (ie) emitter are repelled by the Positive terminal of battery towards the base. Thus the Potential barrier at emitter junction is reduced as a result the depletion region disappears.

→ Hence the holes cross the junction and penetrate into the ntype region at Base. This constitutes Emitter current I_E

→ As the base is lightly doped the holes from emitter finds only few electrons to recombine in n-region of base and about 98% of holes cross emitter to collector region and flow to negative terminal.

→ The operation of npn and pnp transistor are same and the only difference is that the majority carrier in pnp is holes.

→ In reverse bias junction at collector base the depletion region is very large and thus base region becomes smaller.

→ Variation of forward bias voltage at BE junction controls the small base current and the much larger collector and emitter currents

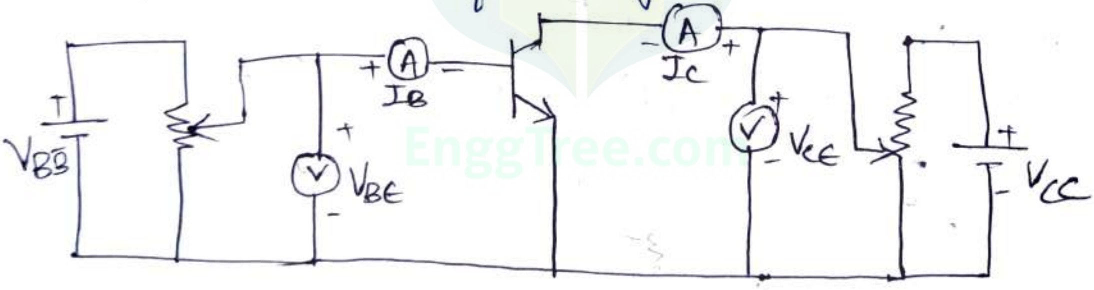
CE CONFIGURATION

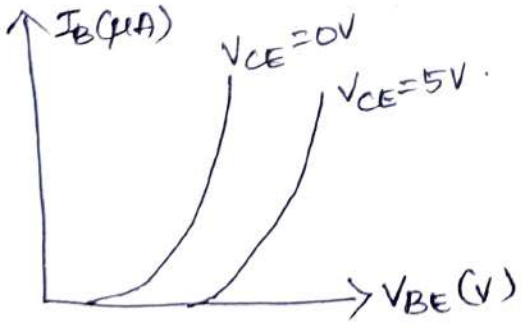
In this configuration base is i/p terminal, collector is o/p Terminal, Emitter is grounded. So input applied between Base and emitter. The amplified o/p signal is taken from the Collector & Emitter.

INPUT CHARACTERISTICS:

→ It is the curve drawn between emitter base voltage (V_{BE}) in x axis and Base current (I_B) in y axis at constant V_{CE}. To determine the i/p characteristics the collector to emitter is kept constant at zero volt. and base current is increased from 0 volt and V_{BE} ~~base~~ increased.

→ For different values of V_{CE} Graph drawn between V_{BE} Vs I_B.





→ When $V_{CE}=0$, Emitter base junction is forward biased and junction behaves forward biased diode. Hence i/p characteristics for $V_{CE}=0$ is similar to that of forward biased diode.

→ When V_{CE} increased, width of depletion region at reverse biased collector base junction will increase. Hence effective width of base will decrease. This causes decrease in I_B.

→ As compared to CB configuration I_B increases, rapidly with V_{BE}. Hence i/p resistance of CE is higher than CB circuit.

Current amplification factor (β)

It is the ratio of change in collector current to change in base current.

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{I_C}{I_B}.$$

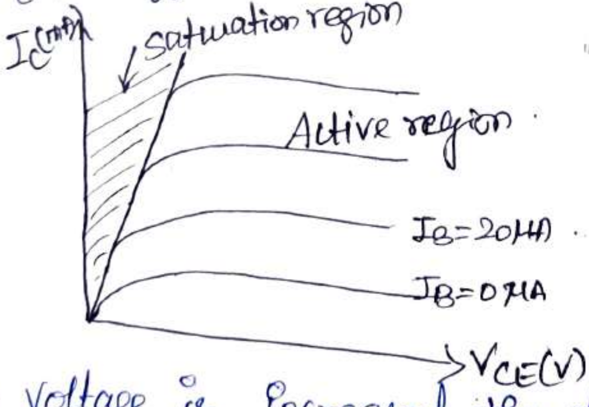
$$\boxed{I_C = \beta I_B}$$

Collector Current :- It is the sum of βI_B and leakage current.

$$\boxed{I_C = \beta I_B + I_{CEO}} \quad I_{CEO} \rightarrow \text{Small}.$$

Output characteristics:-

→ The Base current I_B is kept constant and adjust V_{CE} in several steps and I_C is noted. I_C versus V_{CE} are plotted for different constant values of I_B.



→ As V_{CE} voltage is increased the depletion region increases such that charge carriers from emitter flows to collector terminal.

→ only few carriers passes along base terminal, I_C increases with increasing V_{CE}.

→ Thus the slopes of CE o/p characteristics are more raised than Common base Configuration.

→ The active region is when i/p junction is forward biased and o/p junction is reverse biased. The Transistor is ON state.

→ when Collector Current is zero, the transistor is said to be cutoff region. It behaves as in OFF state.

→ when V_{CE} is very low, the transistor is said to be Saturated and both the junction are forward biased. This is known as saturation region.

$$I_{CEO} = (1+\beta) I_{CBO}.$$

$$I_C = (1+\beta) I_{CBO} + \beta I_B . \qquad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

TRANSISTOR PARAMETERS:-

I/p Impedance, $\boxed{h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}}_{V_{CE} = constant}$

O/p Admittance, $\boxed{h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}}_{I_B = constant}$

Forward Current gain,

$$\boxed{h_{fe} = \frac{\Delta I_C}{\Delta I_B}}_{V_{CE} = constant}$$

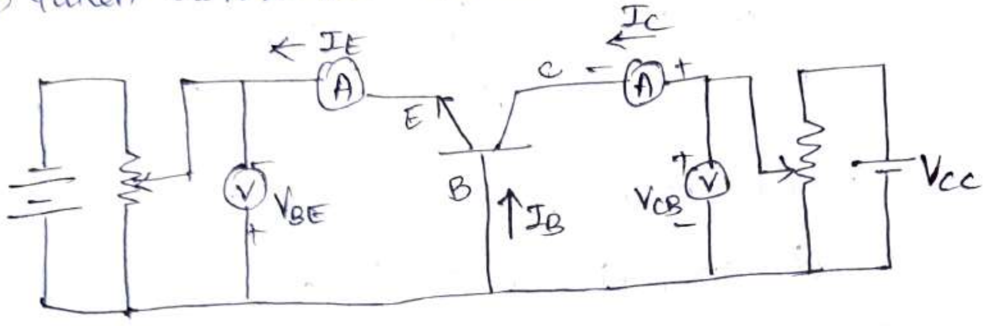
Reverse Voltage gain,

$$\boxed{h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}}_{I_B = constant}$$

COMMON BASE CONFIGURATION:-

→ In common base Configuration the base terminal is Common to both i/p Emitter and the o/p Collector Terminals.

→ The i/p signal applied between emitter base junction and o/p taken across the Collector base junction.

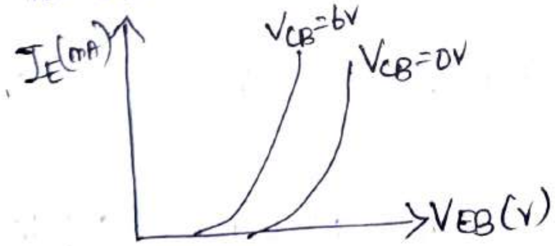


I/p characteristics:-

→ To find i/p characteristics the o/p voltage V_{CB} is Constant

→ The i/p Voltage V_{EB} is set at several levels

→ At each i/p voltage, the corresponding i/p I_E current is noted. The I_E and V_{BE} is plotted to give CB i/p characteristics



→ The Emitter base junction is forward biased and hence the i/p characteristics are same as that of forward biased Pn junction. As shown in graph in forward bias when i/p voltage is given, more i/p Current flows when the CB voltage is high.

→ If the i/p voltage is less than barrier Potential, then due to depletion region very Small Current flows through it.

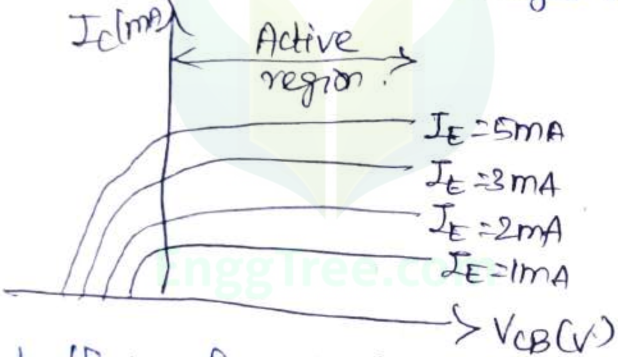
→ If the i/p voltage is greater than barrier potential, then depletion region disappears and thus the current increases with low resistance

O/P Characteristics

→ To determine the o/p characteristics of CB the emitter current I_E is kept constant, the voltage V_{CB} is adjusted in steps and the corresponding values of I_C are noted.

→ In the o/p characteristics, as the value of I_E is fixed, the value of collector current I_C is almost equal to I_E.

→ I_C remains constant when voltage V_{CB} is increased.



→ It is noted that when V_{CB} is reduced to zero I_C still flows.

→ It is because even when externally applied voltage is zero. there is still a existing barrier voltage at CB junction and thus I_C flows.

→ when both the Emitter base & collector base junction is forward biased. It is known as saturation region

→ The region when both the junctions are reverse biased is called cut off region.

→ The region when EB junction is forward biased and CB junction is reverse biased known as Active region

→ The active region is the normal operating region for transistor.

EARLY EFFECT:-

→ The width of base region is dependent on the collector base voltage. This dependence of Base region width is the Early Effect. (or) Base width modulation.

i.e, space charge width between collector & base tends to increase with the result that effective width of base decreases.

i) when the extremely large voltage applied, the effective base width may be reduced to zero causing voltage breakdown called "Punch Through"

ii) Recombination within base region decreases, hence α increases with increase in V_{CB}.

$$\boxed{\alpha = \frac{I_C}{I_E}}$$

iii) Minority carrier increases in base.

CB

$$\alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha I_E$$

$$\boxed{I_E = I_B + I_C}$$

$$I_C = \alpha I_E + I_{CBO}$$

↑ Leakage current

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$\Rightarrow I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}}$$

Transistor parameters:-

i) I/p Impedence.

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}\bigg|_{V_{CB} = \text{Constant}}$$

ii) O/p admittance.

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}\bigg|_{I_E = \text{Constant}}$$

iii) Forward Current gain.

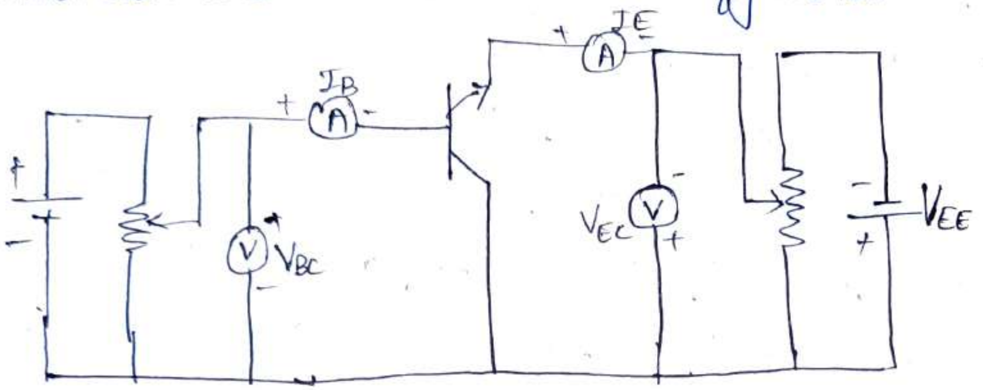
$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}\bigg|_{V_{CB} = \text{Constant}}$$

iv) Reverse Voltage gain.

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}\bigg|_{I_B = \text{Constant}}$$

COMMON COLLECTOR CONFIGURATION :-

The common collector configuration is used for impedance-matching purposes. Since it has a high i/p impedance and low o/p impedance, opposite to that of common base and common-emitter configuration.

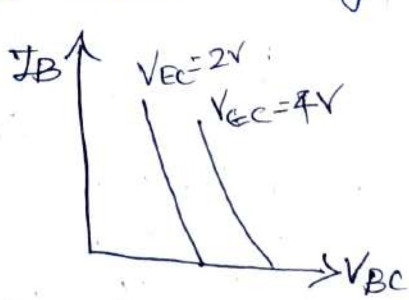


I/p characteristics :-

→ The i/p characteristics of CC is different from common emitter and common base characteristics.

→ The difference is due to the fact that i/p voltage V_{BC} is largely determined by o/p voltage (V_{EC})

→ With V_{EC} held constant, when V_{BC} level is increased, I_B is reduced V_{EB} voltage decreases and thus we get this i/p characteristics graph.



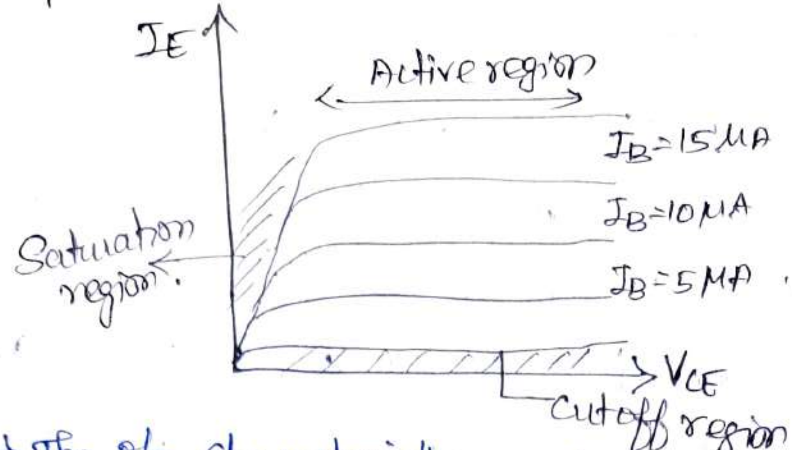
$$V_{EC} = V_{EB} + V_{BC}.$$

$$\boxed{V_{EB} = V_{EC} - V_{BC}}$$

Current amplification factor (γ).

$$\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$$

Output characteristics:



→ The o/p characteristics relates or o/p current I_E to an o/p voltage V_{CE} for various levels of i/p current (I_B). For all practical purposes, the o/p characteristics of CC Configuration are same as for CE Configuration.

$$\gamma_{dc} = \frac{I_E}{I_B}.$$

Transistor Parameters:-

i) I/p impedance:-

$$h_{ic} = \left.\frac{\Delta V_{BC}}{\Delta I_B}\right|_{V_{CE} = \text{Constant}}$$

ii) o/p admittance

$$h_{oe} = \left.\frac{\Delta I_E}{\Delta V_{EC}}\right|_{I_B = \text{Constant}}$$

iii) Forward Current gain.

$$h_{fe} = \left.\frac{\Delta I_E}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

iv) Reverse voltage gain:-

$$h_{re} = \left.\frac{\Delta V_{BC}}{\Delta V_{EC}}\right|_{I_B = \text{Constant}}$$

TRANSISTOR AS AN AMPLIFIER:

Voltage Amplification:-

→ The Transistor is used to amplify voltage, Thus the AC i/p voltage is Superimposed with DC i/p voltage and this is applied at Base Terminal.

→ Thus the resulting base current is DC whose amplitude is changing for the purpose of analysing it is decomposed to AC & DC component.

→ By transistor action the base current is amplified by Transistor into large collector current & producing large collector current.

$$\boxed{A_v = \frac{V_o}{V_{in}}}$$

Current Amplification:-

→ A small change in I_B produce large change in Collector current. I_C.

$$\boxed{\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}}$$

→ Increasing & decreasing magnitude of i/p and o/p Current may be defined as AC Quantities

$$\boxed{\beta_{AC} = \frac{I_C}{I_B}}$$

NOTE:-

Why CE is most Prefered Configuration:-

Reason:-

i) It has high voltage & Current gain.

ii) It has high Power gain because the power gain is product of Voltage & Current gain.

Current Amplification Factor & Relation between α, β, γ

CB configuration $\alpha = \frac{\Delta I_C}{\Delta I_E}$

CE Configuration $\beta = \frac{\Delta I_C}{\Delta I_B}$

CC Configuration $\gamma = \frac{\Delta I_E}{\Delta I_B}$

We know:-

CB, $I_B = 0$

$$\Delta I_E = \Delta I_C + \Delta I_B \quad \text{--- (1)}$$

$$\Delta I_E = \Delta I_C$$

$$\Delta I_C = \alpha \Delta I_E \quad \text{--- (2)}$$

sub (2) in (1)

$$\Delta I_E = \alpha \Delta I_E + \Delta I_B$$

$$\Delta I_E (1-\alpha) = \Delta I_B$$

÷ by ΔI_C,

$$\frac{\Delta I_E}{\Delta I_C}(1-\alpha) = \frac{\Delta I_B}{\Delta I_C}$$

$$\frac{1}{\alpha}(1-\alpha) = \frac{1}{\beta}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \quad \boxed{\alpha = \frac{\beta}{1+\beta}} \quad \boxed{\gamma = \frac{1}{1-\alpha} = 1+\beta}$$

Comparison CB, CE, CC.

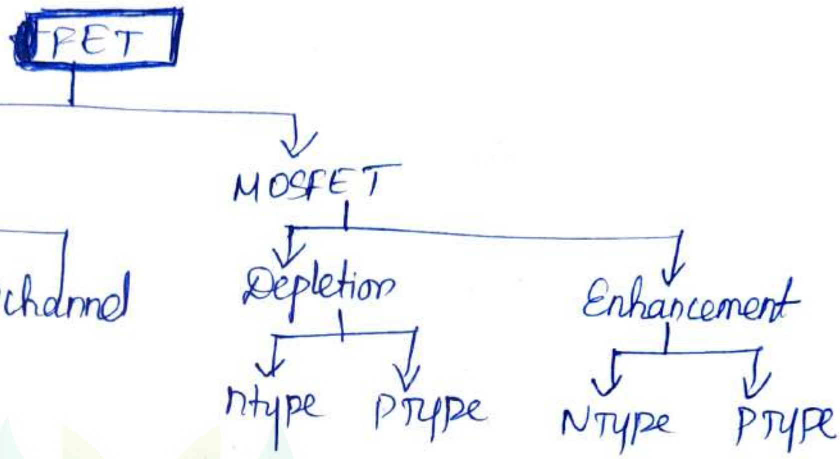
Parameter	CB	CE	CC
1) Common Terminal	Base	Emitter	Collector
2) I/p Current	I_E	I_B	I_B
3) o/p Current	I_C	I_C	I_E
4) O/p voltage	V_{EB}	V_{BE}	V_{BC}
5) I/p Voltage	V_{CB}	V_{CE}	V_{EC}
6) Gain	$\alpha = \frac{I_C}{I_E}$	$\beta = \frac{I_C}{I_B}$	$\gamma = \frac{I_E}{I_B}$
7) Application	High freq. Circuit	Audio ckt.	For impedance Matching

FIELD EFFECT TRANSISTOR

→ FET is a device in which flow of o/p current through the conducting region is controlled by electric field.

→ It is a unipolar device depend either hole or electron.

→ FET is voltage controlled device



N- Channel JFET:-

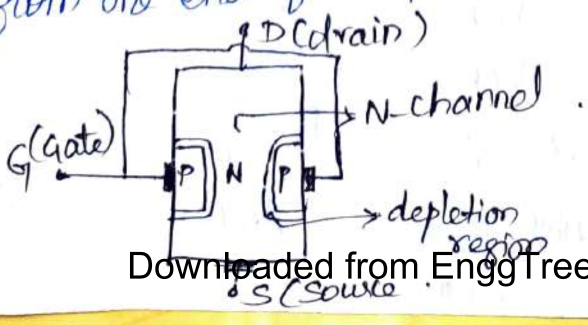
→ In n channel JFET, n type semiconductor is placed between two smaller pieces of P-type semiconductor.

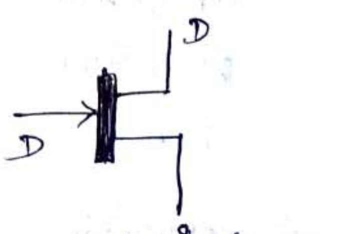
→ The three terminals of JFET are Gate, drain and source

→ The Gate Terminal is two p-type terminal which are connected together, this P-region is heavily doped.

→ 'S' ⇒ source is the terminal through which majority carriers enters the FET

→ 'D' ⇒ Drain is the terminal through which majority carrier leave the FET. When a potential difference is established between source and drain, the majority carrier "electron" flows from one end of N-type to other that forms channel.



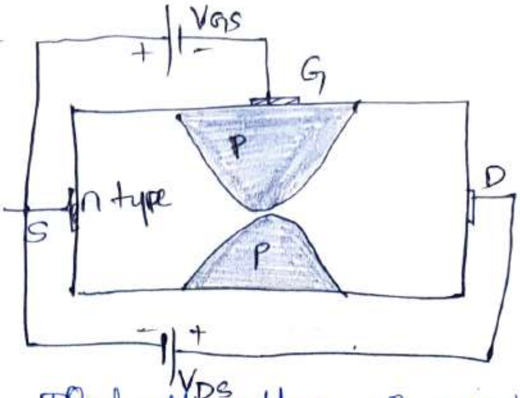


N-channel JFET

DRAIN CHARACTERISTICS WHEN V_{GS} is Negative for n-channel JFET

→ Here the Gate source voltage is set to negative values.

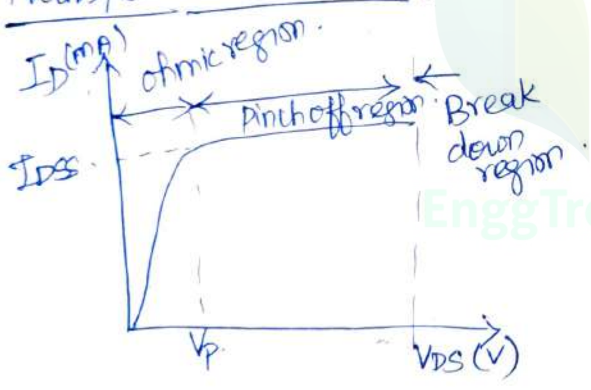
→ when V_{DS} is increased in steps and the corresponding values of I_D is noted at each step V_{DS}.



→ when $V_{GS} = -1V$ is applied the Pinch-off voltage is reached at lower I_D current level than $V_{GS} = 0$.

→ Similarly when furthur negative voltages like $-2V, -3V$ is applied the I_D current level is much lower than $-1V$. when pinch off voltage is reached. furthur increase in voltage, I_D increases this region is breakdown region.

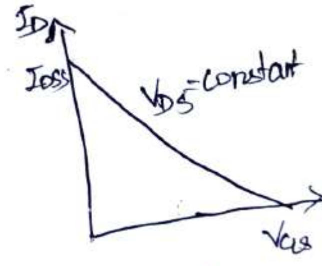
Transfer characteristics:-



Between I_D Vs V_{GS}.

Nchannel

p channel

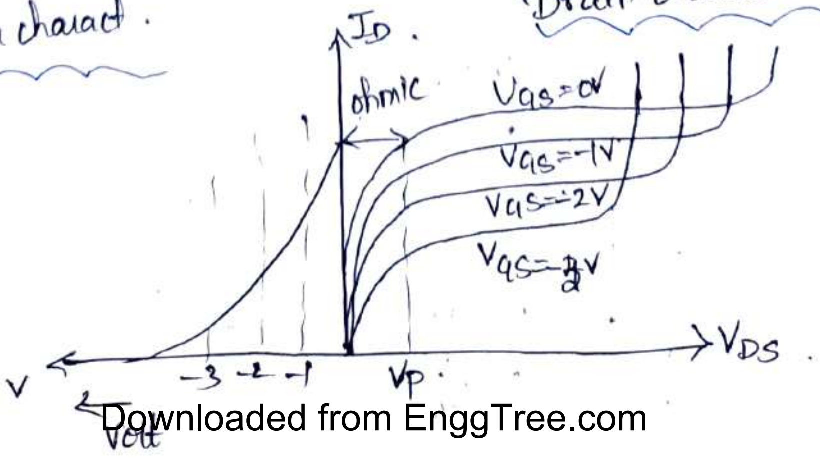


The relation b/w I_D & V_{GS} is non linear. It is given by shockley's eqn.

$$\boxed{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

Transfer charact.

Drain characteristics.



Case(i)

Drain characteristics with $V_{GS}=0$.

→ In this case the gate source voltage (V_{GS}) is at zero potential

→ A positive V_{DD} supply is given between drain and source terminal. The drain characteristics are plotted between I_D and V_{DS} with $V_{GS}=0V$.

→ when V_{DS} is increased by small amount, a small drain current flows and then only a slight change in depletion region.

Case(ii)

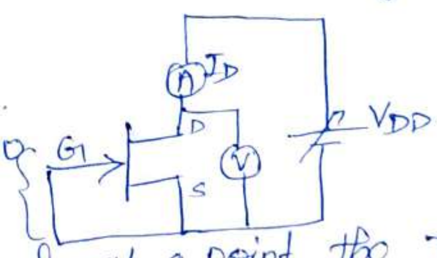
when V_{DS} is increased from zero, produces larger depletion region and increases the resistance and I_D conventional current increased linearly.

→ A saturation level of I_D reached, where further increasing V_{DS} has no effect on I_D.

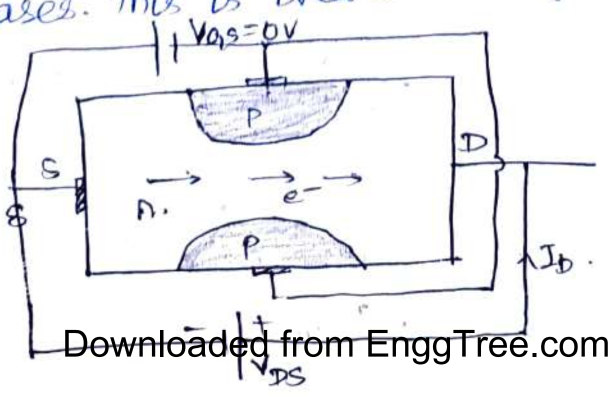
→ The point at which the I_D current becomes constant is known as drain source saturation current (I_{DSS}).

→ The shape of depletion region at I_{DSS} is appearing to pinch off the channel.

→ The region between $V_{DS}=0$ and $V_{DS}=V_P$ is called ohmic contact region.



→ when V_{DS} voltage is further increased at a point the I_D rapidly increases. This is breakdown region.

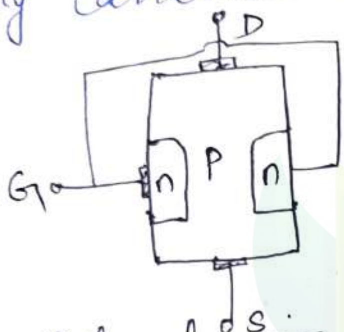


P-channel JFET:-

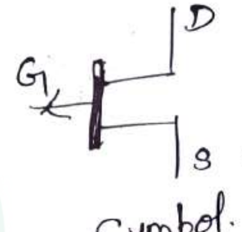
→ In P-channel JFET, P-type semiconductor is placed b/w two small pieces of n-type semiconductor.

→ The gate terminal of JFET is n-type material connected together, n-region is heavily doped.

→ The source 'S' is the terminal through which majority carriers enters the FET and drain is the terminal through which majority carriers leave the FET. P channel JFET majority carriers are holes in p-region.



P channel JFET

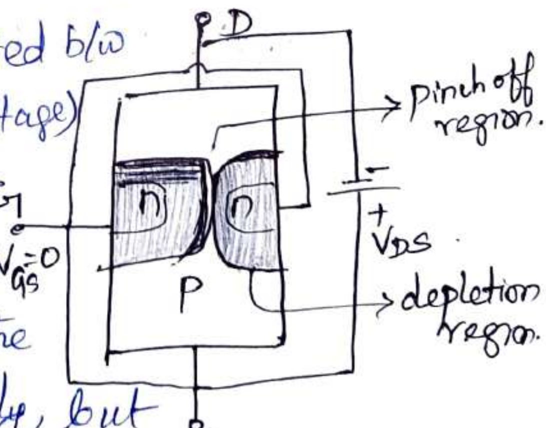


Symbol.

Case(i). Drain characteristics with $V_{GS}=0$.

→ A negative supply is given between drain & source terminal & at zero potential of gate-source voltage V_{GS}

→ The drain characteristics are plotted b/w I_D and V_{GS}. When V_{DS} (negative voltage) is increased the depletion increases which further increase the resistance

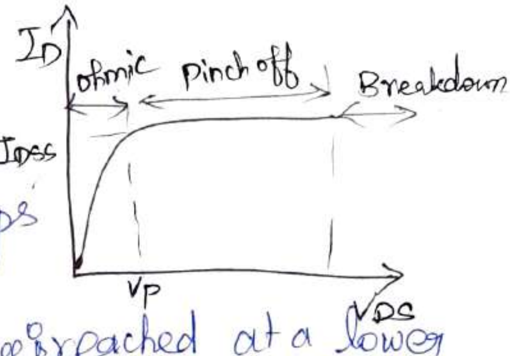


→ Initially with increase in $-V_{DS}$ the current I_D also increases linearly, but further increasing V_{DS} the depletion region is increased and I_D reduces.

→ The saturation level of I_D is reached where further increasing V_{DS} has no effect on I_D. The point at which I_D current becomes constant is I_{DSS} & shape of depletion appearing to pinch off channel.

→ The drain-source voltage at which, point is pinch off voltage V_p. The region between $V_{DS}=0$ & $V_p=V_{DS}$ is ohmic contact region.

→ when V_{DS} is increased, I_D current rapidly increases. This is called breakdown region.

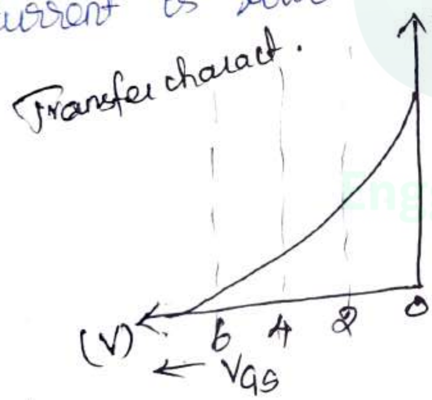


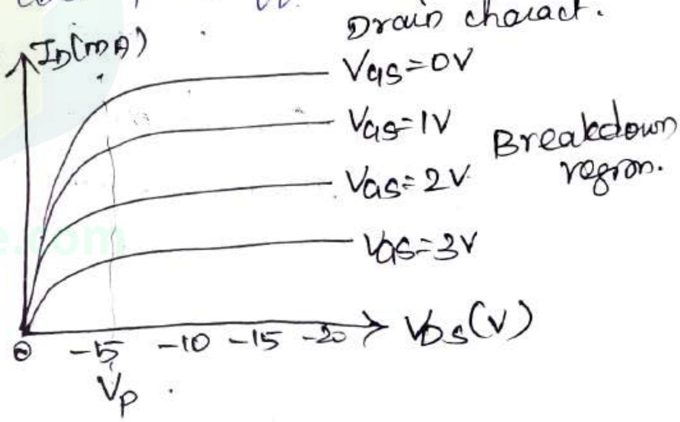
Case (ii) V_{GS} is +ve

→ the Gate-source voltage is set to positive value, V_{DS} is increased in steps and the I_D is noted.

→ when $V_{GS}=+1V$, the pinch off voltage is reached at a lower I_D current level than $V_{GS}=0$.

→ Similarly when further positive value 2V, 3V, 4V is applied and pinch off voltage is reduced. I_D current is lower than 1V





Advantages

i) High i/p resistance.
ii) High frequency response
iii) Small size, Better thermal stability
iv) High Power gain.
v) Long life.

Disadvantages

i) Low gain bandwidth.
ii) Require special handling during installation

Applications

i) Used in buffer in measuring instruments (Receivers).
ii) In operation Amplifier it is used.

Parameters of JFET :-

i) Transconductance (g_m)

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)_{V_{DS} = \text{constant}}.$$

ii) Drain Resistance (r_d)

$$r_d = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right)_{V_{GS} = \text{constant}}$$

iii) Amplification factor :-

$$\mu = g_m r_d \quad (\text{or}) \quad \mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D = \text{constant}}.$$

MOSFET :- [Metal oxide Field effect Transistor].

→ It is also called as Insulated gate field effect Transistor (IGFET) because MOSFET is insulated from the channel.

MOSFET
- Enhanced MOSFET
  - n-channel
  - p-channel
- Depletion MOSFET.
  - n channel
  - p channel.

Enhancement MOSFET.

→ The MOSFET is made of p-type semiconductor for N-channel MOSFET and n-type semiconductor for p-channel MOSFET. For n-channel MOSFET, over p type substrate, two n-channel blocks are present.

→ For p-channel MOSFET, over n type substrate, two p-channel blocks are present.

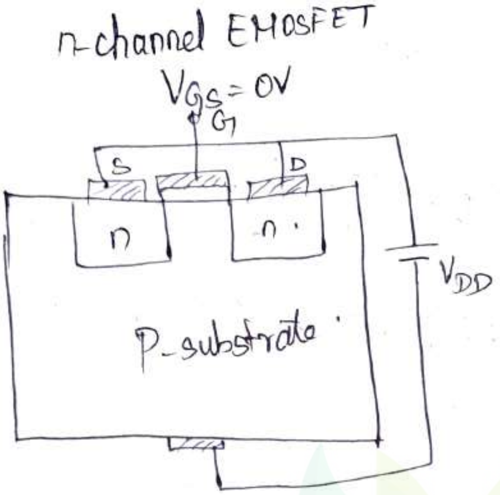
→ In n-channel the two n-type blocks becomes source and drain terminal with a metal plate attached.

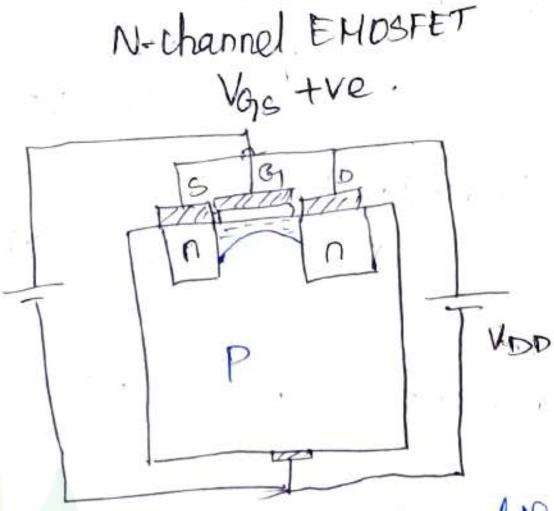
→ The Gate terminal is taken from metal plate connected to SiO_2.

WORKING:-

→ Two PN junctions are present and in E MOSFET there is no channel between source and drain.

→ It operates when V_{DD} is positive and Gate Voltage V_{GS} is positive.





→ When $V_{GS} = 0$, no current flows as there is no channel, thus MOSFET is OFF state.

→ V_{GS} is given +ve, the gate terminal acts as a plate of capacitor and '+ve' charge is created and in substrate negative ions accumulate to form a thin channel/layer. This is inversion layer.

→ The minimum V_{GS} producing inversion layer is called Threshold voltage and is designed as $V_{GS}(th)$.

Thus, $V_{GS} < V_{GS}(th)$ → no current flows from D to S

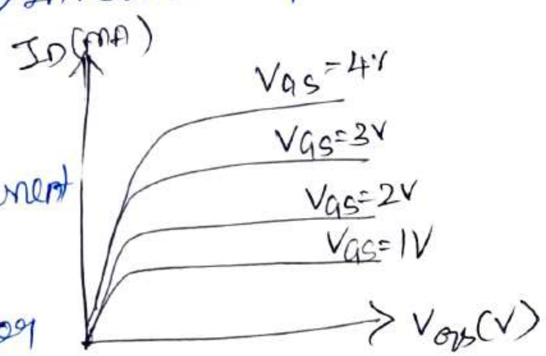
$V_{GS} > V_{GS}(th)$ → Inversion layer connect D to S

DRAIN CHARACTERISTICS:

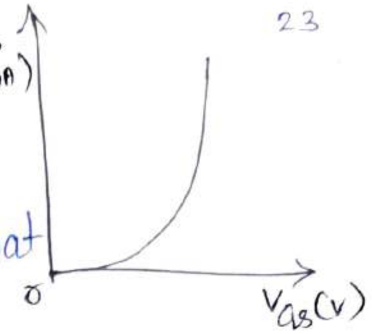
→ As the value of V_{GS} increased the current I_D increases.

→ When $V_{GS} > V_{GS}(th)$ the drain current flows.

→ The width of inversion layer or newly created n-channel increases



TRANSFER CHARACTERISTICS:-



→ The transfer characteristics gives the relation between I_D and V_{GS}.

→ When $V_{GS} > V_{GS}(Th)$, the drain current (I_D) at any point gives the relation.

$$I_D = K\left[V_{GS} - V_{GS}(Th)\right]^2.$$

K → Constant depending on type of MOSFET.

Depletion mode MOSFET:-

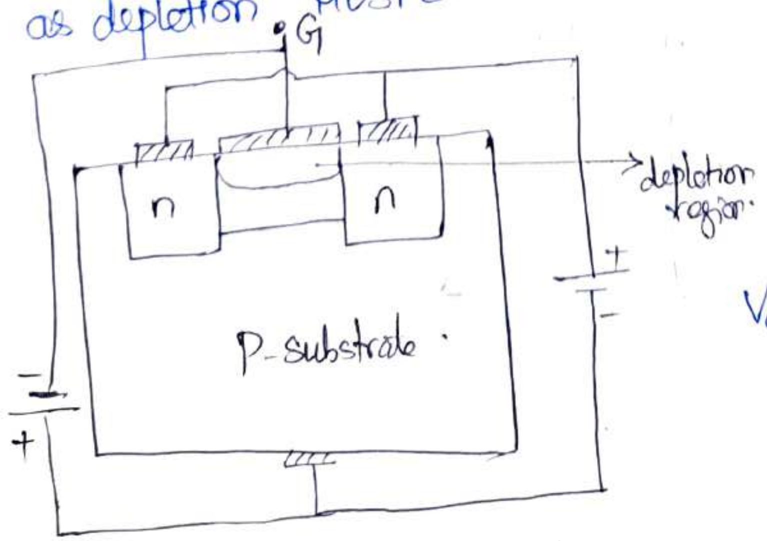
→ In depletion mode MOSFET there already exists a channel between source and drain.

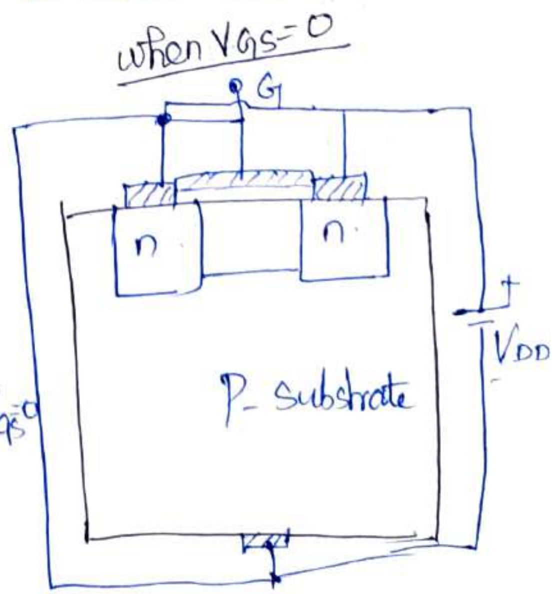
→ The drain source voltage V_{DS} is positive supply and gate source V_{GS} voltage is negative.

→ The negative voltage is applied on gate and thus free electrons are formed on gate. ie) acting as one plate of capacitor, because of this the channel is depleted of free electrons.

→ Because of this the current conduction between source to drain is reduced (I_D decreased, $-V_{GS}$ ↑)

→ As $-V_{GS}$ is further increased, the depletion region is also increased and I_D almost reduced to zero. Thus it is known as depletion MOSFET.



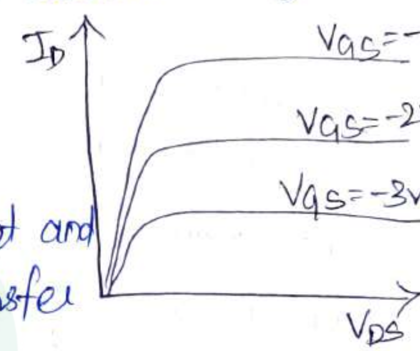


Drain characteristics of depletion MOSFET :-

→ When negative V_{GS} is given and V_{DD} is made positive, then the drain current (I_D) increases linearly.

→ When negative V_{GS} voltage is applied to gate, it induces negative charge/electrons on gate which act as one plate of capacitor.

→ Due to negative charges, the electrons in n-channel depletes and depletion region increases. The current through the channel also decreases.



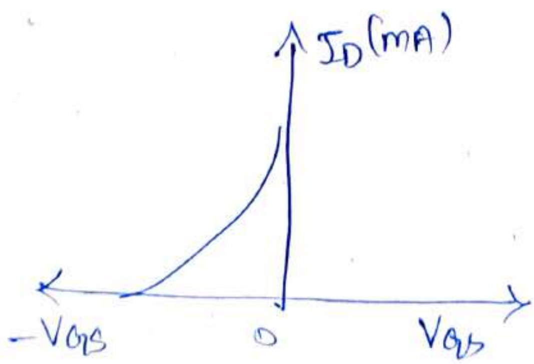
Transfer characteristics:-

→ The plot between drain current and gate source voltage (V_{GS}) gives the transfer characteristics of DMOSFET.

→ When $V_{GS}=0$ there is maximum current I_D flowing from source to drain.

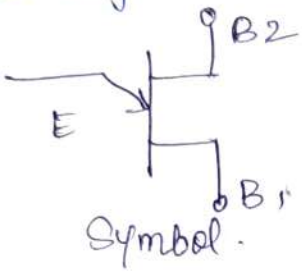
→ When negative V_{GS} is applied, it causes depletion region and I_D reduces.

→ If the V_{GS} supply is positively given the DMOSFET works as EMOSFET. Thus it is also known as depletion Enhancement MOSFET.

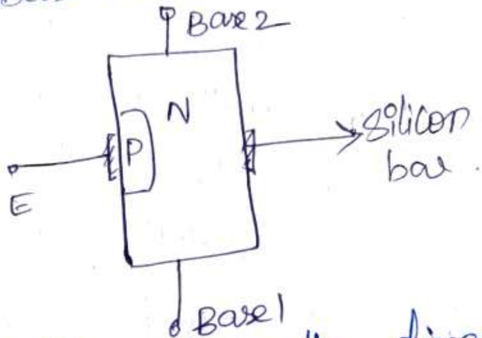


UJT [Unijunction Transistor].

→ Unijunction Transistor has only one PN junction and three terminals they are Emitter, base 1 & base 2.



Symbol.



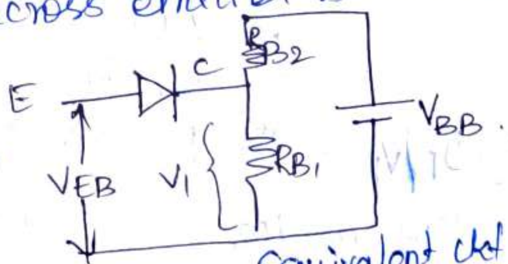
→ The arrow mark in Emitter shows the direction of Current in forward bias condition. The N-region in UJT is lightly doped and P-region is heavily doped.

→ It has negative resistance characteristics which makes it useful as an relaxation oscillator and switching. It is not used as an amplifier.

working:-

→ The equivalent circuit of UJT consists of diode and two base resistance in series.

→ Thus the voltage supplied across emitter is divided across Base 1 & 2 resistors.



Equivalent ckt.

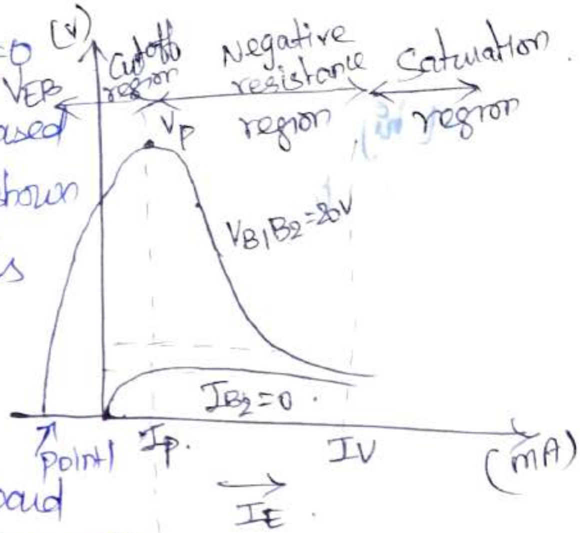
→ Using voltage division rule,

$$\boxed{V_1 = V_{BB} \cdot \frac{R_{B1}}{R_{B1}+R_{B2}}}$$

→ Initially the emitter voltage is reverse biased and emitter Current is so small. when the emitter voltage is increased from zero and when emitter voltage (V_{EB1}) equals V_1. $I_E = 0$.

→ when V_{EB} is further increased, it cross the n-region and through R_{B1} the resistance decreases and the voltage drop across it also decreases but the Current increases. This region is Negative resistance region. Thus the device is ON. region.

Characteristics:-



→ At $I_{B2}=0$, base voltage $V_{B1B2}=0$ and thus a graph for forward biased diode with some resistance is shown

→ At Point 1, the emitter voltage is reverse biased and only small emitter current flows till $I_E=0$

→ Then Emitter voltage is forward biased and current begins to increase.

→ The Emitter voltage is passed through RB1 and resistance decreases, so current increases while voltage is reduced/dropped across RB1. Thus the negative resistance region acts as UJT "ON"

→ when it goes beyond valley voltage/current then it enters Saturation region.

Parameters:-

i) Intrinsic stand off ratio (η)

$$\eta = \frac{R_{B1}}{R_{B1}+R_{B2}}$$

ii) I_P/V_P:- The peak voltage/peak current denotes the point at which device starts showing negative resistive characteristics

iii) I_V/V_V:- The valley voltage/current at the point above which the device is in saturation region

iv) V_{EB} Saturation:- The V_{EB} sat is the voltage above which the device is saturated.

UJT application:-

i) Non sinusoidal oscillator.

ii) phase control

iii) Timing circuit.

iv) Sawtooth generator

UJT Relaxation Oscillator

$$\boxed{V_P = \eta V_{BB} + V_D} \quad \text{--- (1)}$$

$\eta \rightarrow$ stand off ratio of UJT
$V_D \rightarrow$ cut in voltage of diode.

$$V_C = V_V + V_{BB}\left[1 - e^{-t/R_T C_T}\right]$$

$V_C = V_P$ at $t = T$.

$$V_P = V_V + V_{BB}\left[1 - e^{-T/R_T C_T}\right] \quad \text{--- (2)}$$

Equating (1) & (2)

$$\eta V_{BB} + V_D = V_V + V_{BB}\left[1 - e^{-T/R_T C_T}\right]$$

Neglect V_D & V_V.

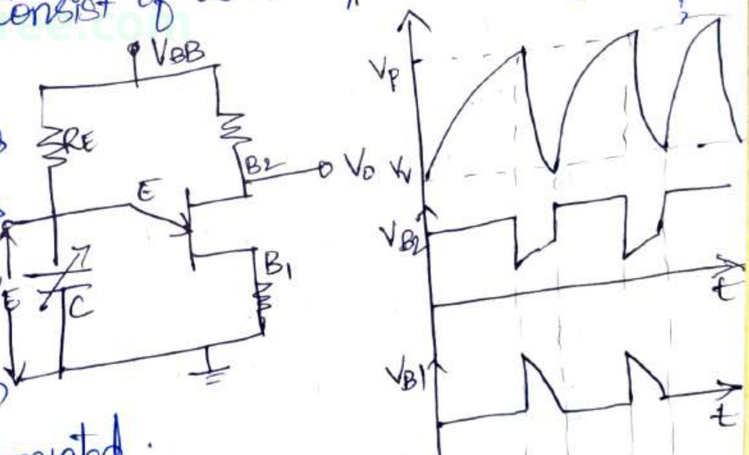
$$\eta = 1 - e^{-T/R_T C_T}$$

$$\boxed{T = R_T C_T \ln\left[\frac{1}{1-\eta}\right]}$$

$$f_o = \frac{1}{T} = \frac{1}{R_T C_T \ln\left[\frac{1}{1-\eta}\right]}$$

f_o = oscillating frequency.

→ The Relaxation oscillator Consist of UJT, capacitor charged via Resistance R_E.



→ when capacitor voltage reaches V_P, the UJT fires and discharges C_1 to $V_{BE(sat)}$

→ The device then cut-off and Capacitor starts charging again and sawtooth waveform is generated.

→ The time (t) for capacitor to charge from $V_{EB(sat)}$ to V_P. The resistance across base produces an spike waveform.

$$\boxed{T = 2.303 R_E C_E \log_{10}\left(\frac{1}{1-\eta}\right)}$$

THYRISTOR:-

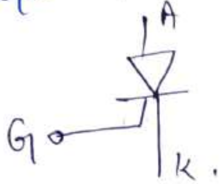
The SCR type power devices with 4 layers i.e) pnpn are known as thyristors. This term is derived from thyratron and transistor. The thyratron is a gas filled electron tube

SILICON CONTROLLED RECTIFIER (SCR).

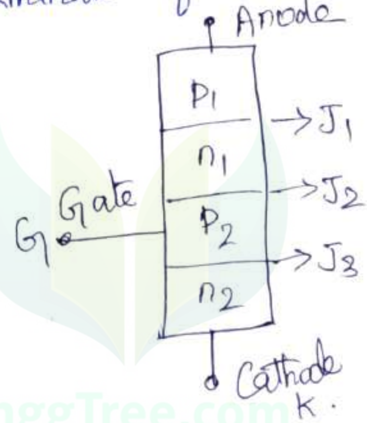
Construction:-

→ The SCR is a four layers diode or pnpn device, alternatively made up of p and n type semiconductor material and there are 3 junctions

→ It is denoted as P_1, n_1, P_2, n_2 and there are 3 junctions J_1, J_2, J_3. The 3 terminals of SCR are Anode A, cathode k and Gate G.



Symbol SCR

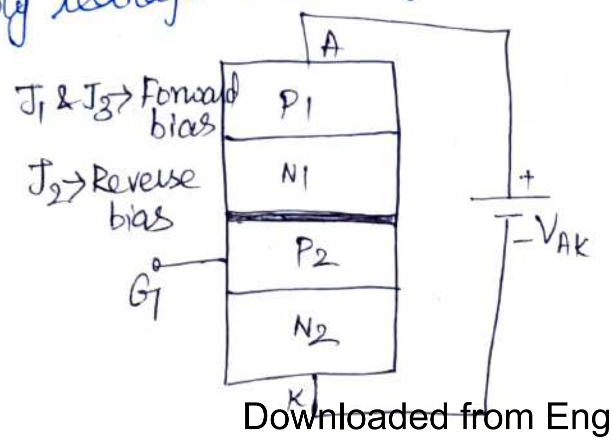


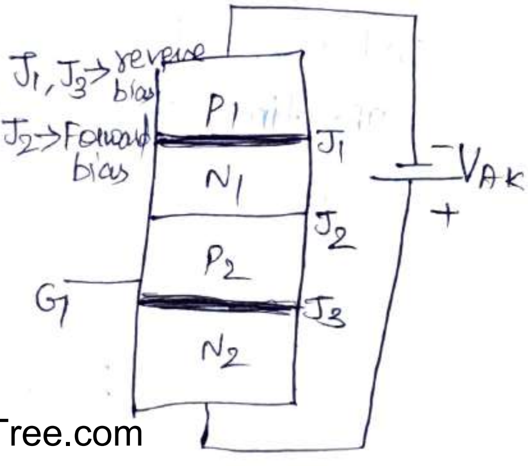
Working:-

when Gate is open:-

Forward bias condition:-

→ consider that the anode is +ve with respect to cathode and gate is open. The junction J_1 & J_3 are forward biased and J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows ≃ small. The SCR is OFF.

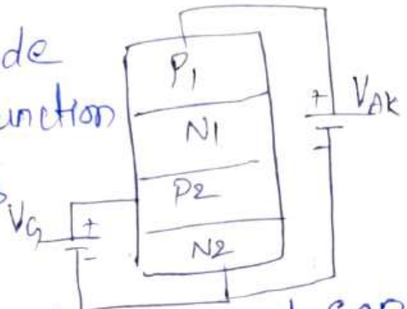




Reverse bias Condition:

→ with Gate open, cathode is positive & anode is −ve. J_1 & J_3 becomes reverse biased and J_2 is forward biased. Still the current flowing is leakage current. ≃ small.

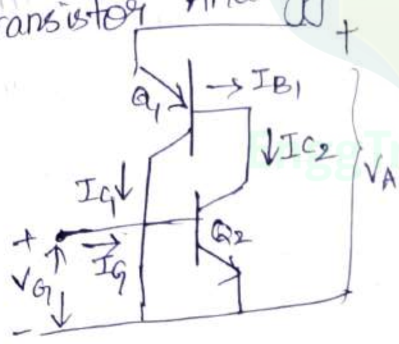
When the Gate is closed:-



1) When Gate is +ve, electrons from cathode which are majority in number, cross the junction J_3 to reach +ve of battery. lly holes from p-type move towards negative of battery. Due to regenerative action J_2 breaks and SCR Conducts heavily.

→ If anode to cathode voltage reversed, then device enters to reverse breakdown reverse blocking region. This is called reverse breakdown.

Two Transistor Analogy:-



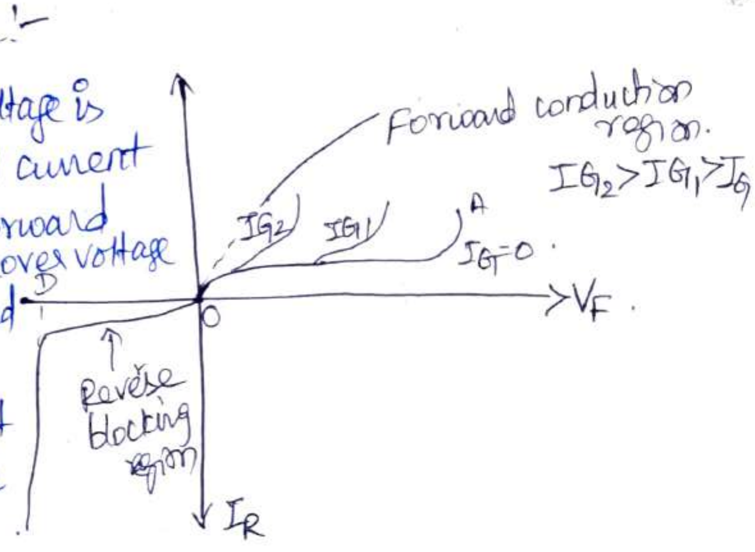
When Gate voltage is forward biased, SCR is ON.

* If Transistors remain ON, even I_G is switched off It is called Latching.

VI characteristics of SCR:-

→ when anode to cathode voltage is increased above zero, a small current flows through the device → Forward breakover voltage

→ when V_{AK} exceeds Forward breakover voltage it conducts heavily than SCR turns ON. At this stage SCR allows more current to flow through it



→ Holding Current is defined as minimum value of anode Current required to keep SCR in ON state. If SCR falls below the holding current SCR turns off.

→ when gate voltage is forward biased the SCR further conducts and current increases. As the Gate voltage reversed, only a small current flows through SCR and thus SCR is OFF state until the applied reverse voltage reaches breakdown voltage.

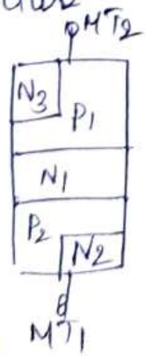
→ When voltage is increased beyond breakdown voltage avalanche breakdown occurs hence SCR starts conducting in reverse direction.

Application:-
i) Relay Controls ii) Motor control. iii) RPS iv) Inverters

DIAC [Diode AC Switch].

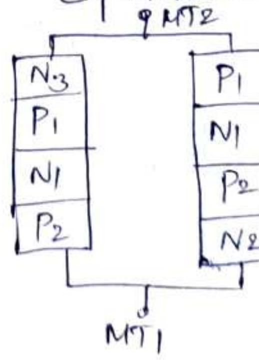
DIAC is a 3 layer, two terminal semiconductor device, it acts as bidirectional device conduct current in either direction when the breakover voltage is reached in either polarity across the two terminals (MT_1 & MT_2) ⇒ Interchangable.

Structure



Symbol

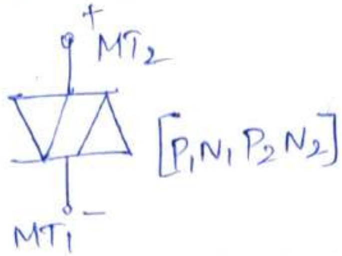
Equivalent ckt.

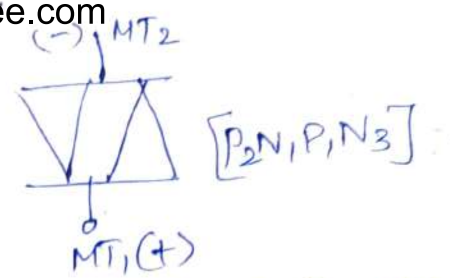


Operation:-

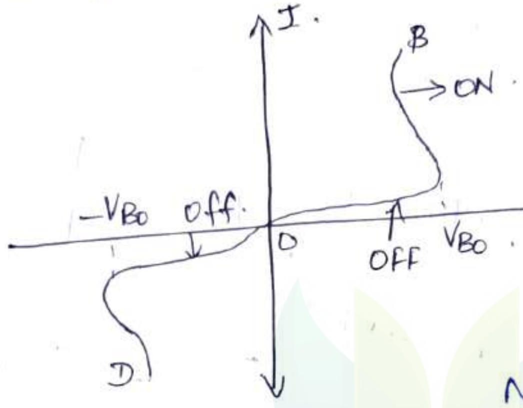
→ It acts like a 2, 4 layer diodes connected in parallel but in opposite directions are $P_1 N_1 P_2 N_2$ & $P_2 N_1 P_1 N_3$

→ The DIAC can pass current in either direction depending upon the polarity of voltage across its main terminal reaches the breakover voltage.





→ The doping level at the two ends of device are same, the DIAC has identical characteristics for both positive to negative half of AC cycle. It will OFF when voltage fall below holding voltage.



→ At voltage less than V_{BO} very small current flows called leakage current.

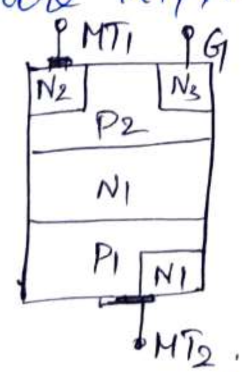
→ when voltage b/w MT_1 & MT_2 reaches V_{BO}, device starts conducting and it exhibit negative resistance characteristics.

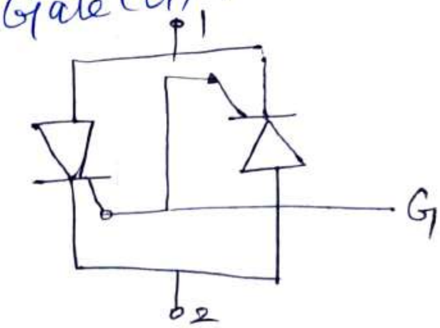
Application:-

→ It is not a control device, it is used as triggering device in speed, heat and dimming control.

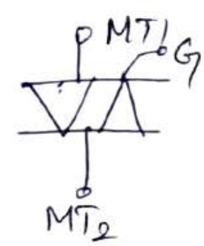
TRIAC [Triode AC switch].

TRIAC is three terminal semiconductor switching device which can control alternating current in load. Its three terminals are MT_1, MT_2 and Gate (G).





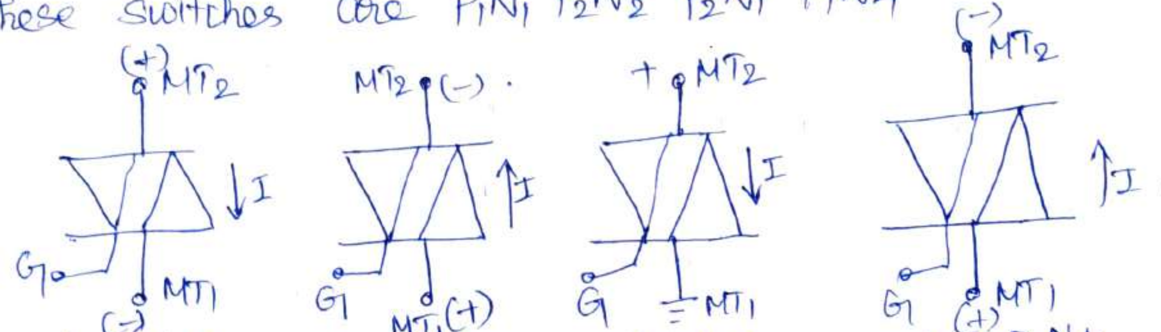
symbol



Operation:-

→ The anode and gate voltage applied in either direction will trigger the Triac. It is due to fact that the applied voltage will trigger either one of SCR connected in opposite direction

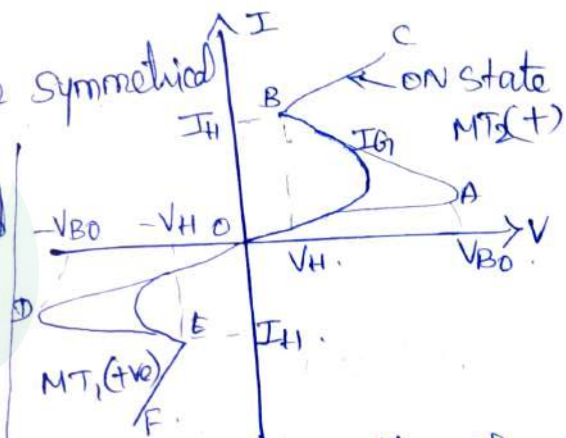
→ The TRIAC consist of two four layer switches in parallel. These switches are P_1N_1 P_2N_2 P_2N_1 P_1N_4



$P_1N_1P_2N_2$ (a) $P_2N_1P_1N_4$ (b) $P_1N_1P_2N_2$ (c) $P_2N_1P_1N_4$ (d)

mode (a) & (d) are efficient modes. It is turned off by reducing the device current below holding current.

VI characteristics:-



→ The curve OABC and ODEF are symmetrical and identical.

→ The TRIAC is OFF until the applied voltage of either polarity (MT_2 w.r to MT_1 or MT_1 w.r to MT_2) exceeds the breakover voltage. As the applied voltage of either polarity exceeds the breakover voltage the triac turns ON and voltage drop across the triac decreases to low value. The TRIAC current increases to voltage determined by supply voltage and load resistance. if $I_G > 0$, breakover voltage is lowered.

Application:-

1) Illumination Control
2) Temperature Control
3) Liquid level "
4) Motor speed control.
5) Switch control.

BJT BIASING

The Process of giving Proper supply voltages and resistances for obtaining the desired Q-point (Quiescent point or operating Point) to the transistor.

Need for Biasing:-

→ To produce distortion free o/p in amplifier circuit.

→ To Set V_{CQ} & I_{CQ} to operate transistor in active region.

Note:-

→ Q-Point Shift due to Temperature changes

→ Collector current in CE

$$I_C = \beta I_B + I_{CEO} \Rightarrow \beta I_B + (1+\beta) I_{CO}.$$

$\boxed{\beta, I_B, I_{CO}}$ → depends on Temp.

Requirements of Transistor Biasing:-

→ Transistor to be operated in active region to act as Amplifier.

→ In saturation & Cutoff ⇒ Act as switch.

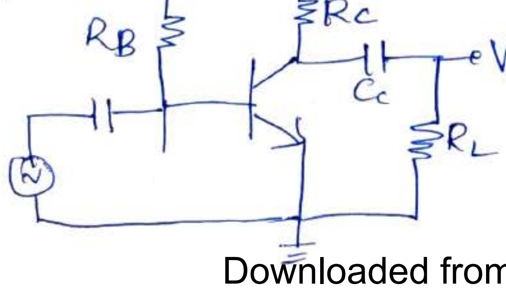
→ Q Point should be adjusted at the centre of load line for voltage amplification.

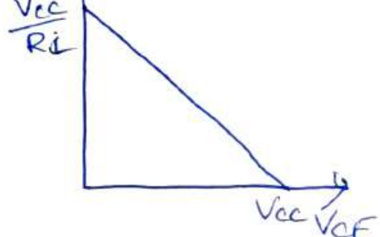
→ Value of stability factor 'S' should be small as possible

→ Q-Point stabilised by negative feedback in biasing ckt.

DC Load line:-

→ A load line which is drawn on o/p characteristics of transistor under DC operating condition without AC s/g at input.





Apply KVL to collector ckt,

$$V_{CC} = I_C R_C + V_{CE} \longrightarrow (1)$$

Sub $V_{CE} = 0$.

$$I_C = \frac{V_{CC}}{R_C}$$

Point A (V_{CE}, I_C)

$$\Rightarrow \left(0, \frac{V_{CC}}{R_C}\right)$$

Sub $I_C = 0$.

$$V_{CC} = V_{CE}$$

So point B (V_{CE}, I_C)

$$\Rightarrow (V_{CC}, 0)$$

Q - Point $\Rightarrow$ On the load line which represents DC current through transistor I_{CQ} and voltage across it V_{CEQ} with no AC s/g applied

→ Reverse saturation current double for ↑10°C.

→ V_{BE} ↓ by 2.5mV per °C.

→ β ↑ with Temp.

Stability Factor (S) :-

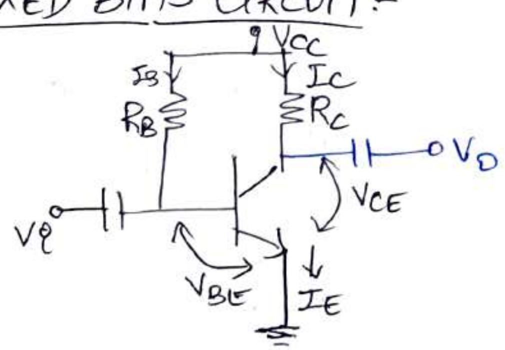
'S' is defined as rate of change of collector current I_C with respect to reverse saturation current I_{CO} at constant β & I_B

$$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{I_B, \beta \to \text{constant}}$$

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO}, \beta \to \text{Constant}}$$

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO}, V_{BE} \to \text{Constant}}$$

FIXED BIAS CIRCUIT :-



NPN Transistor base is Positive than Emitter.

I/P side. Apply KVL,

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B}}$$

Stability factor :-

$$\boxed{S = 1 + \beta}$$

O/p side Apply KVL,

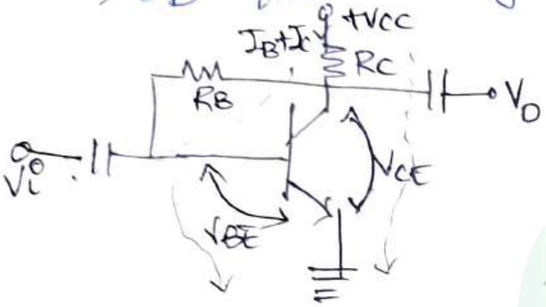
$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}}$$

2) Collector to Base bias. [DC with voltage feedback].

→ In this biasing resistor is connected between collector and base of transistor to provide a voltage feedback path.

→ I_B flows through R_B and $(I_C + I_B)$ flows to R_C.



I/p side (KVL)

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_B R_C + I_C R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_B (R_B + R_C) + I_C R_C + V_{BE}$$

$$\boxed{I_C = \beta I_B}$$

$$V_{CC} = I_B (R_B + R_C) + \beta I_B R_C + V_{BE}$$

$$V_{CC} = I_B (R_B + \beta R_C + R_C) + V_{BE}$$

$$V_{CC} = I_B (R_B + (1+\beta) R_C) + V_{BE}$$

$$\boxed{\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C}}$$

O/p side:-

$$(I_B + I_C) R_C = V_{CC} - V_{CE}$$

$$V_{CC} - (I_B + I_C) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_B + I_C) R_C$$

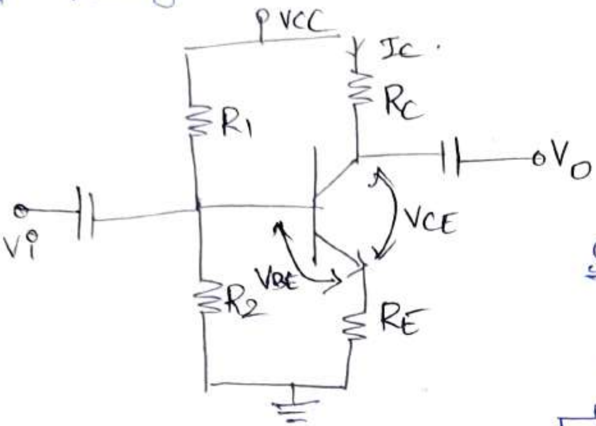
$$\boxed{R_C = \frac{V_{CC} - V_{CE}}{I_B + I_C}}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C + R_B}\right)}}$$

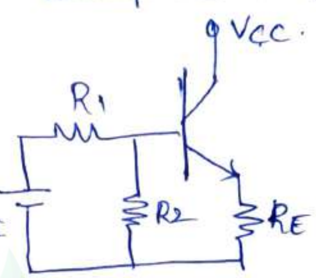
VOLTAGE DIVIDER BIAS (self bias) (emitter bias)

→ It is a circuit used to establish a stable Q-point.

→ The resistors R_1 & R_2 act as potential divider giving a fixed voltage to point B which is base.



Simplified diagram



R_{Th} : R_B

To find R_{Th} the voltage source is replaced by short ckt.

$$R_{Th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}.$$

I/P

$$V_T - I_B R_B - V_{BE} - \underset{\uparrow\, I_B + I_C}{I_E} R_E = 0.$$

$$V_T - I_B R_B - V_{BE} - I_B R_E - I_C R_E = 0$$

$$I_C = \beta . I_B$$

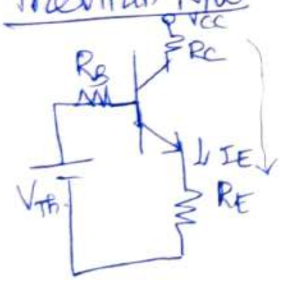
we get,

$$\boxed{I_B = \frac{V_T - V_{BE}}{R_B + (1+\beta) R_E}}$$

V_{Th}

$$V_{Th} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

Thevinin N/W



O/P

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$I_E = I_C + I_B. \quad \boxed{I_E \approx I_C}$$

$$\therefore I_B = 0.$$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0.$$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Stability factor:-

I/P eqn ⇒ $V_T - I_B (R_B + R_E) - V_{BE} - I_C R_E = 0$ — (1)

$$S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Differentiating, (1) $\frac{\partial I_B}{\partial I_C}$.

$$0 - \frac{\partial I_B}{\partial I_C}(R_B + R_E) - 0 - R_E = 0.$$

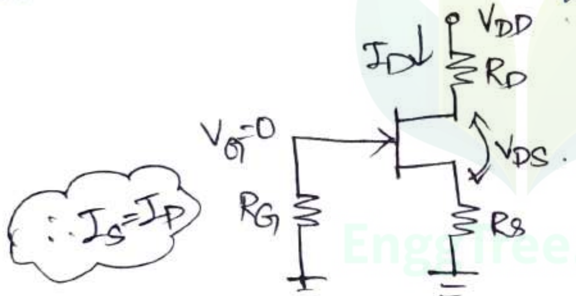
$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E} \qquad \therefore \boxed{S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B + R_E}\right)}}$$

→ Fixed Bias (Gate Bias)
→ self bias
→ voltage divider bias.

Self bias:-

→ In a self bias circuit, Gate source bias is provided (V_{gs}) by the voltage drop across a resistor in series with the device source terminal. JFET must be operated with reverse biased gate source (V_{gs}) voltage.

→ For n channel JFET, V_{gs} should be negative and for p-channel V_{gs} should be positive. when the drain voltage V_{DD} is applied, drain current I_D flows in absence of V_{GS} ($V_{GG} = 0V$)



→ The voltage across resistor R_S produced by drain current

$$\boxed{V_S = I_D R_S}$$

→ The voltage drop reduces the V_{gs} reverse voltage for JFET operation.

$V_D = V_{DD} - I_D R_D$.

The Drain to source voltage,

$$V_{DS} = V_D - V_S.$$
$$= (V_{DD} - I_D R_D) - I_D R_S.$$
$$\boxed{V_{DS} = V_{DD} - (R_D + R_S) I_D}$$

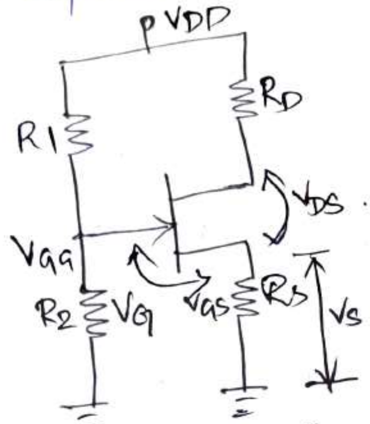
Gate to source voltage,

$$V_{GS} = V_{GG} - V_S \Rightarrow 0 - I_D R_S.$$
$$\boxed{V_{GS} = -I_D R_S}$$

When drain current increases, V_S increases due to this reverse gate to source voltage increases which decreases effective width of channel & reduces I_D.

Voltage divider Bias :-

→ Resistors R_1 & R_2 connected on the gate side forms a voltage divider. It combines the use of source resistor R_S with a gate bias voltage is derived from voltage divider (R_1 and R_2) and source voltage depends on R_S & I_D.



Source voltage,

$$\boxed{V_S = I_D R_S}$$

Gate voltage

$$\boxed{V_{GG} = V_{DD} \times \left(\frac{R_2}{R_1+R_2}\right)}$$

I/P

$V_G - V_{GS} - V_S = 0$

$V_{GS} = V_G - V_S \Rightarrow V_G - I_D R_S$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

O/P

$V_{DD} - I_D R_D - V_S - V_{DS} = 0$

$V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$$\boxed{V_{DS} = V_{DD} - I_D(R_D + R_S)}$$

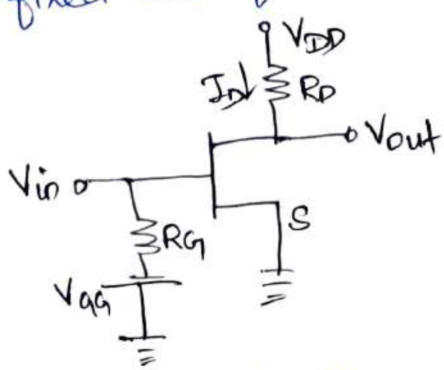
Q-point

$V_{DSQ} = V_{DD} - I_D(R_D + R_S)$

$$\boxed{I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

FIXED BIAS (Gate bias).

The fixed bias for N-channel JFET is,



∴ Since no gate current to produce a voltage drop across R_G the gate-source voltage remains constant at ~~RG~~ V_G.

$V_{GS} = V_G - V_S \Rightarrow -V_{GG} - 0$

$\Rightarrow -V_{GG}$

Voltage drop across R_D,

$$V_{DD} = I_D R_D + V_{DS}$$

$$\therefore \boxed{I_D = \frac{V_{DD} - V_{DS}}{R_D}}$$

MOSFET BIASING:-

→ Zero bias.
→ voltage divider bias
→ Drain feedback bias.

D-MOSFET BIAS:- (Zero bias)

→ It is operated either positive or negative value of V_{GS}.

→ A simple bias method to set $V_{GS}=0$. So AC s/g at gate varies the gate to source voltage above or below 0V.

$V_{GS}=0$.

$I_D = I_{DSS}$.

The drain to source voltage is,

$$\boxed{V_{DS} = V_{DD} - I_{DSS} R_D}$$

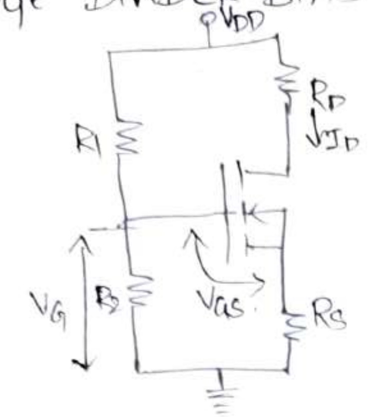
→ $V_{GS}=0, I_G=0$. There is no DC Gate current.

E-MOSFET:-

→ It must have V_{GS} greater than threshold value, so zero bias cannot be used.

→ Two ways to bias E-MOSFET are voltage divider bias and drain feedback bias.

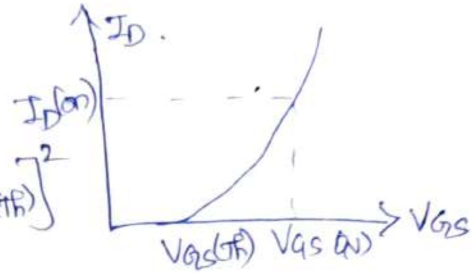
VOLTAGE DIVIDER BIAS



$$V_G = V_{DD}\left(\frac{R_2}{R_1+R_2}\right)$$

$$\boxed{V_{GS} = V_G - I_D R_S}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$



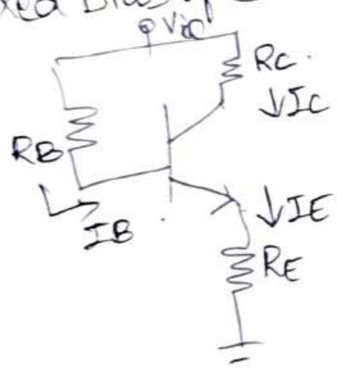
when, $V_{GS} < V_{GS(Th)}$, $I_D = 0$

$V_{GS} > V_{GS(Th)}$, $I_D = K\left[V_{GS} - V_{GS(Th)}\right]^2$

$$K = \frac{I_{D(on)}}{\left[V_{GS(on)} - V_{GS(Th)}\right]^2}$$

Fixed bias of BJT with Emitter resistance:-

To find, I_B, I_C, V_{CE}, S.



To find V_{CE}

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

9) $V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + I_C)R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (I_B + \beta I_B)R_E = 0$$

$$V_{CC} - V_{BE} = I_B R_B + (I_B + \beta I_B)R_E$$

$$V_{CC} - V_{BE} = I_B\left[R_B + (1+\beta)R_E\right]$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$\boxed{I_C = \beta I_B}$$

$$S = \frac{\beta + 1}{1 - \beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

Take i/p eqn.

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Diff w.r.to I_C.

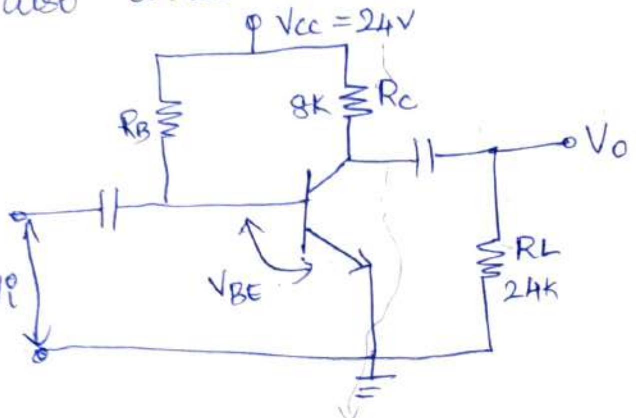
$$-\frac{\partial I_B}{\partial I_C} R_B - 0 - \frac{\partial I_B}{\partial I_C} R_E - R_E = 0$$

$$-\frac{\partial I_B}{\partial I_C}(R_B + R_E) = R_E$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_B + R_E}$$

$$S = \frac{\beta + 1}{1 - \beta\left(\frac{-R_E}{R_B + R_E}\right)}$$

1) In the transistor amplifier $R_C = 8K\Omega$, $R_L = 24K\Omega$ and $V_{CC} = 24V$. Draw the load line and determine the optimum operating point also draw the AC load line.



$$V_{CC} - V_{CE} - I_C R_C = 0$$

Put $V_{CE} = 0$.

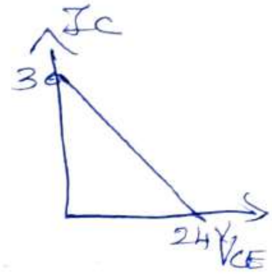
$$24 = 0 + I_C(8\times10^3)$$

$$\boxed{I_C = 3mA}$$

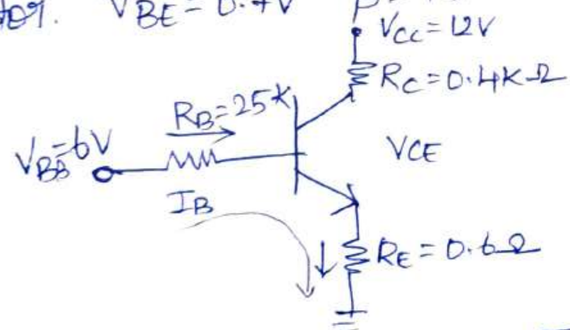
Put $I_C = 0$.

$$V_{CC} = V_{CE}$$

$$\boxed{V_{CE} = 24V}$$



2) Calculate the characteristics of circuit containing an emitter resistor. $V_{BE} = 0.7V$ $\beta = 75$



$$V_{BB} - I_B R_B - V_{BE} - I_E R_E = 0$$

$\because \boxed{I_E = (\beta+1) I_B}$

$I_E = I_C + I_B$

$I_E = \beta I_B + I_B$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (1+\beta)R_E}$$

$$= \frac{6 - 0.7}{25\times10^3 + (76)(0.6\times10^3)}$$

$$\boxed{I_B = 75\mu A}$$

$$I_C = \beta I_B$$

$$= (75)(75.1\times10^{-6})$$

$$\boxed{I_C = 5.63mA}$$

$$I_E = (1+\beta)I_B \Rightarrow (76)(75\times10^{-6})$$

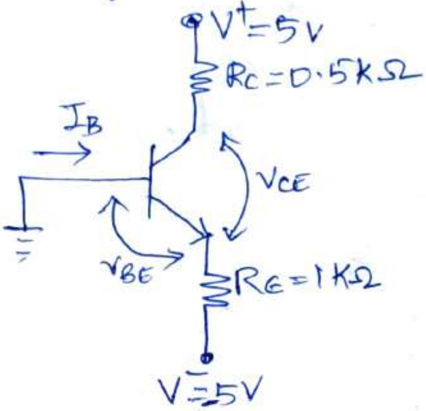
$$= 5.71mA$$

$$V_{CC} - V_{CE} - I_C R_C - I_E R_E = 0$$

$$V_{CE} = 12 - (5.63\times10^{-3})(0.4\times10^{3}) - (5.7\times10^{-3})(0.6\times10^3)$$

$$\boxed{V_{CE} = 6.32V}$$

3) Calculate the characteristics of circuit both +ve and -ve. Power supply voltage. $V_{BE}=0.65V$ & $\beta=100$



$0-V_{BE}-I_ER_E+5=0$

$I_E=\frac{5-0.7}{1\times10^3}$

$\boxed{I_E=4.35mA}$

$I_B=\frac{I_E}{1+\beta}$ $\{I_E=(1+\beta)I_B\}$

$I_B=\frac{4.35\times10^{-3}}{1+100}$

$\boxed{I_B=43.1\mu A}$

$I_C=\beta I_B$

$I_C=100\times43.1\times10^{-6}$

$\boxed{I_C=4.31mA}$

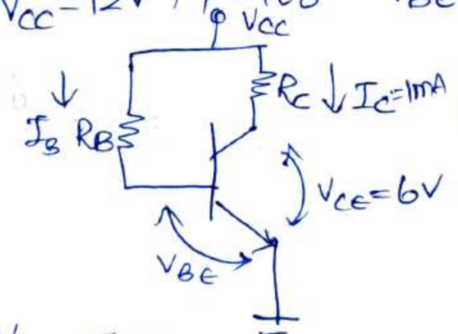
To find VCE

$V_C-I_CR_C-V_{CE}-I_ER_E+5=0$

$V_{CE}=5+5-(4.3\times10^{-3})(0.5\times10^3)$
$-(4.3\times10^{-3})(1\times10^3)$

$\boxed{V_{CE}=3.50V}$

4) HW
Given. $V_{CC}=12V$, $\beta=100$ $V_{BE}=0.7V$.



Find R_B & R_C.

To find I_B

$I_B=\frac{I_C}{\beta}=\frac{1mA}{100}$.

$I_B=10\mu A$

$V_{CC}-I_BR_B-V_{BE}=0$.

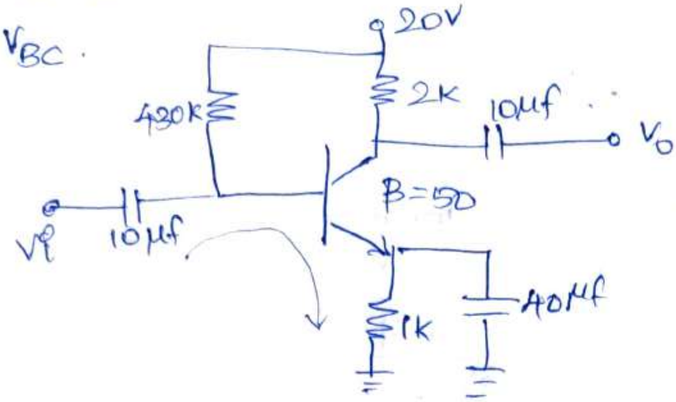
$12-I_BR_B-0.7=0$.

$\boxed{R_B=16K\Omega}$

$V_{CC}-I_CR_C-V_{CE}=0$.

$\boxed{R_C=6K\Omega}$

5) For the Emitter bias Network, Find $I_B, I_C, V_{CE}, V_C, V_E, V_B$ and V_{BC}.



$I_E = (1+\beta)I_B$

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$

$V_{CC} - V_{BE} - I_B\left[(1+\beta)R_E + R_B\right] = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_E} = \frac{20 - 0.7}{430\times10^3 + (1+50)1\times10^3}$$

$\boxed{I_B = 40.13\mu A}$

$I_E = (1+\beta)I_B$

$\boxed{I_E = 2.046mA}$

$V_E = \cancel{V}I_E R_E = 2.046\times10^{-3}\times1\times10^3 = 2.046V$

$\boxed{V_E = 2.046V}$

$V_B = V_E + V_{BE}$

$\boxed{V_B = 2.746V}$

$V_C = V_{CC} - I_C R_C = 20 - (2\times10^{-3}\times2\times10^3) = 16V$

(or)

$V_C = V_{CE} + I_E R_E = 16V$

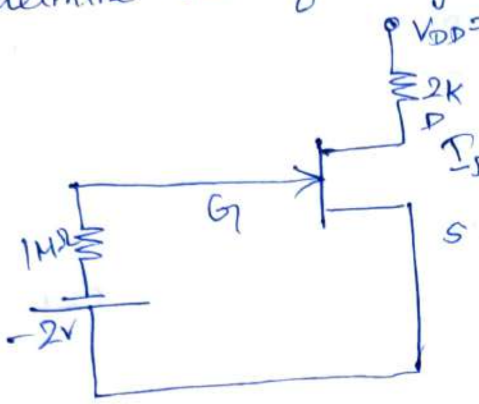
$V_{CE} = V_C - V_E = 16 - 2.046 = 13.954V$

$V_{BC} = V_B - V_C \Rightarrow 2.746 - 16$

$\boxed{V_{BC} = -13.25V}$

FET

1) Determine the following.



$I_{DSS} = 10mA$
$V_p = -8V$

Find
i) V_{GS}
ii) V_{DS}
iii) I_D
iv) V_D
v) V_G.
vi) V_S.

Formula

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$V_{DS} = V_{DD} - I_D R_D$

$V_D = V_{DS}$

$V_G = V_{GS}$.

i) $V_{GS} = -V_{GG} = -2V$

ii) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10\times10^{-3}\left(1 - \frac{-2}{-8}\right)^2$

$\boxed{I_D = 5.62mA}$

iii) $V_{DD} - V_{DS} - I_D R_D = 0$.

$V_{DS} = V_{DD} - I_D R_D$

$= 16 - (5.62\times10^{-3} \times 2\times10^{3})$

$\boxed{V_{DS} = 4.75V}$

iv) $V_D = V_{DS}$.

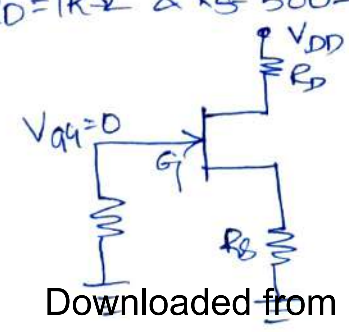
v) $V_G = V_{GS} \Rightarrow -2V$

vi) $V_S = 0V$.

2) HW

$I_{DSS} = 15mA$, $V_p = -10$; $R_D = 1k$, $V_{DD} = 15V$, $V_{GG} = -3V$.

3) For the self bias ckt, find V_{DS} & V_{GS}; $I_D = 5mA$, $V_{DD} = 10V$, $R_D = 1k\Omega$ & $R_S = 500\Omega$



i) $V_{GS} = V_G - I_D R_S$

$$V_G = \frac{R_2}{R_1+R_2} \times V_{DD}$$

$$= \frac{90\times10^3}{(450+90)\times10^3} \times 18$$

$$\boxed{V_G = 3V}$$

$$V_{GS} = 3 - 2\times10^3 I_D$$

ii) $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

$$= 10\times10^{-3}\left[1 - \frac{3-2\times10^3 I_D}{-4}\right]^2$$

$$= \frac{10\times10^{-3}}{16}\left[4+3-2\times10^3 I_D\right]^2$$

$$16 I_D = 10^{-3}\left[7-2\times10^3 I_D\right]^2 \Rightarrow I_D = \frac{29.6 \pm \sqrt{(29.6)^2 - 4\times4\times10^3\times0.049}}{2\times4\times10^3}$$

$$\boxed{I_D = 4.9mA}$$

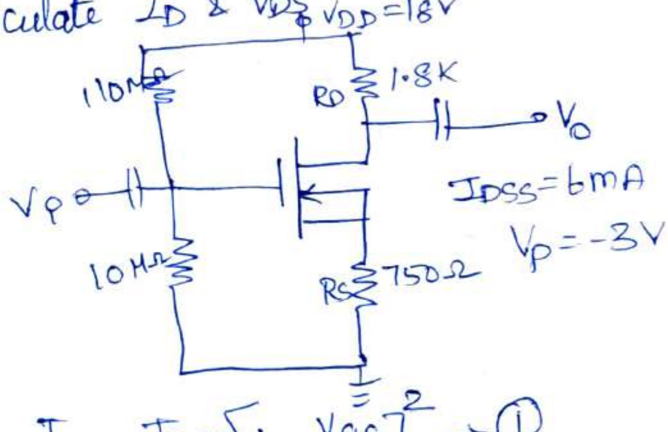
iii) $V_{DS} = V_{DD} - I_D(R_D+R_S)$

$$= 18 - 2.5\times10^{-3}(2+2)\times10^3$$

$$\boxed{V_{DS} = 8V}$$

MOSFET PROBLEMS:-

1) Calculate I_D & V_{DS}



$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \rightarrow (1)$$

$$V_{GS} = V_G - I_D R_S \Rightarrow V_G = \frac{R_2}{R_1+R_2}\times V_{DD} = \frac{10\times10^{+6}}{(10+110)\times10^6}\times18 = 1.5V$$

$$V_{GS} = 1.5 - 750 I_D \rightarrow (2)$$

Sub 2 in 1

$$I_D = 6\times10^{-3}\left[1-\frac{1.5-250I_D}{-3}\right]^2$$

$$= 6\times10^{-3}\left[1.5-250I_D\right]^2$$

$$I_D = 6\times10^{-3}\left[2.25-750I_D+62500I_D^2\right]$$

$$I_D = 0.0135-5.5I_D+375I_D^2$$

$$I_D = \frac{-b\pm\sqrt{b^2-4ac}}{2a}$$

$$= \frac{5.5\pm\sqrt{(5.5)^2-4(375\times0.0135)}}{2\times375}$$

$$\boxed{I_D = 8.11mA \text{ (or) } 11.55mA}$$

At 11.55mA $V_{DS} = V_{DD} - I_D(R_D+R_S)$

$$= 18-11.55(1.8+0.75)$$

$$\boxed{V_{DS} = -11.45V}$$

At 8.11mA $V_{DS} = 18-8.11\times10^{-3}[1.8+0.75]\times10^{3}$

$$\boxed{V_{DS} = 10.07V}$$

UJT Problem

1) A UJT with $\eta = 0.62$ is used in relaxation oscillator circuit $R = 5k\Omega$ & $C = 0.05\mu f$

i) Determine period & freq. of oscillator

ii) Determine new value of R, changed in order to obtain a frequency of oscillation of 50HZ

iii) if 'C' increased by factor 10, how the value of R changes if freq is 50HZ

Given

$R = 5k\Omega$, $\eta = 0.62$, $C = 0.05\mu f$

i) $T = RC\ln\left[\frac{1}{1-\eta}\right] = (5\times10^3\times0.05\times10^{-6})\ln\left[\frac{1}{1-0.62}\right]$

$\boxed{T = 0.2419 \text{ msec}}$ $f = \frac{1}{T} = 4.134KHZ$

$V_{GG} = V_{GS} + I_D R_S$

$V_{GG} = 0$

$V_{GS} = -I_D R_S = -5 \times 10^{-3} \times 500$

$\boxed{V_{GS} = -2.5V}$

$V_{DD} - I_D(R_D + R_S) - V_{DS} = 0$

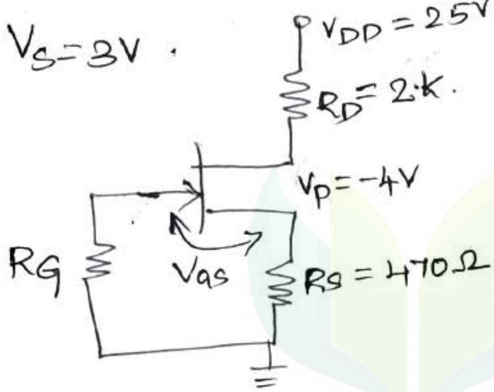
$V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 10 - 5 \times 10^{-3}(1500)$

$\boxed{V_{DS} = 2.5V}$

3) Find I_D, V_{GS}, I_{DSS}, V_D, V_{DS}.

Given. $V_S = 3V$.



$-V_{GS} - I_S R_S = 0$

$-V_{GS} = I_D R_S$

$-V_{GS} = 6.3mA \times 470$

$\boxed{V_{GS} = -3}$

$I_D = \frac{V_{GS}}{R_S} = \frac{3}{370} = 6.3mA$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$I_{DSS} = \frac{I_D}{\left(1 - \frac{V_{GS}}{V_P}\right)^2} = \frac{6.3 \times 10^{-3}}{\left(1 - \frac{-3}{-4}\right)^2}$

$\boxed{I_{DSS} = 102.08mA}$

$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$

$V_{DS} = 25 - 6.38 \times 10^{-3}(2 \times 10^3 + 470)$

$\boxed{V_{DS} = 9.24V}$

$V_D = V_{DS} + V_S$

$V_D = 9.24 + 3$

$\boxed{V_D = 12.24V}$

$V_{DS} = V_D - V_S$

4) A JFET amplifier with voltage divider bias ckt has the : $V_p = -2V$, $I_{DSS} = 4mA$, $R_D = 910\Omega$, $R_S = 3k\Omega$, $R_1 = 12M\Omega$, $R_2 = 8.57M\Omega$, $V_{DD} = 24V$. Find I_D. Check whether FET will operate in pinch off region.

$$V_G = \frac{R_2}{R_1+R_2} \cdot V_{DD}$$

$$\Rightarrow \frac{8.57\times10^{6}}{(12+8.57)\times10^{6}} = 10V$$

$$V_{GS} = V_G - I_D R_S.$$

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1-\frac{V_G - I_D R_S}{V_P}\right)^2$$

$$I_D = 4\left(1-\frac{10-I_D\times3}{-2}\right)^2$$

$$I_D = (3.39\,mA)$$

$$V_{GS} = V_G - I_D R_S$$

$$= 10-(3.39\times10^{-3}\times3\times10^{3})$$

$$\boxed{V_{GS} = -0.17V}$$

$$V_{DS} = V_{DD} - I_D(R_D+R_S)$$

$$= 24 - 3.39\times10^{-3}(0.91+3)\times10^{3}$$

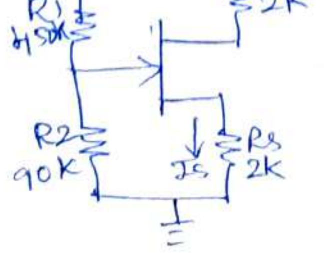
$$\boxed{V_{DS} = 10.745V.}$$

$$V_{DG} = V_{DS} - V_{GS}$$

$$= 10.745+0.17$$

$$\boxed{V_{DG} = 10.915V}$$

5) An N-channel JFET having $V_p = -4V$ & $I_{DSS} = 10mA$, $V_{DD} = 18V$, $R_S = 2K\Omega$, $R_1 = 450K\Omega$, $R_2 = 90K\Omega$, Find I_D & V_{DS}



Verified
M. [illegible] 13/9/19

UNIT-3

AMPLIFIERS.

BJT Small signal Model- Analysis of CE, CB, CC Amplifiers. Gain & frequency Response - MOSFET Small signal model- Analysis of CS & Source follower - Gain & frequency Response.

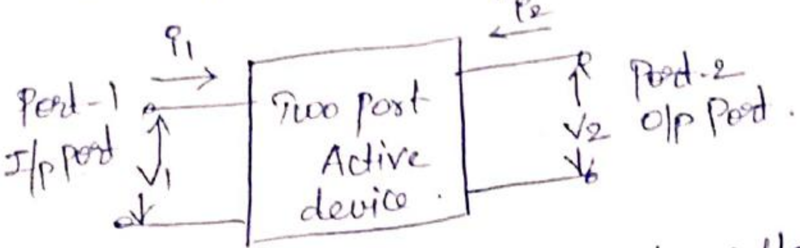
The equivalent circuit for transistor can be drawn using simple approximations by retaining its important features at the same time neglecting its less important features. The equivalent circuits of transistor are derived.

When s/g level is too small, the need for amplification arises to raise the s/g level to desired level. For low i/p s/g the o/p swing of the active devices is also small and the devices are considered to operate in the region.

TWO PORT DEVICES AND HYBRID MODEL :-

→ BJT is two port device which have one terminal is common to both i/p and o/p ports. The behaviour of the two port network is analysed using current and voltage parameters at i/p and o/p ports namely, i/p current, i/p voltage, o/p current and o/p voltage.

→ Consider two port network can be specified by the terminal voltages V_1 and V_2 at port 1 and 2 respecti and current i_1 & i_2 entering port 1 and 2 respectiv



If the i/p current is i_1 and o/p voltage V_2 are take as independent variables the i/p voltage V_1 & current o/p i_2 can be written as,

$$\boxed{\begin{aligned} V_1 &= h_{11} i_1 + h_{12} V_2 \\ i_2 &= h_{21} i_1 + h_{22} V_2 \end{aligned}}$$

The pair hybrid parameter h_{11}, h_{12}, h_{22} & h_{21} are defined,

→ $h_{11} = \left[\frac{V_1}{i_1}\right]$ when $V_2 = 0$.

h_i → i/p impedance with o/p port short circuited.

→ $h_{22} = \left[\frac{i_2}{V_2}\right]$ when $i_1 = 0$.

h_o ⇒ o/p admittance with i/p port open circuited

→ $h_{21} = \left[\frac{i_2}{i_1}\right]$ when $V_2 = 0$.

h_f → Forward current gain with o/p port short circuited

→ $h_{12} \Rightarrow \left[\frac{V_1}{V_2}\right]$ when $i_1 = 0$.

h_r → Reverse voltage Transfer ratio with i/p port open circuited

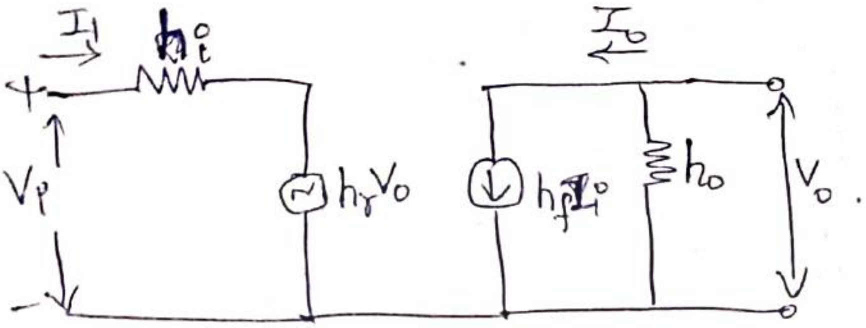
$h_{11} \rightarrow \Omega$

$h_{22} \rightarrow \mho$

$h_{21}, h_{12} \rightarrow$ dimensionless

SMALL SIGNAL AMPLIFIER INTERMS OF HYBRID (H-PARAMETER) MODEL.

→ In order to analyze transistorized amplifier circuit and to calculate its i/p impedance, o/p impedance, current gain and voltage it is necessary to replace transistor circuit with h-parameter equivalent circuit.



The h-parameter equivalent ckt can be drawn with the help of below equations,

$$\boxed{\begin{aligned} V_i &= h_i I_i + h_r V_o \\ I_o &= h_f I_i + h_o V_o \end{aligned}}$$

Benefits of h-parameter:-

i) Real numbers at Audio freq.

ii) Easy to Measure

iii) Can be obtained from transistor static curve.

iv) Convenient to use in circuit analysis and design

v) Most of transistor manufacturing specify the h-parameter.

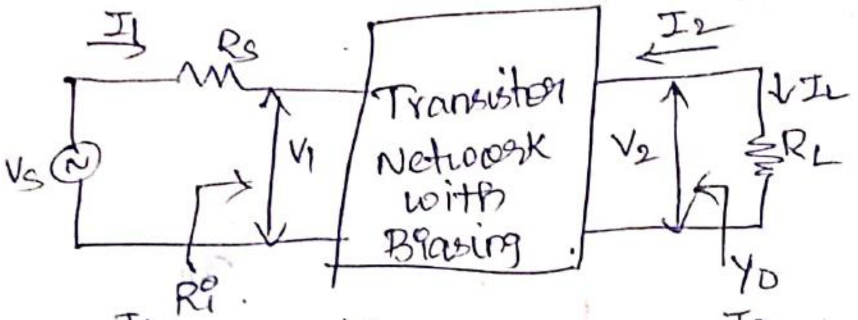
h-parameters for three Configuration:-

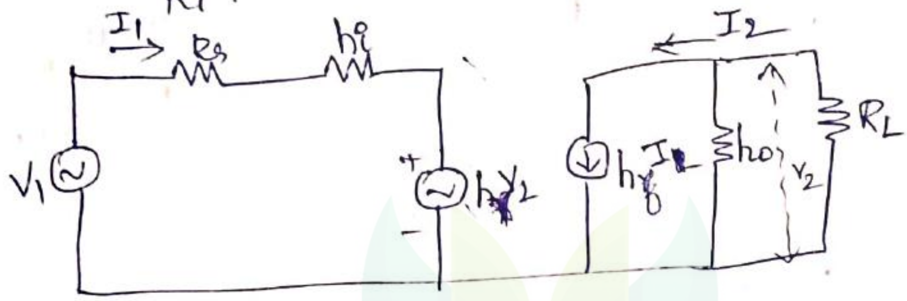
	CB	CE	CC
I/p resistance	h_{ib}	h_{ie}	h_{ic}
Reverse voltage gain	h_{rb}	h_{re}	h_{rc}
Forward transfer current gain	h_{fb}	h_{fe}	h_{fc}
o/p admittance.	h_{ob}	h_{oe}	h_{oc}

→ Small s/g analysis of Transistor can be made for 3 configuration interms of hybrid parameter method.

i) CB-h parameter
ii) CE-h parameter
iii) CC-h parameter

1) Derive the h-parameter of Basic Transistor Amplifier using small s/g Analysis.





i) Current Gain (A_i)

For transistor amplifier A_i defined as ratio of o/p to i/p current.

$$A_i = \frac{I_L}{I_1} = \frac{-I_2}{I_1} \Rightarrow \frac{-i_2}{i_1}$$

We Know that,

$$i_2 = h_f i_1 + h_o V_2 \longrightarrow (1)$$

$$V_2 = -i_2 R_L \longrightarrow (2)$$

Sub 2 in (1)

$$i_2 = h_f i_1 - i_2 R_L h_o$$

$$i_2 + i_2 R_L h_o = h_f i_1$$

$$i_2(1 + R_L h_o) = h_f i_1$$

$$\boxed{A_i = i_2 / i_1 = \frac{-h_f}{1 + R_L h_o}}$$

ii) I/p Resistance (R_i).

It is the i/p resistance looking into the amplifier i/p Terminal. $R_i = \frac{V_1}{I_1}$

The i/p current is i_1,

$$V_1 = h_i i_1 + h_r V_2.$$

Here $$R_i = \frac{h_i i_1 + h_r V_2}{i_1}$$

$$R_i = h_i + \frac{h_r V_2}{i_1} \longrightarrow (1)$$

Sub $V_2 = -i_2 R_L \Rightarrow A_i i_1 R_L \longrightarrow (2)$

Sub (2) in (1)

$$R_i = h_i + \frac{h_r A_i i_1 R_L}{i_1}$$

$$R_i = h_i + h_r A_i R_L.$$

Sub $A_i = \frac{-h_f}{1+h_o R_L}$

$$R_i = h_i - \frac{h_r h_f R_L}{1+h_o R_L}.$$

$\div$ Num & Denom. by R_L.

$$R_i = h_i - \frac{h_r h_f}{1/R_L + h_o}.$$

$\because 1/R_L = Y_L$

$$\boxed{R_i = h_i - \frac{h_r h_f}{Y_L + h_o}}$$

iii) Voltage Gain (A_v).

It is the ratio of o/p voltage V_2 to i/p voltage V_1.

$$A_v = \frac{V_2}{V_1}$$

We know, $\boxed{V_2 = A_i i_1 R_L}$

$$A_v = \frac{A_i i_1 R_L}{V_1} = \frac{A_i R_L}{R_i}$$

iv) O/P Admittance :-

$$Y_o = \frac{i_2}{V_2}$$

We have $i_2 = h_f i_1 + h_o V_2$.

$$\frac{i_2}{V_2} = \frac{h_f i_1 + h_o V_2}{V_2} \Rightarrow \frac{h_f i_1}{V_2} + h_o \quad \text{—— (1)}$$

Applying KVL in i/p Loop.

$$R_s i_1 + h_i i_1 + h_r V_2 = 0.$$

$$(R_s + h_i) i_1 = -h_r V_2.$$

$$\frac{i_1}{V_2} = \frac{-h_r}{R_s + h_i} \quad \text{—— (2)}$$

∴ Sub (2) in (1)

$$\boxed{Y_o = \frac{i_2}{V_2} \Rightarrow h_o - \frac{h_f h_r}{R_s + h_i}}$$

the ... h parameters of ...

$$V_1 = h_{11} i_1 + h_{12} V_2$$
$$i_2 = h_{21} i_1 + h_{22} V_2.$$

$h_{11} = \left[\frac{V_1}{i_1}\right]_{V_2 = 0}$ (i/p impedance)

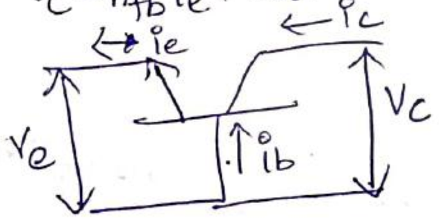
$h_{22} = \left[\frac{i_2}{V_2}\right]_{i_1 = 0}$ (o/p admitance)

$h_{12} = \left[\frac{V_1}{V_2}\right]_{i_1 = 0}$. (Reverse voltage gain)

$h_{21} = \left[\frac{i_2}{i_1}\right]_{V_2 = 0}$ (Forward current gain)

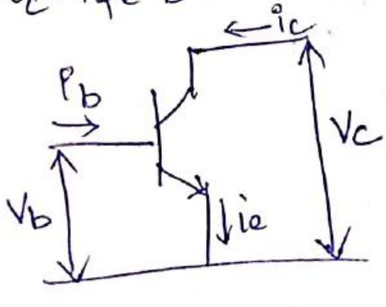
1) CB configuration.

$$V_e = h_{ib} i_e + h_{rb} V_c$$
$$i_c = h_{fb} i_e + h_{ob} V_c.$$



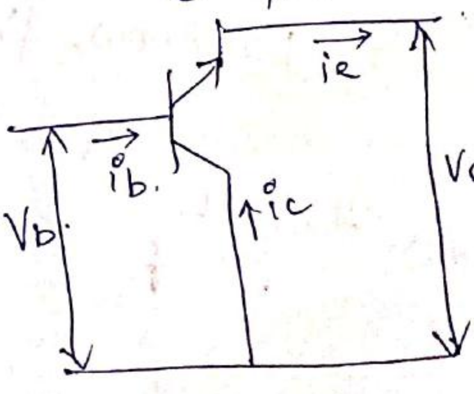
2) CE configuration

$$V_b = h_{ie} i_b + h_{re} V_c$$
$$i_c = h_{fe} i_b + h_{oe} V_c$$

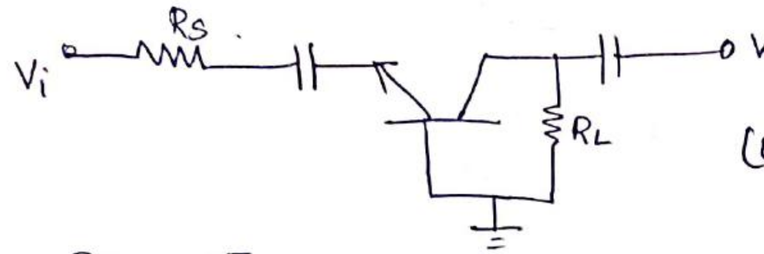


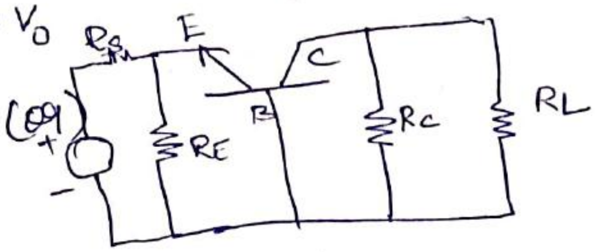
3) CC configuration.

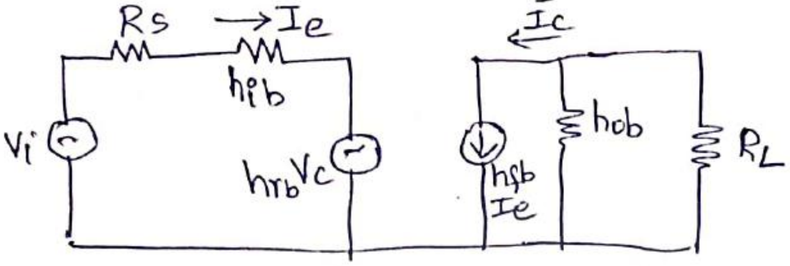
$$V_b = h_{ic} i_b + h_{rc} V_e$$
$$i_e = h_{fc} i_b + h_{oc} V_e.$$



the expression for A_i, A_v, R_i and R_o for CB amplifier using h parameter Model.







i) Current gain:- (A_i)

$$A_i = \frac{-i_2}{i_1} = \frac{-i_c}{i_e}$$

We know,

$$i_c = h_{fb} i_e + h_{ob} V_e \quad \text{--- (1)}$$

$$\boxed{V_c = -i_c R_L} \quad \text{--- (2)}$$

Sub (2) in (1)

$$i_c = h_{fb} i_e - i_c R_L h_{ob}$$

$$i_c(1 + R_L h_{ob}) = h_{fb} i_e$$

$$\boxed{A_i = \frac{i_c}{i_e} = \frac{-h_{fb}}{1 + R_L h_{ob}}}$$

$V_i = h_i i_1 + h_r V_o$

$i_2 = h_f i_1 + h_o V_o$

$V_e = h_{ib} i_e + h_{rb} V_c$

$i_c = h_{fb} i_e + h_{ob} V_e$

$h_{ib} \rightarrow$ i/p impedance when CB Terminals are short circuited

$h_{rb} \rightarrow$ Reverse voltage gain when EB is open ckt

$h_{fb} \rightarrow$ Forward current gain when CB is short circuit

$h_{ob} \rightarrow$ o/p admittance when BE is open ckt

ii) I/p Resistance (R_i).

$$R_i = \frac{V_e}{I_e}$$

We know, $V_e = h_{ib} i_e + h_{rb} V_c$

$$R_i = \frac{h_{ib} i_e + h_{rb} V_c}{i_e}$$

$$= h_{ib} + \frac{h_{rb} V_c}{i_e}$$

$V_c = -i_c R_L \Rightarrow A_i i_e R_L$

$$R_i = \frac{h_{ib} i_e + h_{rb} A_i i_e R_L}{i_e}$$

$$\boxed{R_i = h_{ib} + h_{rb} A_i R_L}$$

iii) Voltage gain (A_V)

$$A_V = \frac{V_c}{V_e} = \frac{A_i i_e R_L}{V_e} \Rightarrow \frac{A_i R_L}{R_i}.$$

iv) o/p Admittance (Y_0).

$$Y_0 = \frac{i_c}{V_c} \quad \text{we know } i_c = h_{fb} i_e + h_{ob} V_c$$

$$\frac{i_c}{V_c} = \frac{h_{fb} i_e}{V_c} + h_{ob}.$$

Apply Kirchoff law,

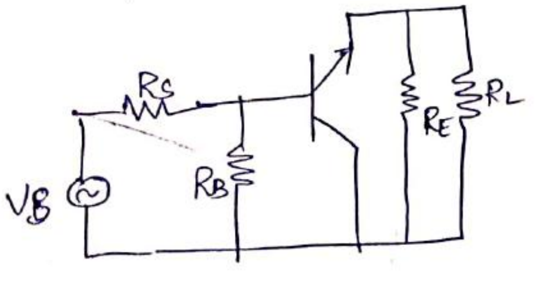
$$R_S i_e + h_{ib} i_e + h_{rb} V_c = 0.$$

$$i_e (R_S + h_{ib}) = -h_{rb} V_c$$

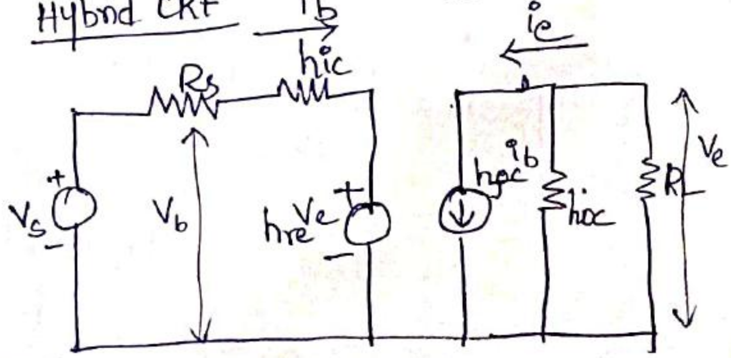
$$\frac{i_e}{V_c} = \frac{-h_{rb}}{R_S + h_{ib}}.$$

$$\boxed{Y_0 = h_{ob} - \frac{h_{rb} h_{fb}}{R_S + h_{ib}}} \qquad \boxed{R_0 = 1/Y_0.}$$

3) Derive the expression for current gain, voltage gain, i/p impedance and o/p impedance for an emitter follower circuit. (CC) configuration (Emitter follower)



Hybrid ckt



$$\boxed{\begin{aligned} V_b &= h_{ic} i_b + h_{rc} V_e \\ i_e &= h_{fc} i_b + h_{oc} V_e. \end{aligned}}$$

$h_{ic} \rightarrow$ i/p impedance when emitter Collector terminal short circuit

$h_{rc} \rightarrow$ Reverse voltage gain when Collector-base Terminal open ckt

$h_{fc} \rightarrow$ forward current gain when CE is short circuit.

$h_{oc} \rightarrow$ o/p admittance when BC is open ckt.

[Cur]rent gain (A_i).

$$A_i = \frac{-i_e}{i_b} \rightarrow (1)$$

$$i_e = h_{fc} i_b + h_{oc} V_e$$

$$V_e = -i_e R_L$$

$$i_e = h_{fc} i_b + h_{oc} (i_e R_L) \rightarrow (2)$$

$$(1 + h_{oc} R_L) i_e = h_{fc} i_b$$

$$\boxed{\frac{i_e}{i_b} = \frac{h_{fc}}{1 + h_{oc} R_L}}$$

ii) **I/P Resistance R_i.**

$$R_i = \frac{V_b}{i_b}$$

From i/p ckt,

$$V_b = h_{ic} i_b + h_{rc} V_e$$

$$\therefore V_e = -i_e R_L = A_i i_b R_L$$

$$R_i = \frac{h_{ic} i_b + h_{rc} A_i i_b R_L}{i_b}$$

$$\boxed{R_i = h_{ic} + h_{rc} A_i R_L}$$

Sub $A_i = \frac{-h_{fc}}{1 + h_{oc} R_L}$

$$\boxed{R_i = h_{ic} - \frac{h_{rc} h_{fc} R_L}{1 + h_{oc} R_L}}$$

iii) **voltage gain A_V :-**

$$A_V = \frac{V_e}{V_b}$$

$$= \frac{A_i i_b R_L}{V_b} \Rightarrow \frac{A_i R_L}{R_i}$$

$$\boxed{A_V = \frac{A_i R_L}{R_i}}$$

iv) **O/P Admittance (Y_o)**

$$Y_o = \frac{i_2}{V_2} = \frac{i_e}{V_e}$$

$$i_e = h_{fc} i_b + h_{oc} V_e$$

$$\frac{i_e}{V_e} = \frac{h_{fc} i_b + h_{oc} V_e}{V_e}$$

$$= \frac{h_{fc} i_b}{V_e} + h_{oc} \rightarrow (1)$$

Apply Kirchoff law,

$$R_s i_b + h_{ic} i_b + h_{rc} V_e = 0$$

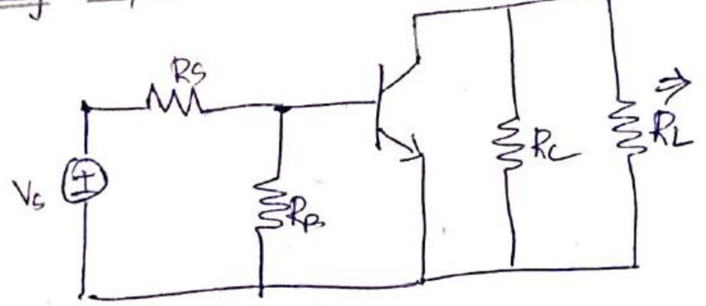
$$(R_s + h_{ic}) i_b = -h_{rc} V_e$$

$$\frac{i_b}{V_e} = \frac{-h_{re}}{R_s + h_{ic}} \rightarrow (2)$$

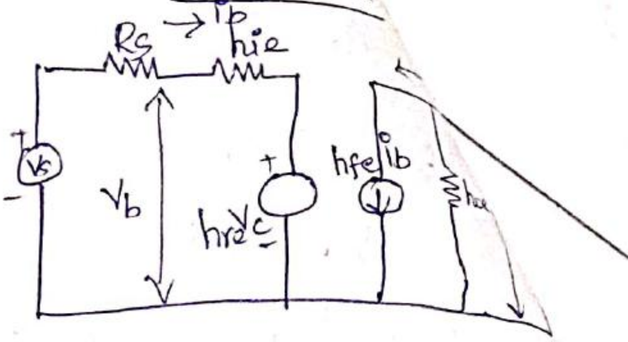
Sub (2) in (1).

$$\boxed{\frac{i_e}{V_e} = h_{oc} - \frac{h_{fc} h_{re}}{h_{ic} + R_s}}$$

4) Derive the expression for A_i, A_v, R_i & R_o for C... using h-parameter model.



H-parameter



The h-parameter equivalent ckt,

$$\boxed{\begin{aligned} V_s &= h_{ie} i_b + h_{re} V_c \\ i_c &= h_{fe} i_b + h_{oe} V_c \end{aligned}}$$

$h_{ie} \rightarrow$ I/p impedance when emitter collector are short circuited

$h_{re} \rightarrow$ Reverse voltage gain when emitter-base terminal are open ckt

$h_{fe} \rightarrow$ Forward current gain when EC terminal short circuit

$h_{oe} \rightarrow$ o/p admittance when EB terminal is open ckt

i) Current gain A_i.

$$A_i = \frac{i_L}{i_b} = -\frac{i_c}{i_b} \longrightarrow (1)$$

$$i_c = h_{fe} i_b + h_{oe} V_c$$

$$i_c = h_{fe} i_b + h_{oe}(-i_c R_L) \longrightarrow (2)$$

$$\boxed{V_c = -i_c R_L}$$

$$\frac{i_c}{i_b} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$\boxed{A_i = \frac{-h_{fe}}{1 + h_{oe} R_L}}$$

ii) Input Resistance (R_i)

$$R_i = \frac{V_b}{i_b} \quad \text{—— (1)}$$

From i/p ckt,

$$V_b = h_{ie} i_b + h_{re} V_c \quad \text{—— (2)}$$

$$V_c = -i_c R_L = A_i i_b R_L$$

$$V_b = h_{ie} i_b + h_{re} A_i i_b R_L \quad \text{—— (3)}$$

sub (3) in (1)

$$R_i = \frac{h_{ie} i_b + h_{re} A_i i_b R_L}{i_b}$$

$$R_i = \frac{i_b(h_{ie} + h_{re} A_i R_L)}{i_b}$$

$$R_i = h_{ie} + h_{re} A_i R_L \longrightarrow (4)$$

Sub $A_i = \frac{-h_{fe}}{1+h_{oe}R_L}$ in (4)

$$\boxed{R_i = h_{ie} - \frac{h_{re} h_{fe} R_L}{1+h_{oe}R_L}}$$

(iii) Voltage gain :- $A_V = \frac{V_c}{V_b}$

$$= \frac{A_i i_b R_L}{V_b}$$

$$\boxed{A_V = \frac{A_i R_L}{R_i}}$$

iv) o/p admittance :-

$$Y_o = \frac{i_c}{V_c}$$

We know,

$$i_c = h_{fe} i_b + h_{oe} V_c$$

$$Y_o = \frac{h_{fe} i_b + h_{oe} V_c}{V_c}$$

$$Y_o = \frac{h_{fe} i_b}{V_c} + h_{oe} \longrightarrow (1)$$

Apply Kirchoff law,

$$R_s i_b + h_{ie} i_b + h_{re} V_c = 0$$

$$i_b (R_s + h_{ie}) = -h_{re} V_c$$

$$\frac{i_b}{V_c} = \frac{-h_{re}}{R_s + h_{ie}} \longrightarrow (2)$$

Sub (2) in (1)

$$\boxed{Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}}$$

common
...-101, hre=

Formulas.

$$A_i = \frac{-h_f}{1+h_o R_L}$$ (Current gain)

$$A_v = \frac{A_i R_L}{R_i}$$ (voltage gain)

$$R_i = h_i - \frac{h_f h_r}{Y_L + h_o} \text{ (or) } h_i + h_r A_i R_L$$ (I/P Impedance)

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}.$$ (O/P Admittance)

Overall voltage gain including Source resistance $A_{VS} = A_V \cdot \left[\frac{R_i}{R_s+R_i}\right]$.

(or) $A_{VS} = A_i \left[\frac{R_L}{R_s+R_i}\right]$

Power Gain $A_p = A_I^2 \frac{R_L}{R_i}$.

Overall Current gain Including Source res $A_{iS} = A_i \left[\frac{R_s}{R_i+R_s}\right]$

Problem-1

1) Consider a Single stage CE amplifier with $R_S = 1K$ & $R_L = 1.2K$ calculate A_I, R_i, A_V, A_{IS}, Power gain & R_o. If $h_{ie} = 1.1K$ $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25\,\mu A/V$

Solution

i) $A_i = \frac{-h_{fe}}{1+h_{oe} R_L} = \frac{-50}{1+(25\times10^{-6}\times1.2\times10^{3})} = -48.54$

ii) $R_i = h_{ie} + h_{re} A_i R_L = 1.1\times10^3 + [2.5\times10^{-4}\times -48.54\times1.2\times10^3] = 1.08\,k\Omega$

iii) $A_V = A_i \frac{R_L}{R_i} = -48.54 \times \left[\frac{1.2\times10^3}{1.08\times10^3}\right] = -53.663$.

iv) $A_{VS} = A_V \left[\frac{R_i}{R_s+R_i}\right] = -53.66 \left[\frac{1.08\times10^3}{1\times10^3+1.08\times10^3}\right] = -27.93$

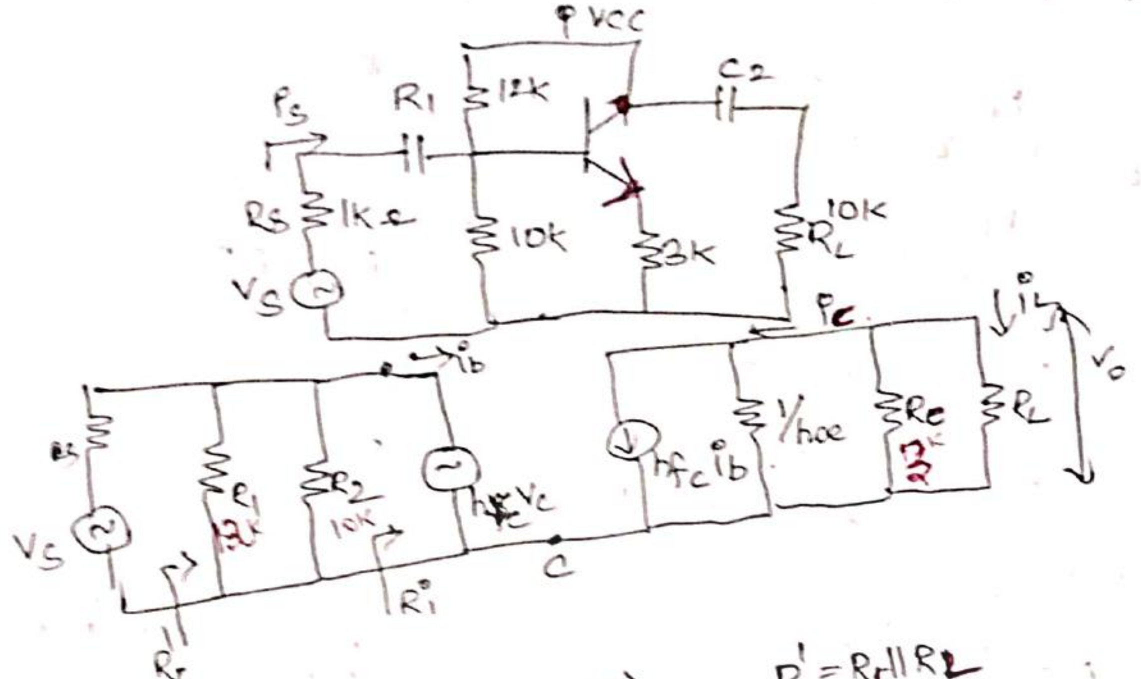
v) $A_{IS} = A_I \left[\frac{R_s}{R_s+R_i}\right] = -48.54 \left[\frac{1\times10^3}{1\times10^3+1.08\times10^3}\right] = -23.28$

vi) $Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie}+R_s} = 25\times10^{-6} \left[\frac{50\times2.5\times10^{-4}}{1.1\times10^3+1\times10^3}\right] = 19.0\,\mu A/V$

vii) $R_o = 1/Y_o = \frac{1}{19\times10^{-6}} = 52.6k$

viii) $A_p = A_i^2 \left[\frac{R_L}{R_i}\right] = (-48.54)^2 \left[\frac{1.2\times10^3}{1.08\times10^3}\right] = 2.62\times10^3$

Common ~~collector~~ emitter, the transistor Parameters are $h_{ie} = 1.2k$, $h_{fe} = -101$, $h_{re} = 1$, $h_{oe} = 25\mu A/V$. Calculate $R_i, A_i, A_{is}, A_v, A_{vs}, R_o$.



$R_L' = R_E \| R_L$

i) $A_i = -\dfrac{i_e}{i_b} = \dfrac{-h_{fe}}{1 + h_{oe} R_L'} = \dfrac{-(-101)}{1 + 25\times10^{-6}(3k\|10k)}$

$= 95.5$

ii) $R_i = h_{ie} + h_{re} A_i \cdot R_L'$

$= 1.2K + 1 \times 91.81 (3k\|10k)$

$\boxed{R_i = 220.85 K\Omega}$

iii) $A_V = \dfrac{A_i R_L'}{R_i}$

$= \dfrac{95.5 \times (3k\|10k)}{220.85k}$

$\boxed{A_v = 0.995}$

iv) $A_{vs} = \dfrac{V_o}{V_S} = \dfrac{V_o}{V_b} \times \dfrac{V_b}{V_S} \Rightarrow A_v \cdot \dfrac{V_b}{V_S}$

$\dfrac{V_b}{V_S} = \dfrac{R_i'}{R_i' + R_S}$ $\qquad R_i' = R_i \| R_1 \| R_2$

$= 220.8k \| 12k \| 10K$

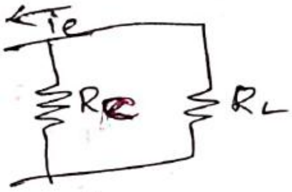
$= 5.32k$

$= \dfrac{5.32K}{5.32k + 1K}$

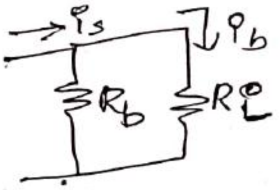
$AV_S = 0.99 \times \dfrac{5.32K}{5.32k + 1K}$

$\boxed{A_{vs} = 0.836}$

v) $A_{is} = \frac{i_L}{i_s} = \frac{i_L}{i_e} \cdot \underbrace{\frac{i_e}{i_b}}_{A_i} \cdot \frac{i_b}{i_s}$.



$\frac{i_L}{i_e} = \frac{-R_e}{R_L+R_e} = \frac{-3k}{3k+10k} = -0.23$



$\frac{i_b}{i_s} = \frac{R_b}{R_b+R_i}$.

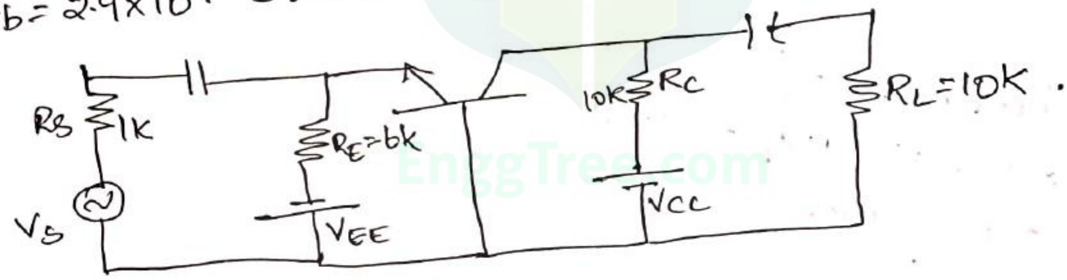
$= \frac{5.45\times10^3}{5.45k+220.8k}$

$= 0.024$.

$A_{IS} = \frac{I_L}{I_S} \Rightarrow (-0.23)\times(-95.5)\times(0.024)$

$\boxed{A_{IS} = 0.527}$ //.

3) For the common base circuit, $h_{ib} = 22\Omega$, $h_{fb} = 0.98$, $h_{ob} = 0.49\mu A$ $h_{rb} = 2.9\times10^{-4}$. Calculate i/p res, o/p res, A_i, A_v.



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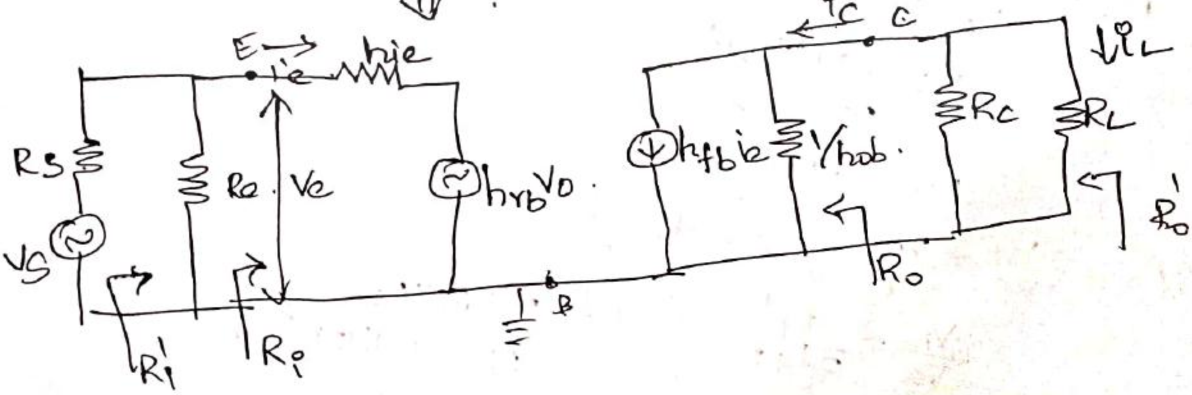
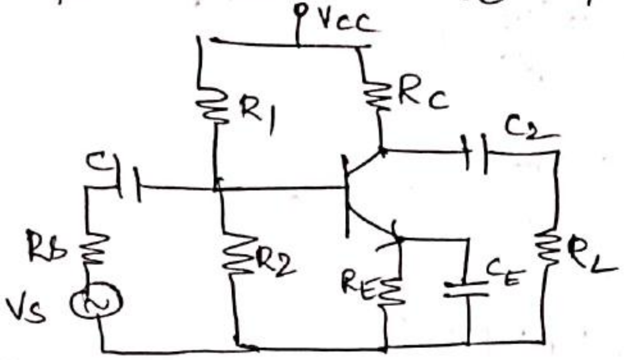
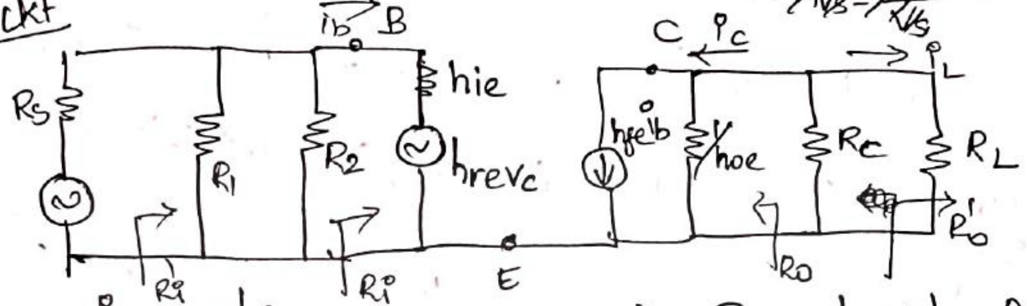


Consider CE amplifier with $R_s = 1K\Omega$, $R_1 = 50K$, $R_2 = 2K$, $R_C = 1K$, $R_L = 1.2K$, $h_{fe} = 50$, $h_{ie} = 1.1K$, $h_{oe} = 25\mu A/V$, $h_{re} = 2.5\times10^{-6}$



Find
1. A_i
2. R_i
3. A_V
4. $A_{Is} = \frac{I_L}{I_s}$
5. $A_{Vs} = \frac{V_o}{V_s}$

Equiv. ckt



i) $A_i = \frac{-i_c}{i_b} = \frac{-h_{fe}}{1+h_{oe}R_L'}$

$R_L' = R_C \| R_L$

$= 1K \| 1.2K \Rightarrow 545.4\Omega$

$A_i = \frac{-50}{1+25\times10^{-6}(545.4)}$

$\boxed{A_i = -49.3}$

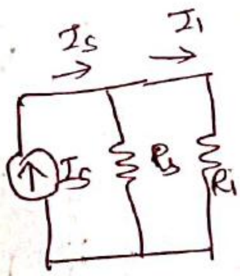
ii) $R_i = h_{ie} + h_{re} A_i \cdot R_L'$

$= 1.1K + 2.5\times10^{-4}\times(-49.32)\times545.45$

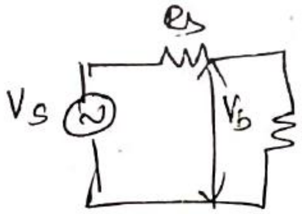
$\boxed{R_i = 1093\Omega}$

iii) $A_V = \frac{V_o}{V_b} = \frac{A_i R_L'}{R_i} = \frac{-49.3\times545.4}{1093}$

$\boxed{A_V = -24.61}$



iv) $A_{Vs} = A_V \frac{V_b}{V_s}$ $\left(\frac{V_o}{V_b}\right)$



$R_i' = R_e \| R_1 \| R_2$

$= 1093 \| 50K \| 2K$

$R_i' = 696.2\Omega$

$V_b = V_s \cdot \frac{R_i'}{R_i' + R_s}$

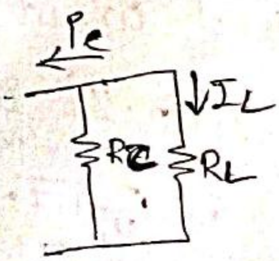
$\frac{V_b}{V_s} = \frac{R_i'}{R_i' + R_S}$

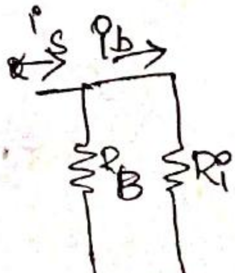
$A_{Vs} = -24.61 \times \frac{696.2}{696+1K}$

$\boxed{A_{Vs} = 10.1}$

v) $A_{Is} = \frac{I_L}{I_s} = \frac{I_L}{I_c}\times\frac{I_c}{I_b}\times\frac{I_b}{I_s}$

$\frac{I_L}{I_c} = \frac{-R_c}{R_c+R_L} = \frac{-2K}{2K+2K} = -0.5$





$$\frac{I_c}{I_b} = h_{fe} = 50.$$

$$\frac{I_b}{I_s} = \frac{R_B}{R_B + R_i} = \frac{20\|10}{(20\|10)+1.1} \qquad R_B = R_1 \| R_2$$

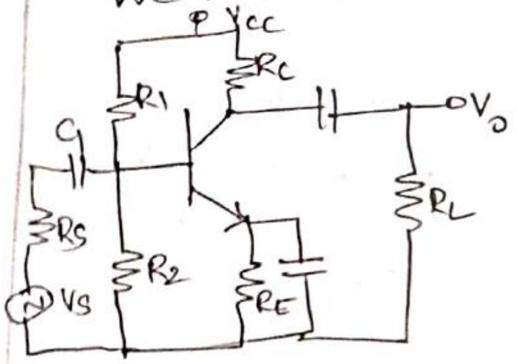
$$= 0.862.$$

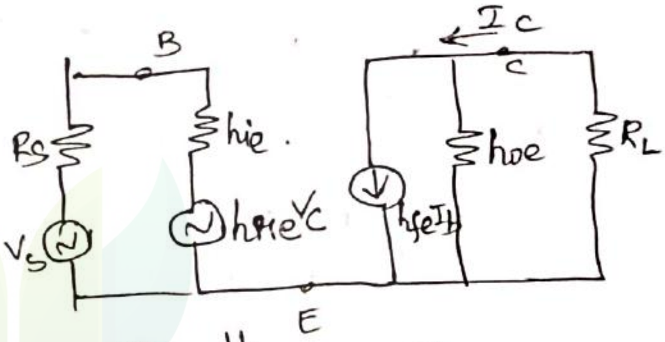
$$\boxed{A_{is} = 0.5 \times 50 \times 0.862 = -21.55}$$

SIMPLIFIED HYBRID MODEL :-

CE $[h_{oe} R_L < 0.1]$ & Neglect h_{oe} & h_{re}.

We know that, Let us consider, CE amplifier.





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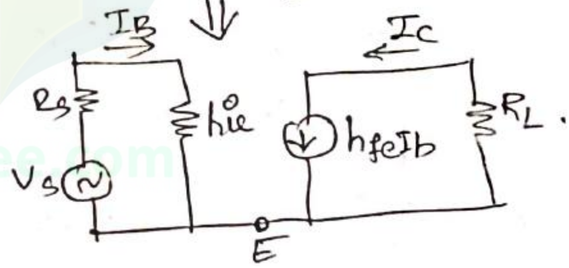


i) Current gain $= \frac{-I_c}{I_b} = \frac{h_{fe} i_b}{i_b}$

$$A_i = -h_{fe}.$$

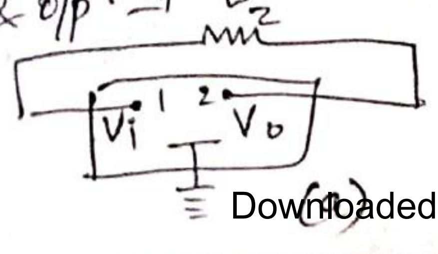
ii) Voltage gain $A_V = \frac{A_i R_L}{h_{ie}}$

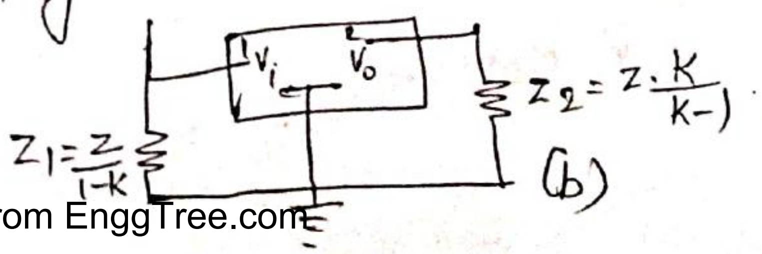
iii) $R_i = h_{ie}$.

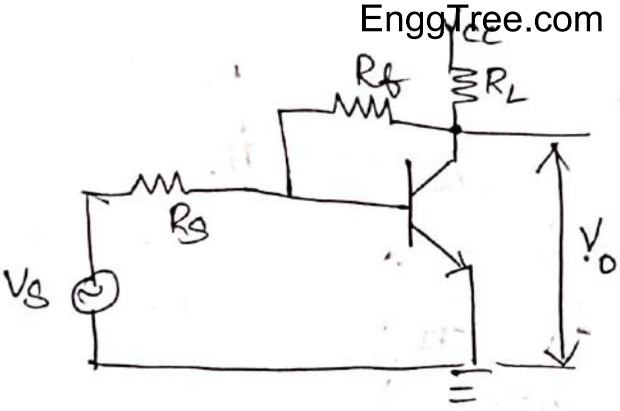
iv) $R_o = \infty$. $Y_o = 0$.

CE amplifier with collector to base bias.

→ The Resistance R_E is connected b/w i/p & o/p. For the analysis of circuit it is necessary to split this resistance for i/p & o/p. It is achieved by Millers theorem.







[Collector to base Bias]

→ Miller theorem is used to convert any circuit from (a) to (b)

→ Z is the impedance connected b/w 2 nodes, node 1 & node 2 it can be seperated as Z_1 & Z_2.

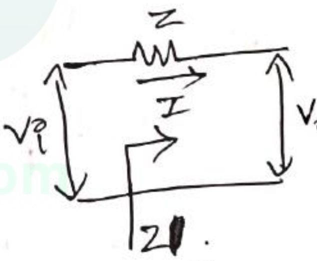
→ Vi and Vo are the voltages.

$$\boxed{\begin{aligned} Z_1 &= \frac{Z}{1-K} \\ Z_2 &= Z \cdot \frac{K}{K-1} \end{aligned}}$$

Proof of Miller Theorem:-

→ Effect of resistance Z on the i/p circuit is ratio of Vi to current I.

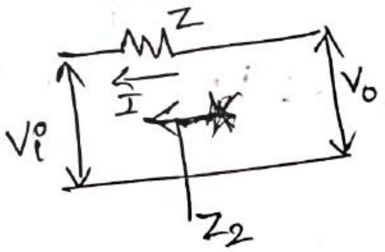
$$\boxed{Z_1 = \frac{V_i}{I}}$$



$$I = \frac{V_i - V_o}{Z} = \frac{V_i\left[1 - \frac{V_o}{V_i}\right]}{Z}$$

$$= \frac{V_i[1 - A_v]}{Z}$$

$$Z_1 = \frac{V_i}{I} = \frac{Z}{1 - A_v} = \frac{Z}{1-K}.$$



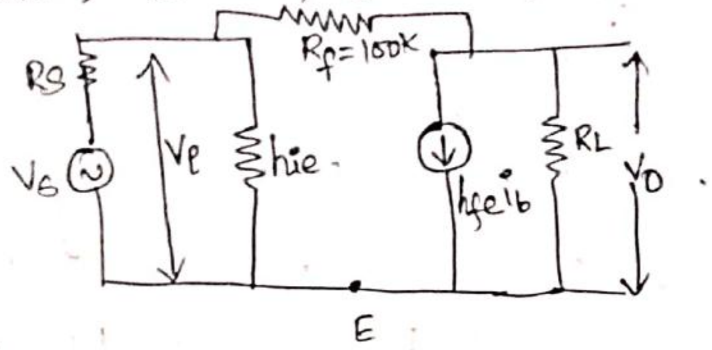
$$Z_2 = \frac{V_o}{I}.$$

$$I = \frac{V_o - V_i}{Z} = \frac{V_o\left[1 - \frac{V_i}{V_o}\right]}{Z} = \frac{V_o\left[1 - \frac{1}{A_v}\right]}{Z}$$

$$= \frac{V_o\left[\frac{A_v - 1}{A_v}\right]}{Z}$$

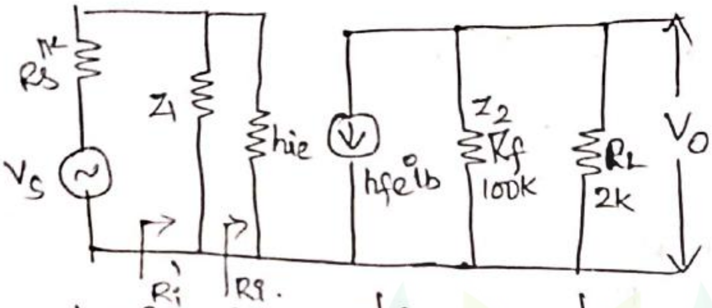
$$Z_2 = \frac{V_o}{I} = \frac{Z}{\frac{A_v - 1}{A_v}} = \frac{Z \cdot A_v}{A_v - 1} = \frac{Z \cdot K}{K-1}$$

4) For the Common Emitter Ampr with collector to base bias has $R_f = 100K\Omega$, $R_L = 2K\Omega$, $R_S = 1K\Omega$, $h_{ie} = 1.1K$, $h_{fe} = 50$, $h_{oe} = h_{re} = 0$



$\boxed{Z_2 = Z}$

Soln.



i) Current gain $A_i = \frac{-h_{fe}}{1+h_{oe}R_L} \Rightarrow \frac{-h_{fe}}{1+0} \Rightarrow -50$.

ii) I/p Resistant $R_i = h_{ie} = 1.1k\Omega$

iii) voltage gain $A_v = \frac{A_i R_L'}{R_i} = \frac{50 \times 1.96 \times 10^3}{1.1 \times 10^3}$

$R_L' = R_f \parallel R_L$
$= 100k \parallel 2k$
$= 1.96 \times 10^3$

$\boxed{A_v = -89.09}$

iv) Overall i/p resistance:-

$R_i' = Z_1 \parallel R_i = 1110 \parallel 1110$

$\boxed{R_i' = 1009\,\Omega}$.

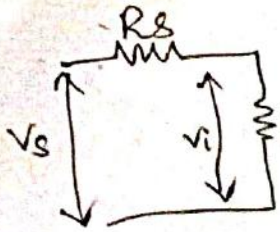
$Z_1 = \frac{Z}{1-A_v} = \frac{100K}{1+89.09}$

$Z_1 = 1110\,\Omega$

v) Overall voltage gain:-

$A_{vs} = \frac{V_o}{V_s} = \frac{V_o}{V_i} \cdot \frac{V_i}{V_s}$.

$\Rightarrow A_v \cdot \frac{V_i}{V_s}$.



$V_i = V_s \cdot \frac{R_i'}{R_i' + R_s}$.

$\frac{V_i}{V_s} = \frac{1009}{1009+1000} = 0.50$

$\boxed{A_{vs} = 89.09\,(0.50) = -44.55}$

FREQUENCY RESPONSE OF TRANSISTOR AMPLIFIER :-

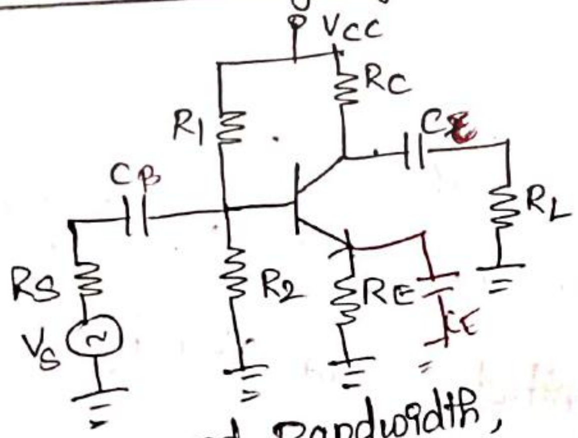
→ An ideal Ampr provides some amplification for all frequencies. The degree of amplification is indicated by the frequency response curve.

→ The frequency response curve is plotted b/w voltage gain and frequency, To plot this curve,

> * I/p Voltage should be constant.
> * Frequency of i/p should be varied.
> * O/p voltage at each frequency of i/p signal is noted.
> * Gain of ampr is calculated.

Frequency region		Frequency Response
i) Mid frequency region	–	Ideal.
ii) High & Low frequency region	–	Deviates from ideal characteristics region.

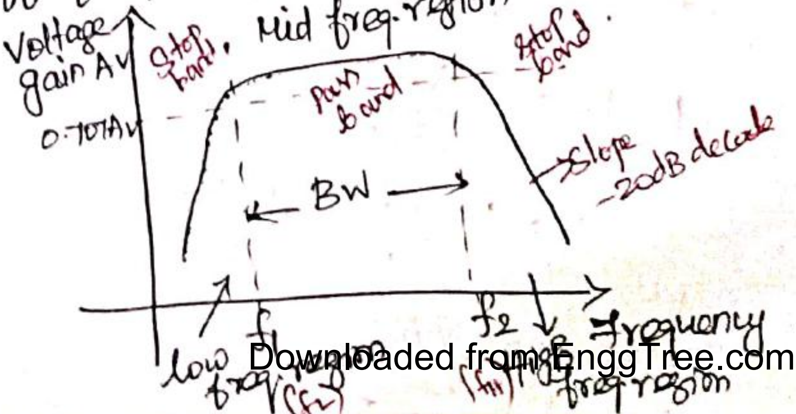
→ The decrease in voltage gain with frequency is called roll off.



RC Coupled CE Ampr.

C_B → Blocking cap.
CC → Coupling cap.
CE → Bypass cap.

Cutoff frequency and Bandwidth,



Power gain = Voltage Gain × Current

There are 3 regions namely,

* Low frequency region → Coupling, bypass ⇒ Lower Gain
* High frequency region → stray cap lower Gain.
* Mid frequency region

We know

Cascading Amp limit the Gain at high & low freq.

Bandwidth is defined as difference b/w f_2 & f_1:

$$\boxed{BW = f_2 - f_1}$$

f_2 & f_1 → half power frequencies since gain drops to 70.7% of Maximum value.

Frequency response can be analysed in,

→ Low frequency response

→ High frequency response.

LOW FREQUENCY RESPONSE :-

At high freq, $X_C = \frac{1}{2\pi fc} = 0\Omega$.

At Low freq $X_C = \frac{1}{2\pi fc} = \infty\ \Omega$

Apply voltage divider rule, $V_0 = R.\frac{V_{in}}{R - jX_C}$ —— (1)

Magnitude of Vout given by,

$|V_0| = R.\frac{V_{in}}{\sqrt{R^2 + X_C^2}}$ when $X_C = R$ —— (2)

$|V_0| = R.\frac{V_{in}}{\sqrt{R^2 + R^2}}$

$\Rightarrow R.\frac{V_{in}}{\sqrt{2R^2}} = \frac{R.V_{in}}{\sqrt{2}.R}$

$$\boxed{|V_{out}| = \frac{V_{in}}{\ }}$$

We know that Gain $|A_V| = \frac{|V_{out}|}{|V_{in}|} = \frac{\frac{1}{\sqrt{2}} V_{in}}{V_{in}}$

$= \frac{1}{\sqrt{2}} = 0.707$

$\boxed{|A_V| = 0.707.}$ at $X_C = R$.

As per our assumption, $X_C = R$.

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f_1 C} = R.$$

$$\boxed{f_1 = \frac{1}{2\pi RC}}$$

From eq (1).

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R}{R - jX_C} = \frac{R}{R\left(1 - \frac{jX_C}{R}\right)}$$

$$A_V = \frac{1}{1 - j\left(\frac{X_C}{R}\right)} = \frac{1}{1 - j\left[\frac{1}{2\pi f RC}\right]}$$

$$= \frac{1}{1 - j\left[\frac{1}{2\pi RCf}\right]}.$$

$\therefore f_1 = \frac{1}{2\pi RC}$.

$$\boxed{A_V = \frac{1}{1 - j(f_1/f)}}$$

where $f = f_1$.

$$A_V = \frac{1}{\sqrt{1+1}} = \frac{1}{\sqrt{2}} = 0.707.$$

Av can be written in Magnitude & phase.

$$A_V = \frac{V_{out}}{V_{in}} = \frac{\tan^{-1}(f_1/f)}{\sqrt{1 + (f_1/f)^2}}$$

Taking log of Av,

$$A_V = 20\log_{10} \frac{1}{\sqrt{1 + (f_1/f)^2}}$$

$$= 20\log_{10}\left(\sqrt{1 + (f_1/f)^2}\right)^{-1}$$

$$= 20\log_{10}\left[1 + (f_1/f)^2\right]^{-1/2}.$$

$$= -20/2 \log_{10}\left[1 + (f_1/f)^2\right]$$

$$= -10\log_{10}\left(1+\left(\frac{f_1}{f}\right)^2\right)$$

i) $f_1 >> f$

$$|A_V| = -20\log_{10}\left(\frac{f_1}{f}\right)$$

ii) $f = f_1$

$$\therefore f_1 = f = 1$$

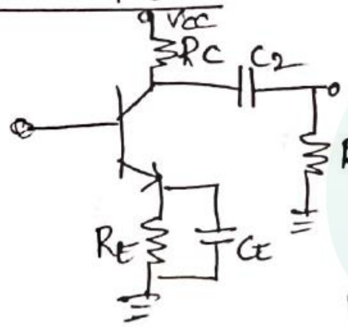
$$|A_V| = -20\log_{10}(1) = 0\,dB$$

iii) when $f = f_1/2$

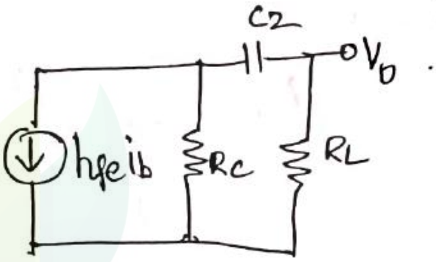
$$|A_V| = -20\log_{10}(2) = -6\,dB$$

OUTPUT RC N/w:-

case(i)

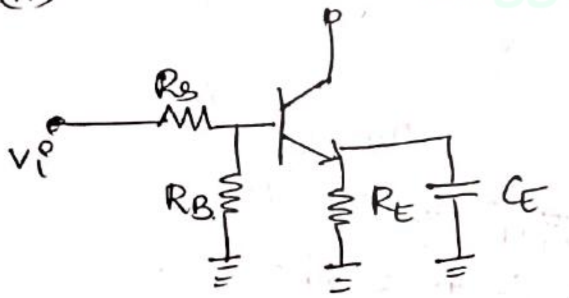


$\Rightarrow$

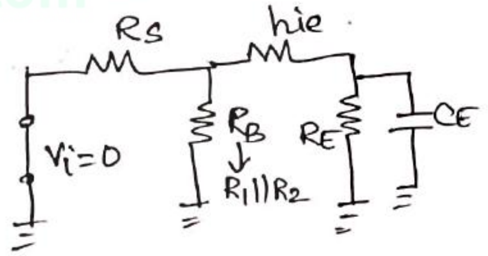


$$\boxed{f_c = \frac{1}{2\pi(R_C+R_L)C_1}}$$

case(ii)



$\Rightarrow$



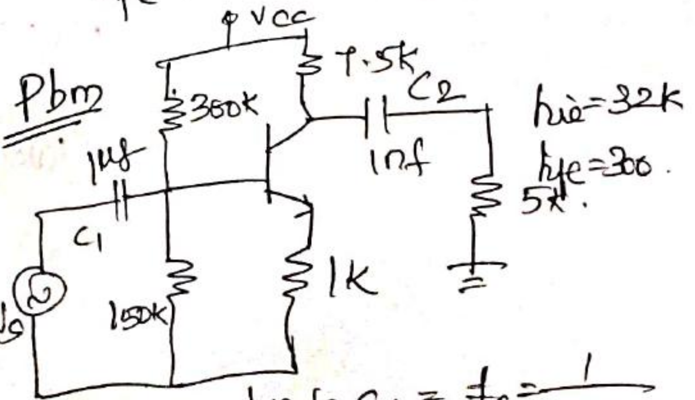
$$R_r = \frac{(R_S \| R_B) + h_{ie}}{h_{fe}}$$

Bypass N/w

Formula

$$\boxed{f = \frac{1}{2\pi\left[\left(\frac{R_{Th}+h_{ie}}{\beta}\right) \| R_E\right] C_E}}$$

Pbm



$h_{ie} = 3.2K$

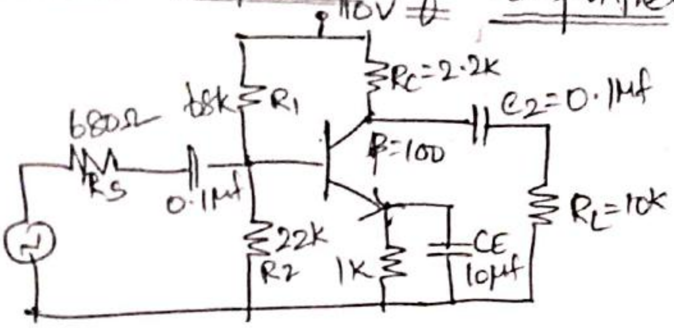
$h_{fe} = 300$

i) Cutoff freq f_c due to $C_1 = f_c = \frac{1}{2\pi R_{in} C_1}$

$R_{in} = R_1 \| R_2 \| h_{ie}$

ii) due to $C_2 - f_c = \frac{1}{2\pi(R_C+R_L)C_2}$

...ermine the freq. resp. of amplifier ckt.



$h_{ie} = 1.1K$

(i) I/P RC N/w

$$f_c = \frac{1}{2\pi[R_S + (R_1 \| R_2 \| h_{ie})]C_1}$$

$$= \frac{1}{2\pi[680 + (68k \| 22k \| 1.1k)] \times 0.1 \times 10^{-6}}$$

$$= 929.8\,Hz \; [i/P]$$

ii) O/P RC N/w

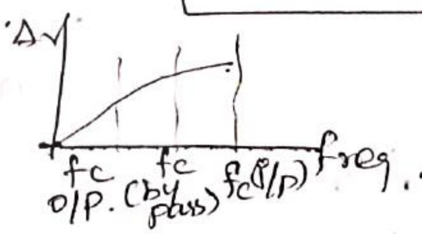
$$f_c = \frac{1}{2\pi(R_C + R_L)C_2} = \frac{1}{2\pi(2.2k + 10k) \times 0.1 \times 10^{-6}} = 130.45\,Hz \; [o/P]$$

iii) Bypass N/w

$$f_c = \frac{1}{2\pi\left[\left(\frac{R_{Th} + h_{ie}}{\beta}\right) \| R_E\right] C_E} = \frac{1}{2\pi\left(\frac{653.2 + 1100}{100}\right) \| 1k \times 10 \times 10^{-6}}$$

$R_{Th} = R_1 \| R_2 \| R_S$
$= 68k \| 22k \| 680$
$= 653.28\,\Omega$

$\Rightarrow 923.7\,Hz \; [By\ pass]$



HIGH FREQUENCY RESPONSE:-

Parasitic Capacitance → C_{be}, C_{bc}, C_{ce}

wiring capacitance → C_{wi}, C_{wo}

Miller capacitance → C_{mi}, C_{mo}.

$$\boxed{\begin{array}{l} \text{I/p capacitance } C_P = C_{wi} + C_{be} + C_{mi} \\ \text{O/p capacitance } C_o = C_{wo} + C_{ce} + C_{mo} \end{array}}$$ → (1) → (2)

By Millers Theorem,

$$\boxed{C_{mi} = (1 - A_V)C_{bc}} \rightarrow (3)$$

Sub (3) in (1).

$$\boxed{C_i = C_{wi} + C_{be} + (1 - A_V)C_{bc}}$$

Sub (3) in (2)

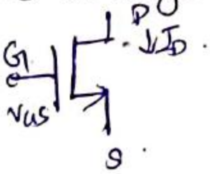
$$C_o = C_{wo} + C_{ce} + (1 - A_V)C_{bc}.$$

Here $1 >> A_V$.

$$\boxed{C_o = C_{wo} + C_{ce} + C_{bc}}.$$

MOSFET SMALL SIGNAL ANALYSIS.

The instantaneous gate to source voltage is given by



$$V_{GS} = V_{GSQ} + V_i.$$

$$V_i = V_{gs}.$$

$$\boxed{V_{GS} = V_{GSQ} + V_{gs}} \rightarrow (1)$$

$V_{GSQ} \rightarrow$ DC component | $V_{gs} \rightarrow$ A C component

The instantaneous drain current is,

$$\boxed{i_D = k(V_{GS} - V_T)^2} \rightarrow (2).$$

Sub (1) in (2).

$$i_D = k\left[V_{GSQ} + V_{gs} - V_T\right]^2 = k\left[(V_{GSQ} - V_T) + V_{gs}\right]^2.$$

$$\boxed{i_D = \underbrace{k\left[(V_{GSQ} - V_T)^2\right]}_{\text{DC component}} + \underbrace{2k\left[V_{GSQ} - V_T\right]V_{gs}}_{\text{Time varying } I_D \text{ component}} + \underbrace{kV_{gs}^2}_{\text{Produce Harmonic}}} \rightarrow (3)$$

i) The 1st term $\Rightarrow$ Quiescent drain current / DC drain current

ii) The 2nd term $\Rightarrow$ Time varying drain current

iii) The 3rd term $\Rightarrow$ Proportional to square of signal voltage.

$\rightarrow$ For sinusoidal i/p signal the squared term produces undesirable harmonics in o/p voltage.

TO MINIMIZE THE HARMONICS.

$V_{gs} << 2(V_{GSQ} - V_T)$. Neglect V_{gs}^2 in (3).

$$\boxed{i_D = I_{DQ} + i_d.} \rightarrow (4).$$

where, $\left\{ \begin{array}{l} I_{DQ} = k(V_{GSQ} - V_T)^2 \\ i_d = 2k(V_{GSQ} - V_T)V_{gs} \end{array} \right\}$

The small s/g drain transconductance is,

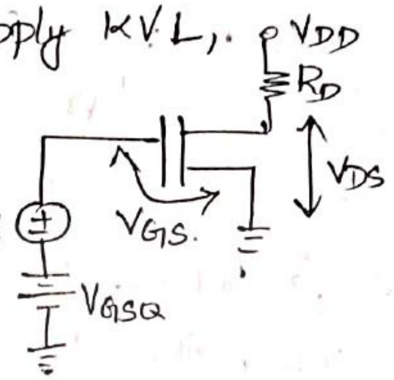
$$g_m = \frac{i_d}{V_{gs}} = \frac{2K(V_{GSQ} - V_T)V_{gs}}{V_{gs}}.$$

$$\boxed{g_m = 2K\left[V_{GSQ} - V_T\right]}$$

MOSFET SMALL SIGNAL MODEL:-

From the diagram apply KVL,

o/p voltage is,



$V_{DS} = V_o = V_{DD} - i_D R_D$.

Sub $\boxed{i_D = I_{DQ} + i_d}$ from (4)

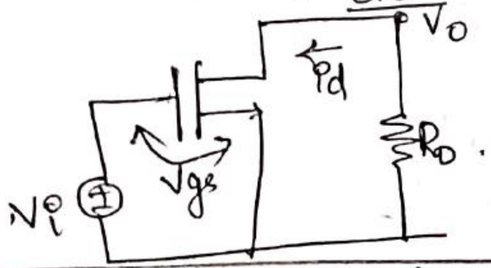
$$\boxed{V_{DS} = V_{DD} - I_{DQ}R_D - i_d R_D}$$

* The o/p voltage is combination of AC & DC values.
* The time varying o/p s/g is time varying drain to source voltage.

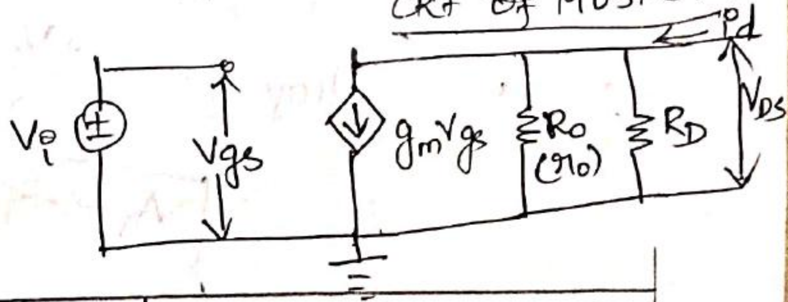
$$V_o = V_{ds} = -i_d R_D.$$

$$\boxed{V_{ds} = -g_m V_{gs} R_D} \quad \left[\because i_d = g_m V_{gs}\right]$$

AC equivalent ckt



small s/g equivalent ckt of MOSFET.

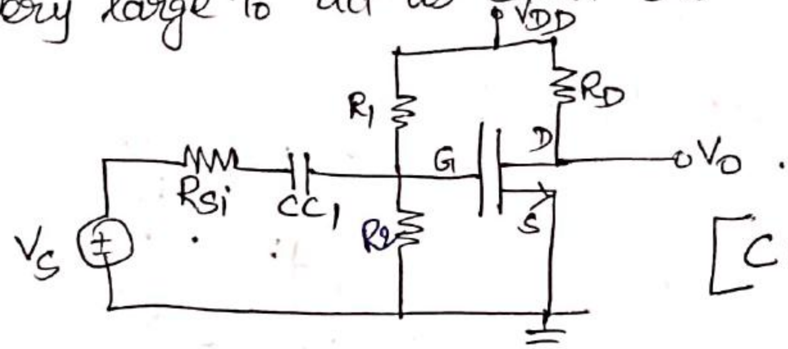


i) The relation b/w I_d & V_{gs} includes.
ii) current source $g_m V_{gs}$ connected from Drain to source
iii) The i/p impedence is open ckt & $I_g = 0$.

Analysis of Common Source Amplifier

→ The common source ckt with voltage divider is given below,

→ Assume that the s/g frequency of Coupling Capacitors are very large to act as Short ckt.



[CS circuit with voltage divider bias]

→ The s/g source is represented by Thevinin's equivalent circuit in which the s/g voltage source Vs is series with equivalent source resistance Rsi

Small s/g Equivalent ckt.

The Gain is Calculated by,

i) $A_V \Rightarrow$ Voltage gain $= \frac{+V_o}{V_i} = \frac{-g_m V_{gs}[R_o \| R_D]}{V_{gs}}$ $\quad [V_i = V_{gs}]$

$$\boxed{A_V = -g_m [R_o \| R_D]}$$

ii) Overall voltage gain,

$$A_{VS} = \frac{V_o}{V_s} \times \cancel{\ } = \frac{V_o}{V_i} \times \frac{V_i}{V_s}$$

$$= \frac{-g_m[R_o \| R_D] \cdot [R_i] \cancel{V_{gs}}}{\cancel{V_{gs}} \cdot [R_i + R_{si}]}$$

$\because V_i = V_{gs}$

$$V_i = V_s \cdot \frac{R_i}{R_i + R_{si}}$$

$$\frac{V_s}{V_i} = \frac{R_i + R_{si}}{R_i}$$

$$= -g_m (R_o \| R_D) \left[\frac{R_i}{R_i + R_{si}}\right] \Rightarrow A_V \left[\frac{R_i}{R_i + R_{si}}\right]$$

I/P Resistance $R_{is} = R_1 || R_2$

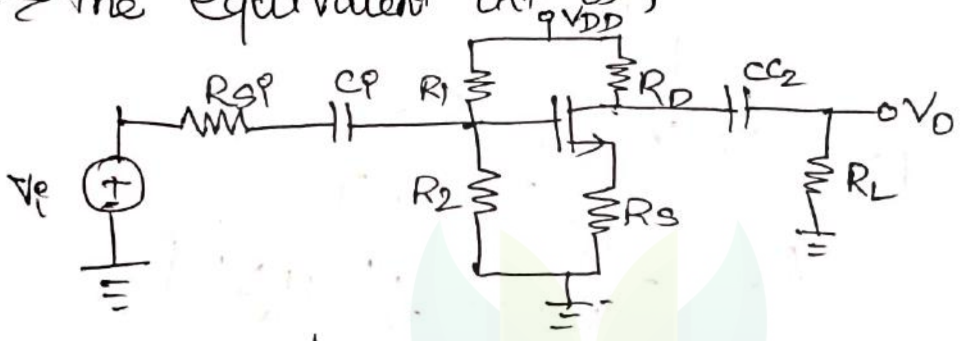
O/P Resistance $R_o = R_D || R_o$.

Ac drain to source voltage $V_{gs} = -I_D R_D$.

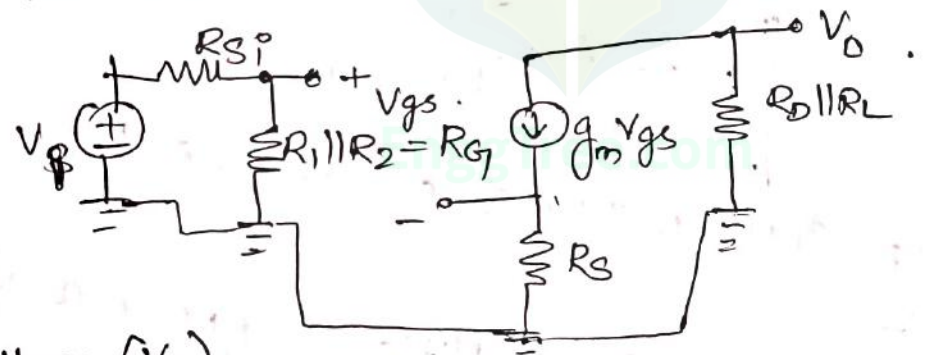
COMMON SOURCE AMPLIFIER WITH SOURCE RESISTANCE.

→ The common source resistance is introduced to stabilize the Q-point against variations in MOSFET parameters. The source resistor reduces signal gain.

→ The equivalent ckt is,



Equivalent ckt:-



i) o/p voltage (V_o)

$$V_o = -g_m V_{gs} [R_D || R_L] \longrightarrow (1)$$

ii) Gate to Source voltage (V_{gs}),

Apply KVL to i/p around Gate to source loop.

$$V_i = V_{gs} + g_m V_{gs} \cdot R_s \longrightarrow (2).$$

$$V_i = V_{gs} [1 + g_m R_s]$$

$$\boxed{V_{gs} = \frac{V_i}{1 + g_m R_s}} \longrightarrow (3)$$

iii) Voltage gain $A_V = \dfrac{V_o}{V_i} = \dfrac{-g_m \cancel{V_{gs}} [R_D || R_L]}{\cancel{V_{gs}} [1 + g_m R_s]} = \dfrac{-g_m [R_D || R_L]}{1 + g_m R_s}$

iv) Overall voltage gain A_{VS}.

$$A_{VS} = \frac{V_o}{V_S} \longrightarrow (5).$$

$$V_i = V_S \cdot \left[\frac{R_G}{R_{Si}+R_G}\right]$$

$$\therefore V_S = \frac{V_i\left[R_{Si}+R_G\right]}{R_G} \rightarrow (6)$$

$$\boxed{R_G = R_1 \| R_2}$$

Sub (1) & (6) in (5)

$$\therefore A_{VS} = \frac{-g_m V_{gs}\left[R_D \| R_L\right]}{\left[\frac{R_{Si}+R_G}{R_G}\right] \cdot V_i}$$

From (3) $V_i = V_{gs}\left[1+g_m R_S\right]$

$$A_{VS} = \frac{-g_m \cancel{V_{gs}}\left[R_D \| R_L\right]}{\left[\frac{R_{Si}+R_G}{R_G}\right] \cdot \cancel{V_{gs}}\left[1+g_m R_S\right]}$$

$$\boxed{A_{VS} = A_V \cdot \left[\frac{R_G}{R_{Si}+R_G}\right]}$$

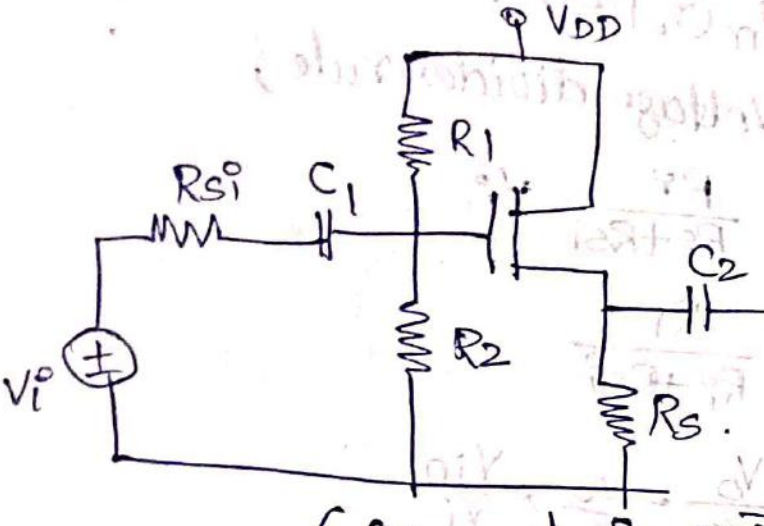
ANALYSIS OF COMMON DRAIN OR SOURCE FOLLOWER AMPLIFIER:-

→ The Common drain amplifier is known as grounded drain amplifier.

→ The I/P signal is Coupled through C_{C1} to the MOSFET gate & O/P S/g at the MOSFET source is Coupled to C_{C2} to Load Resistance R_L.

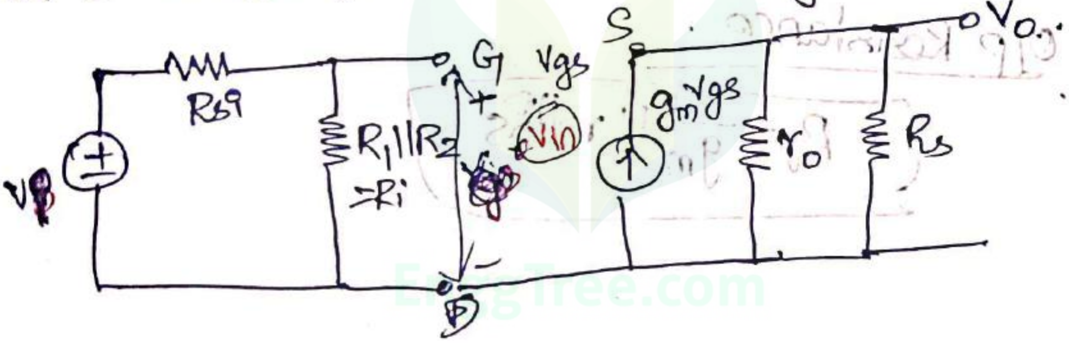
→ The R_L is Connected in series to source terminal of MOSFET.

FET Source-follower Amplifier :- [Common drain]



(Common drain ampr)

The above shows source follower (common drain) Here o/p is taken from the source with respect to ground & drain is connected directly to VDD



I/p Resistance (Ri)

$$R_i = R_1 || R_2$$

Voltage gain (Av)

$$V_o = g_m V_{gs} (r_o || R_s) \longrightarrow (1)$$

$$A_V = \frac{V_o}{V_i} = \frac{V_o}{V_{in}} \times \frac{V_{in}}{V_i}$$

Apply KVL o/p loop.

$$V_{in} = V_{gs} + V_o \longrightarrow (2)$$

$$V_{in} = V_{gs} + g_m V_{gs} (r_o || R_s)$$

$$V_{gs} = \frac{V_{in}}{1 + g_m (r_o || R_s)} \text{---} (3)$$

$$\frac{V_o}{V_{in}} = \frac{g_m(r_o \| R_s)}{1+g_m(r_o \| R_s)}$$

Using voltage divider rule,

$$V_{in} = \frac{R_i}{R_i + R_{si}} V_i$$

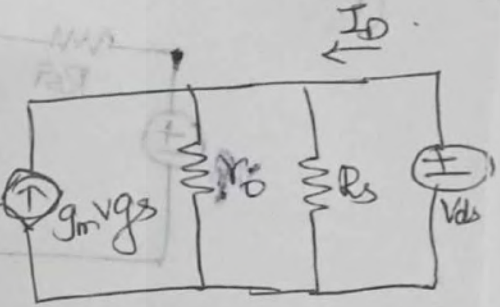
$$\frac{V_{in}}{V_i} = \frac{R_i}{R_i + R_{si}}$$

$$A_V = \frac{V_o}{V_i} = \frac{V_o}{V_{in}} \times \frac{V_{in}}{V_i}$$

$$= \frac{g_m(r_o \| R_s)}{1+g_m(r_o \| R_s)} \cdot \frac{R_i}{R_i + R_{si}} \longrightarrow (4)$$

O/P Resistance.

$$\boxed{R_o = \frac{1}{g_m} \| r_o \| R_s}$$



Proof

$$I_D + g_m v_{gs} = \frac{V_{ds}}{r_o} + \frac{V_{ds}}{R_s} \longrightarrow (5)$$

from eq (2) $\Rightarrow$ $V_{in} = V_{gs} + V_o$

Put $V_{in} = 0$

$$V_{gs} = -V_{ds} \longrightarrow (6)$$

Sub (6) in eq (5).

$$I_D - g_m V_{ds} = \frac{V_{ds}}{r_o} + \frac{V_{ds}}{R_s}$$

$$I_S = V_{ds}\left[\frac{1}{r_o} + \frac{1}{R_s} + \frac{1}{(1/g_m)}\right]$$

$$R_o = \frac{V_{ds}}{I_S} \Rightarrow \left[\frac{1}{(1/r_o) + (1/R_S) + (g_m)}\right]$$

$$\boxed{R_o = r_o \| R_s \| \frac{1}{g_m}}$$

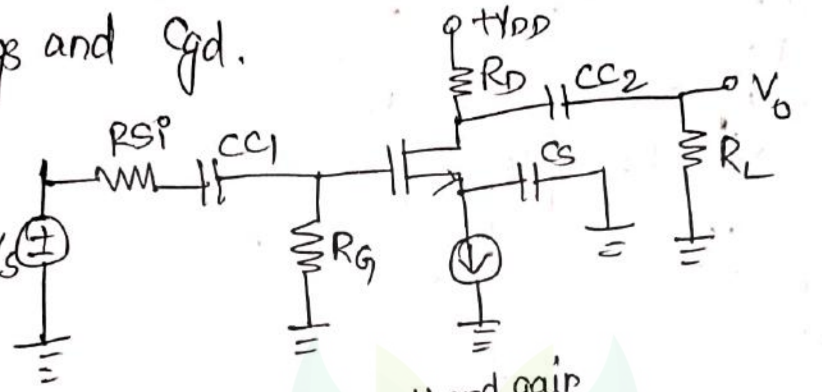
iv) O/P Resistance $R_o = \frac{1}{g_m} \| r_o$.

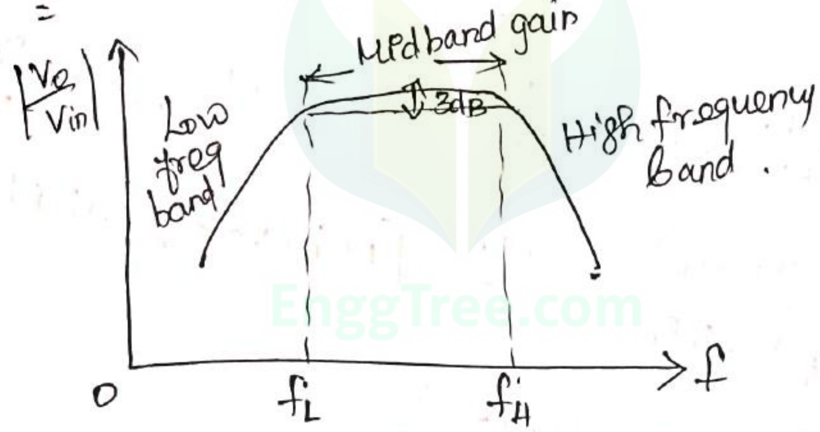
$$\boxed{R_o = \frac{1}{g_m}.} \qquad \boxed{\frac{1}{g_m} \ll r_o}$$

FREQUENCY RESPONSE OF MOSFET AMPLIFIER:-

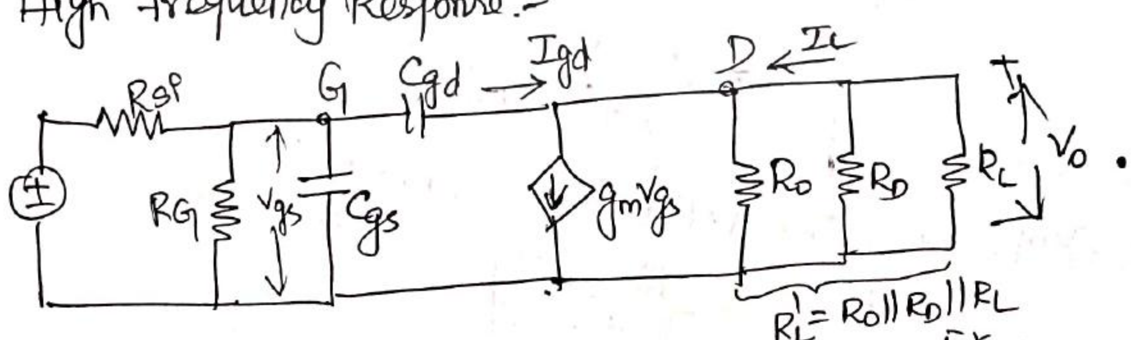
→ The below figure is CS MOSFET Amplifier

→ Its gain falls at high frequency due to the effect of C_{gs} and C_{gd}.





High frequency Response:-



Equivalent ckt for CS MOSFET Ampr.

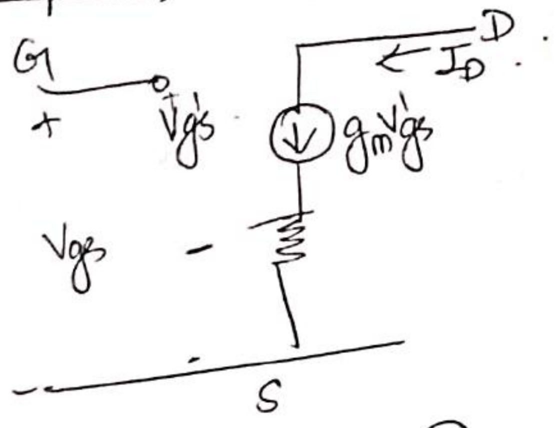
Let the load current is,

$$\boxed{I_L = g_m V_{gs} - I_{gd}}$$

$g_m V_{gs}$ → O/P current of MOSFET

I_{gd} → current through capacitance C_{gd}

High freq resp:-



$$I_d = g_m V'_{gs} \quad \text{—— (1)}$$

$$V_{gs} = V'_{gs} + (g_m V'_{gs}) r_s$$

$$= V'_{gs}[1 + g_m r_s]$$

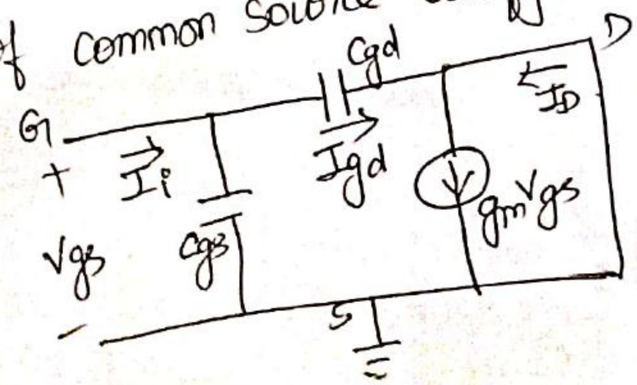
$$V'_{gs} = \frac{V_{gs}}{1 + g_m r_s} \quad \text{—— (2)}$$

Sub V'_{gs} in I_d.

$$\boxed{I_d = \frac{g_m \cdot V_{gs}}{[1 + g_m r_s]}}$$

Unit Gain freq:-

It is defined as freq. at which short ckt current gain of common source config. becomes unity.



Apply KCL,

$$I_D = \frac{V_{gs}}{\left(\frac{1}{j\omega C_{gs}}\right)} + \frac{V_{gs}}{\left(\frac{1}{j\omega C_{gd}}\right)} \longrightarrow (1)$$

$= j\omega C_{gs} V_{gs} + j\omega C_{gd} V_{gs}$.

$I_i = j\omega V_{gs}[C_{gs} + C_{gd}] \longrightarrow (2)$

Similarly Apply KCL at o/p node,

$\frac{V_{gs}}{\frac{1}{j\omega C_{gd}}} + I_D = g_m V_{gs} \longrightarrow (3)$.

$j\omega C_{gd} V_{gs} + I_D = g_m V_{gs}$.

$I_D = g_m V_{gs} - j\omega V_{gs} C_{gd}$.

$= V_{gs}[g_m - j\omega C_{gd}]$

$$\boxed{V_{gs} = \frac{I_D}{[g_m - j\omega C_{gd}]}} \longrightarrow (4)$$

Sub(4) in (2)

$$I_i = \frac{I_d[j\omega(C_{gs} + C_{gd})]}{[g_m - j\omega C_{gd}]}$$

$$A_i = \frac{I_d}{I_i} = \frac{(g_m - j\omega C_{gd})}{[j\omega(C_{gs} + C_{gd})]} \longrightarrow (5)$$

if $C_{gd} = 0.05pF$ and $g_m = 1mA/V$ for $f = 100MHz$.

$\omega C_{gd} << g_m$.

eq(5) becomes,

$$A_I = \frac{g_m}{[j\omega(C_{gs} + C_{gd})]} \longrightarrow (6)$$

For unit Gain

$$A_I = 1$$

$$1 = \frac{g_m}{[2\pi f_T (C_{gs}+C_{gd})]}$$

$$\boxed{f_T = \frac{g_m}{2\pi[C_{gs}+C_{gd}]}}$$

Pbm

1) Determine the Unity gain BW of MOSFET. The transistor Parameter are $K_n = 0.25\,mA/V^2$, $V_T = 1V$, $\lambda = 0$, $C_{gd} = 0.04\,PF$, $C_{gs} = 0.2\,Pf$ and assume $V_{gs} = 3V$

$$g_m = 2K_n(V_{GS} - V_T) = 1\,mA/V.$$

$$f_T = \frac{g_m}{2\pi[C_{gs}+C_{gd}]} = 663\,MHZ$$

2) Find the midband gain A_M and upper 3dB freq f_H of CS Amp. freq with s/g source having an internal Resistance $R_{sig} = 100\,k\Omega$. The amplifier has $R_G = 4.7\,M\Omega$, $g_m = 1\,mA/V$, $r_o = 150\,k\Omega$, $C_{gs} = 1\,pf$, $R_D = R_L = 1.5\,k\Omega$, $C_{gd} = 0.4\,Pf$.

$$A_M = \frac{-R_G}{R_G + R_{sig}} g_m R_L' = -7$$

$$R_L' = r_o \| R_D \| R_L$$

$$C_{eq} = (1 + g_m R_L')C_{gd} = 3.26\,Pf$$

$$C_{in} = C_{gs} + C_{gd} = 4.26\,Pf$$

$$f_H = \frac{1}{2\pi C_{in}(R_{sig} \| R_G)} = 382\,KHZ$$

Low Frequency Response:-

→ The low freq. response of MOSFET is affected by three RC Networks.

→ The corner frequency due to 3 RC Networks are

$$f_1 = \frac{1}{2\pi C_{C1}(R_{Si}+R_G)} \quad \text{(Network 1)}$$

$$f_1' = \frac{g_m}{2\pi C_S} \quad \text{(Network 2)}$$

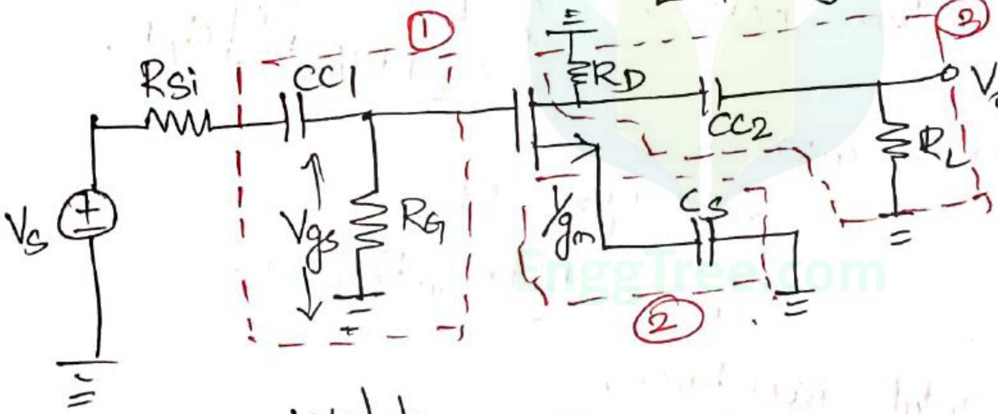
$$f_1'' = \frac{1}{2\pi C_{C2}(R_D+R_L)} \quad \text{(Network 3)}$$

Overall low freq. Transfer function is given by

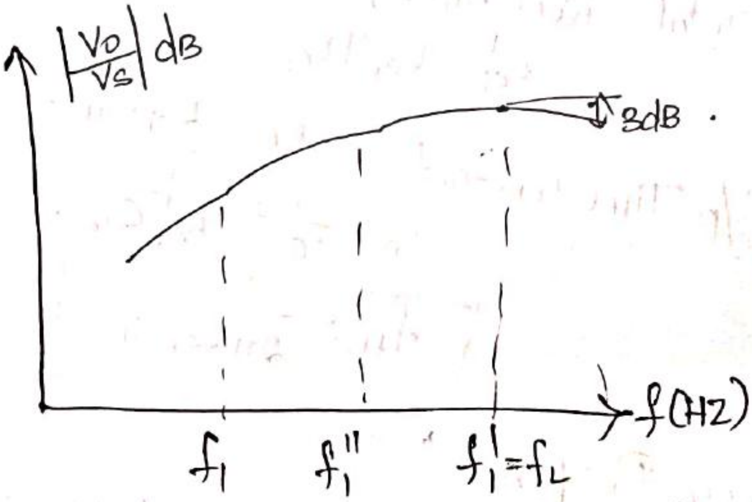
$$\frac{V_o}{V_S} = \frac{-g_m R_L' V_{gs}}{V_S}$$

$$= \frac{-g_m [R_L \| R_D] \cdot R_G V_{gs}}{V_i (R_G + R_{Si})} \quad \left\{ \because V_S = V_i \frac{(R_{Si}+R_G)}{R_G},\ V_i = V_{gs} \right.$$

$$\frac{V_o}{V_S} = \left[-g_m (R_L \| R_D)\right] \left[\frac{R_G}{R_G+R_{Si}}\right] \left[\frac{S}{S+\omega_1}\right] \left[\frac{S}{S+\omega_1'}\right] \left[\frac{S}{S+\omega_1''}\right]$$



Response.



→ The highest of these 3 frequencies is 3dB freq. f_L

→ Most of the times, f_1' is higher than the other two and hence the lower 3dB frequency.

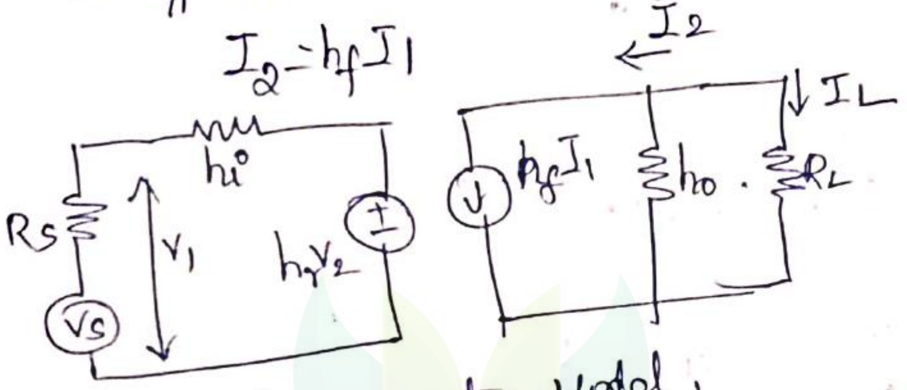
verified
M. [signature] 13/9/19
(Dr. M. Ettappan)

...ysis of Transistor amp configuration using Simplified h-parameter Model.

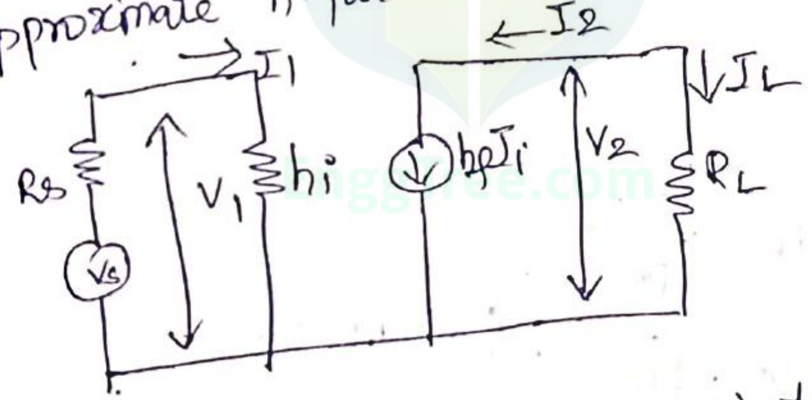
In h parameter Model admittance h_o is parallel to R_L. Parallel combination of 2 unequal impedance $h_o >> R_L$. so h_o is Neglected.

So o/p current is,

$I_2 = h_f I_1$

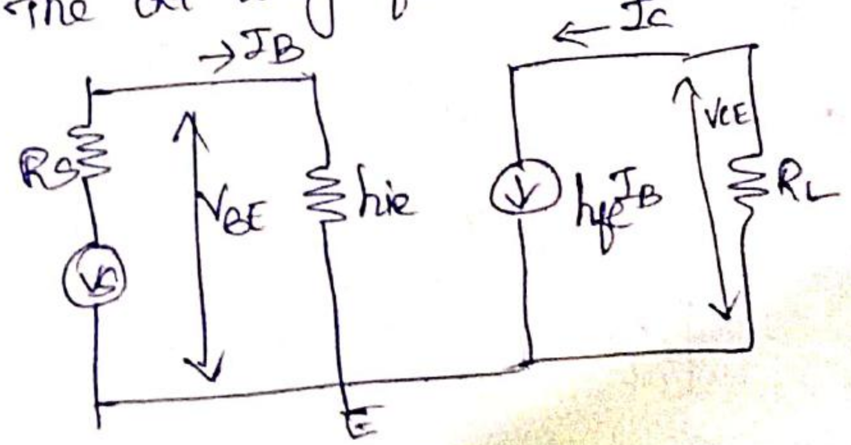


Approximate h-parameter Model,



Analysis of CE amplifier using approximate Model

The ckt diag for CE model ampr



Current Gain,

$$A_I = \frac{-h_{fe}}{1+h_{oe}R_L} \longrightarrow (1)$$

h_{oe} is Neglected

$$\boxed{A_I = -h_{fe}} \longrightarrow (2)$$

I/p Imp:-

$$R_i = h_{ie} - \frac{h_{re}h_{fe}}{h_{oe}R_L}.$$

In approximation,

$$\boxed{R_i = h_{ie}} \longrightarrow (3)$$

Voltage gain:

$$\boxed{A_V = A_I\left(\frac{R_L}{R_i}\right)} \longrightarrow (4)$$

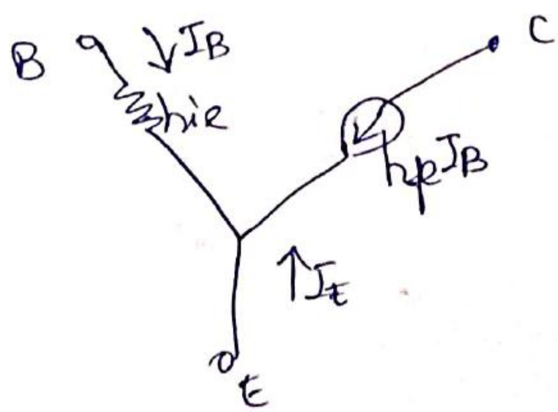
O/p Imp:-

$$Y_o = h_{oe} - \frac{h_{re}h_{fe}}{h_{ie}+R_S}.$$

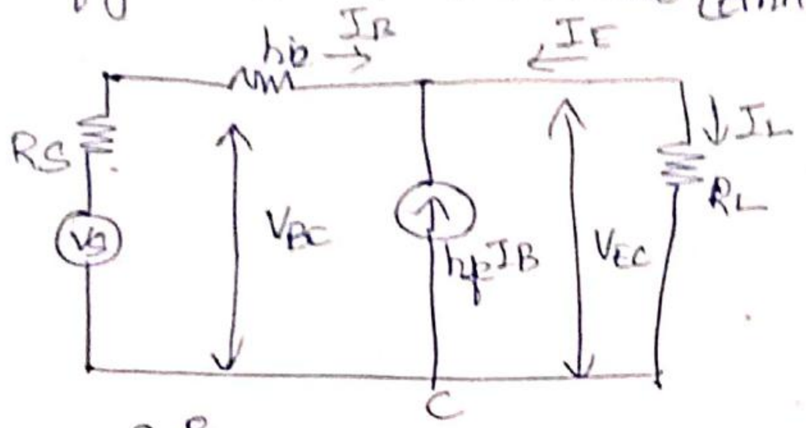
$Y_o = 0$. [Neglect h_{re} & h_{oe}] .

O/p Resistance

$$R_o = \frac{1}{Y_o} = \frac{1}{0} = \infty .$$



CC configuration Approximate Model [Emitter follower]



i) Current Gain,

$$I_E = h_{fe} I_B + I_B$$

$$= I_B[1+h_{fe}] \longrightarrow (1)$$

$$A_I = \frac{I_E}{I_B} = \frac{I_B(1+h_{fe})}{I_B} = (1+h_{fe}) \longrightarrow (2)$$

ii) I/P Resistance :-

From the above ckt diag V_{BC} is,

$$V_{BC} = h_{ie} I_B + (1+h_{fe}) I_B R_L \longrightarrow (3)$$

I/P Resistance $R_i = \frac{V_{BC}}{I_B} = \frac{h_{ie} I_B + (1+h_{fe}) I_B R_L}{I_B}$

$$\boxed{R_i = h_{ie} + (1+h_{fe}) R_L} \longrightarrow (4)$$

iii) Voltage Gain :-

$$A_V = \frac{V_{EC}}{V_{BC}} = \frac{(1+h_{fe}) I_B R_L}{h_{ie} I_B + (1+h_{fe}) I_B R_L}$$

$$A_V = \frac{(1+h_{fe})R_L}{h_{ie} + (1+h_{fe})R_L} \longrightarrow (5)$$

if $(1+h_{fe}) >> h_{ie}$

$$A_V = \frac{(1+h_{fe})R_L}{(1+h_{fe})R_L} = 1$$

O/p Resistance,

$$R_O = \frac{V_{EC}}{I_E}.$$

Apply KVL,

$$I_B R_S + I_B h_{ie} + V_{EC} = V_S.$$

Put $V_S = 0$.

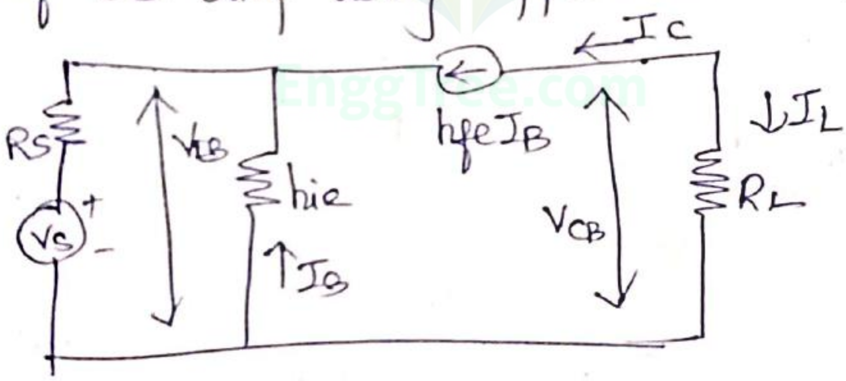
$$I_B [R_S + h_{ie}] = -V_{EC} \longrightarrow (6)$$

We know $I_E = -[1 + h_{fe}] I_B \longrightarrow (7)$

Sub 6 & 7 in RO,

$$R_O = \frac{-I_B [R_S + h_{ie}]}{-I_B [1 + h_{fe}]} = \frac{R_S + h_{ie}}{1 + h_{fe}}.$$

Analysis of CB amp using approximate h-parameter



Current Gain:-

$$A_I = \frac{-I_C}{I_E} = \frac{-h_{fe} I_B}{I_E} \longrightarrow (1)$$

$$I_E = -h_{fe} I_B - I_B.$$

$$= -I_B [1 + h_{fe}] \longrightarrow (2)$$

Sub (2) in (1)

$$A_I = \frac{-h_{fe} I_B}{-(1 + h_{fe}) I_B} = \frac{h_{fe}}{1 + h_{fe}}. \longrightarrow (3)$$

I/P Resistance,

$$R_i = \frac{V_{EB}}{I_E} = \frac{-h_{ie} I_B}{-(1+h_{fe}) I_B} = \frac{h_{ie}}{1+h_{fe}}.$$

Voltage Gain :-

$$A_V = \frac{V_{CB}}{V_{EB}} = \frac{-h_{fe} I_B R_L}{-h_{ie} I_B} = \left(\frac{h_{fe}}{h_{ie}}\right) R_L.$$

O/P Resistance (R_o)

$$R_o = \left.\frac{V_{CB}}{I_C}\right|_{V_S=0}.$$

$$R_o = \infty.$$

Quantity.	CE	CB	CC.
A_i	$-h_{fe}$.	$\frac{h_{fe}}{1+h_{fe}}$	$1+h_{fe}$
R_i	h_{ie}	$\frac{h_{ie}}{1+h_{fe}}$	$h_{ie}+(1+h_{fe})R_L$
A_V	$\frac{h_{fe} R_L}{h_{ie}}$	$\frac{h_{fe} R_L}{R_e}$	$1-\frac{h_{ie}}{R_i}$
R_o.	∞	∞	$\frac{h_{ie}+R_s}{1+h_{fe}}$.

UNIT - 4

MULTISTAGE AMPLIFIER & DIFFERENTIAL AMPLIFIER

Multistage Amplifier :-

→ An amplifier should have a desired voltage gain & current gain and it should match its input impedance of source with o/p impedance of load but with single stage amplifier this cannot be achieved.

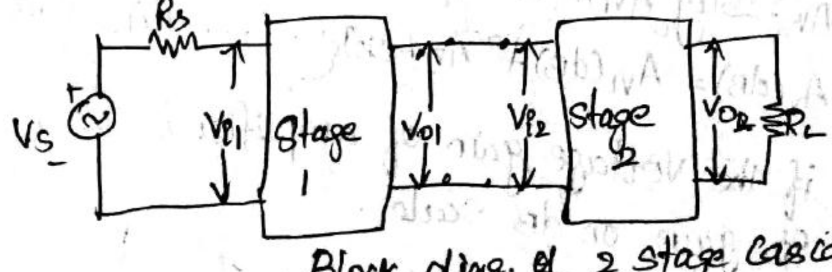
→ Therefore more than one amplifier stages are cascaded so that the i/p and o/p stages provide impedance matching requirement with some amplification and remaining middle layer provide most of the amplification.

Limitations of multistage amplifier :-

1. The bandwidth of multistage amplifier is always less than that of bandwidth of single stage amplifier.
2. Non linear distortion is more in multistage amplifier than single stage amplifier.

Two stage Cascaded Amplifier.

The block diagram of two stage cascaded amplifier is shown below. The stages are connected such that the o/p of first stage is connected to the i/p of second stage.



Block diag. of 2 stage cascade Amplifier

V_{i1} is i/p of 1st stage and V_{o2} is o/p of second stage.

Therefore overall voltage gain of two stage cascade amplifier can be written as,

$$A_V = \frac{V_{o2}}{V_{i1}} = \frac{V_{o2}}{V_{i2}} \times \frac{V_{i2}}{V_{i1}} \rightarrow (1)$$

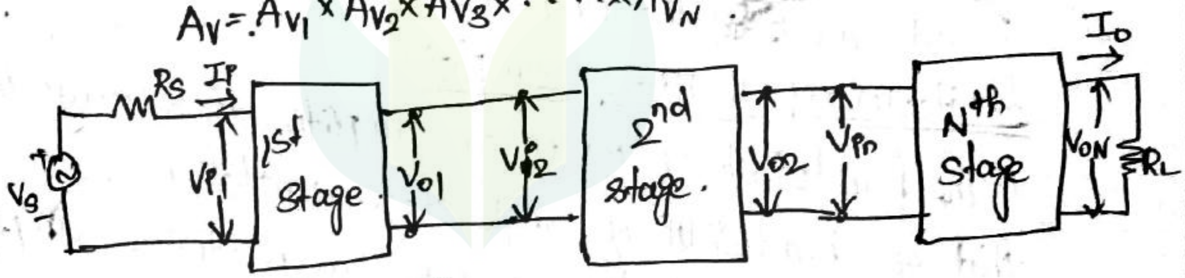
where $V_{o1} = V_{i2}$

$$A_V = \frac{V_{o2}}{V_{i2}} \times \frac{V_{o1}}{V_{i1}} = A_{V2} \cdot A_{V1}$$

$$\therefore \boxed{A_V = A_{V2} \cdot A_{V1}}$$ ⇒ It is the product of voltage gain of individual stages.

N stage cascaded Amplifier:-

$$A_V = A_{V1} \times A_{V2} \times A_{V3} \times \cdots \times A_{VN}$$



Gain of multistage amplifier:-

It is represented in terms of decibel (dB).

$$N = 10 \log_{10}\left(\frac{\text{o/p Power}}{\text{I/p Power}}\right).$$

The gain of a multistage amplifier can be easily calculated if the gain of individual stages are known in dB.

$$20\log_{10} A_V = 20\log_{10} A_{V1} + 20\log_{10} A_{V2} + \cdots + 20\log_{10} A_{VN}.$$

$$A_V(dB) = A_{V1}(dB) + A_{V2}(dB) + \cdots + A_{VN}(dB).$$

Problem-1 if the voltage gain of amplifier is 100, Calculate its gain on dB scale.

$$\text{Gain in dB} = 20\log_{10}(100) = 40\,dB.$$

2 ②

2 Amplifiers having gain 20dB and 40dB are cascaded. Find the overall gain in dB.

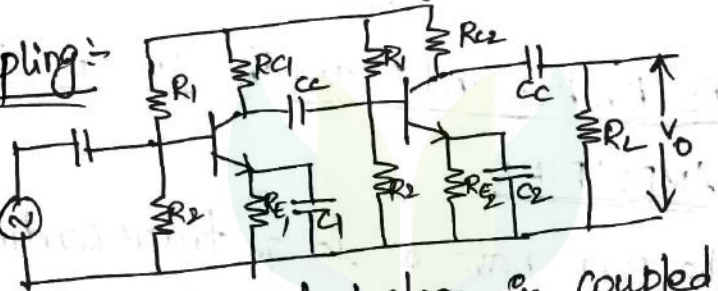
$$A_V(dB) = A_{V_1}(dB) + A_{V_2}(dB)$$
$$= 20 + 40 = 60dB.$$

Methods of coupling Multistage Amplifier.

In multistage amplifier the o/p s/g of preceding stage is to be coupled to the i/p circuit of succeeding stage.

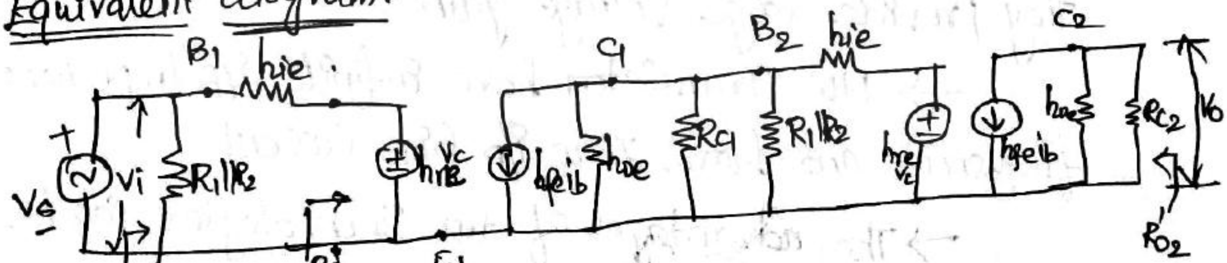
* RC coupling
* Transformer coupling.
* Direct coupling.

RC Coupling:-



Here the o/p s/g of first stage is coupled to the i/p of next stage through coupling capacitor. (CE - CE cascade Amplifier).

Equivalent diagram:-



Analysis of 2nd CE:-

Current gain $A_{i_2} = -h_{fe}$, where $h_{oe}R_L < 0.1$

I/P Resistance $R_{i_2} = h_{ie}$.

Voltage gain $A_{V_2} = \frac{A_{i_2} \times R_{L_2}}{R_{i_2}} \rightarrow ①$

Analysis of 1st stage:- Here $h_{oe} R_{L1} < 0.1$

Current gain $A_{i1} = -h_{fe}$.

I/P Resistance $R_{i1} = h_{ie}$

Voltage gain $A_{V1} = \frac{A_{i1} \times R_{L1}}{R_{i1}}$

Overall Voltage gain $\Rightarrow A_{V2} \times A_{V1}$

$$= \left[\frac{A_{i2} \times R_L}{R_{i2}}\right]\left[\frac{A_{i1} R_{L1}}{R_{i1}}\right]$$

$$= A_V \cdot \frac{R_{i1}'}{R_{i1}' + R_S}$$ where $R_{i1}' = R_1 \| R_2 \| R_{i1}$

Problem

1) Calculate A_I, A_V, A_{VS}, and R_o for the cascade circuit.

BICMOS AMPLIFIER:-

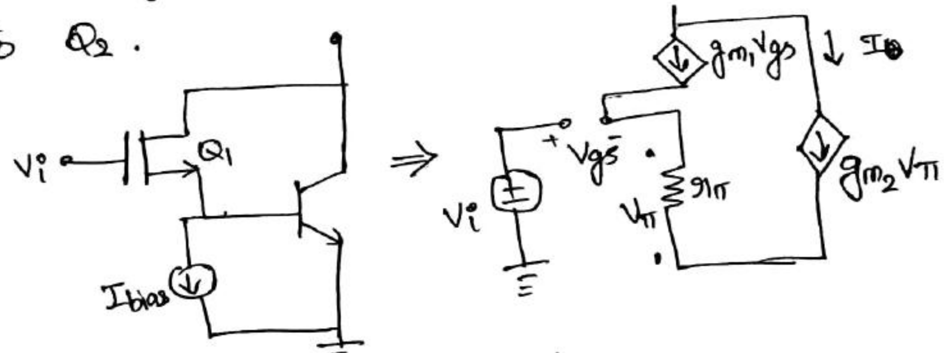
→ The BJT have a large transconductance than MOS transistor biased at the same current level and they have higher switching speed. Due to large g_m, they provide large voltage gain.

→ MOS Transistor have infinite i/p impedance at low frequencies and have zero i/p bias current.

→ The advantages of two Technologies can be done by combining BJT with MOS on the same substrate, i.e In the same integrated circuit. Such a Technology is called BICMOS Technology.

→ Ibias are bias current and some equivalent element to control the quiescent current in Q1. The effective current gain of BJT is boosted in this circuit. ⑨

→ It has high i/p resistance and large transconductance due to Q_2.



* Assume $r_o = \infty$ in both Transistors

* The o/p current $I_o = g_{m_1}V_{gs} + g_{m_2}V_\pi \longrightarrow (1)$

Voltage across r_π $\boxed{V_\pi = g_{m_1}V_{gs} \cdot r_\pi} \longrightarrow (2)$.

I/p voltage $V_i = V_{gs} + V_\pi$. ⇒ we know.

$V_\pi = g_{m_1}V_{gs}r_\pi$
sub in V_i
$\therefore V_i = V_{gs} + g_{m_1}V_{gs}r_\pi$
$V_i = V_{gs}[1 + g_{m_1}r_\pi]$

Voltage divider rule} $V_{gs} = \dfrac{V_i}{1 + g_{m_1}r_\pi} \longrightarrow (3)$

Sub (2) in (1).

$I_o = (g_{m_1} + g_{m_2}g_{m_1}r_\pi)V_{gs} \longrightarrow (4)$

Sub (3) in (4).

$$I_o = \frac{g_{m_1}(1 + g_{m_2}r_\pi)V_i}{1 + g_{m_2}r_\pi}$$

$\therefore \boxed{I_o = g_{m_1}V_i}$.

Differential Amplifier:-

→ The differential amplifier amplifies the difference between two i/p voltage S/g.

→ Let V_1 & V_2 are the two i/p signals in an ideal differential amplifier, the o/p voltage V_o is proportional to the difference between two i/p signals. $V_o = [V_1 - V_2]$

Differential gain (A_d)

$$V_o = A_d(V_1 - V_2)$$

$A_d \rightarrow$ Proportionality constant (differential gain).

The difference between the two i/p $(V_1 - V_2)$ is V_d.

$\therefore$ $V_o = A_d V_d$.

$$\boxed{A_d = \frac{V_o}{V_d}}$$

In decibel,

$$A_d = 20\log_{10}(A_d)\ [dB]$$

Common mode Gain (A_c)

Practically differential ampr not only depend on difference voltage but also depends on average common level of two i/p. Hence it is called common mode gain.

$$V_c = \frac{V_1 + V_2}{2}$$

The gain with which it amplifies the common mode signal to produce o/p is called common mode gain.

$$V_o = A_c V_c.$$

$$\boxed{V_o = A_d V_d + A_c V_c}$$

Common mode Rejection ratio (CMRR)

It is defined as ratio of differential voltage gain A_d to common mode voltage gain A_c.

$$CMRR = \left|\frac{A_d}{A_c}\right|$$

$$CMRR = 20\log_{10}\left|\frac{A_d}{A_c}\right| dB.$$

Features of differential amplifier:-

i) High differential voltage gain.

ii) Low common mode gain

iii) High i/p impedance.

iv) Large Bandwidth.

(9)

v) Low o/p impedance.
vi) Low offset voltage & current.

CMRR o/p voltage:-

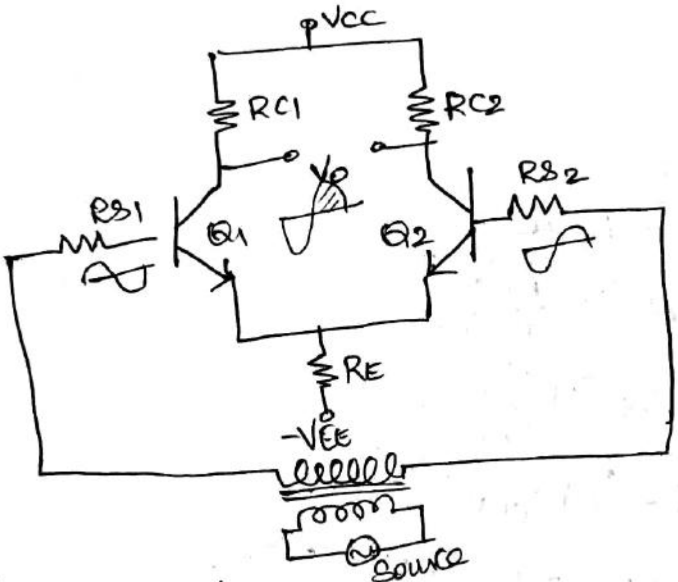
$$V_0 = A_d V_d + A_c V_c$$
$$= A_d V_d \left(1 + \frac{A_c V_c}{A_d V_d}\right)$$
$$= A_d V_d \left(1 + \frac{1}{\frac{A_d}{A_c}} \cdot \frac{V_c}{V_d}\right)$$
$$V_0 = A_d V_d \left[1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d}\right]$$

OPERATION OF DIFFERENTIAL AMPLIFIER.

i) Differential mode operation
ii) Common mode operation.

Differential mode:-

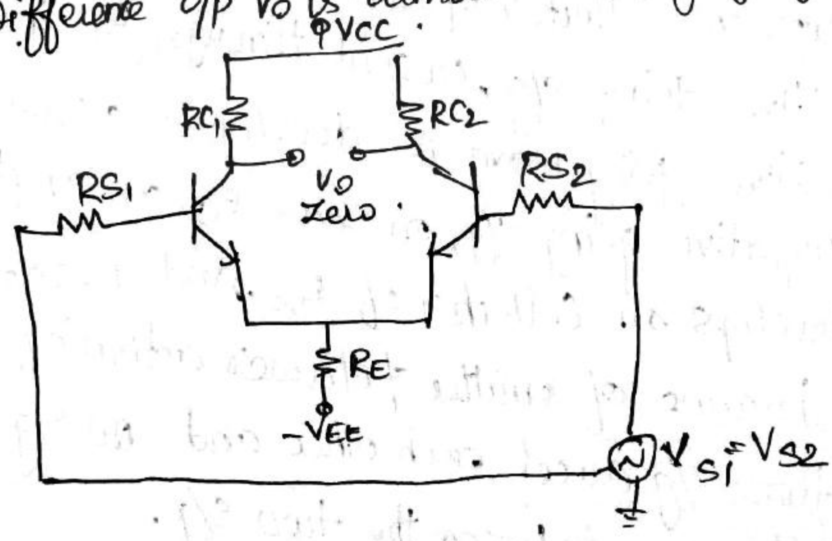
* In this mode, the two signals are different from each other which are same in magnitude but 180° out of phase.
* Assume sine wave on base of Q_1 is positive going, base of Q_2 is negative going.
* With positive going s/g on base Q_1 an amplified negative going develops on collector of Q_1.
* Due to positive going s/g, current through R_E increases and hence a positive going wave is developed across R_E.
* Due to negative going s/g, on base Q_2 an amplified positive going s/g develops on collector of Q_2. And negative s/g across R_E develops, because of emitter follower action of Q_2
* Hence two s/g cancel each other and no s/g across R_E.
* V_0 is difference between the two s/g.
* In differential mode V_0 is twice as large as s/g voltage from either collector to ground.



Differential mode operation

Common mode operation.

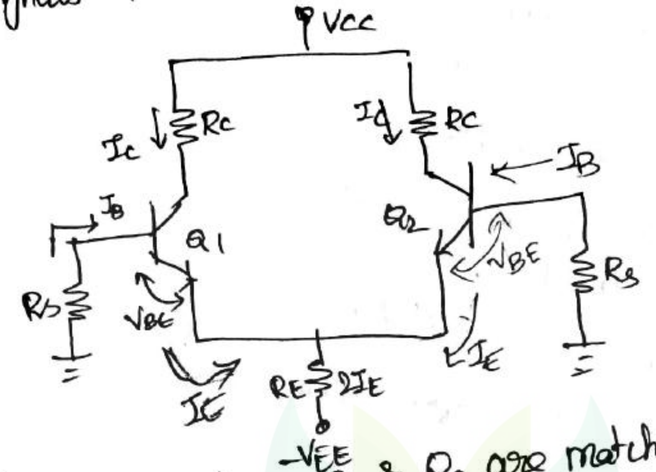
* In this mode, signals applied to base Q_1 & Q_2 are derived from same source.
* Two signals equal in magnitude as well as in phase.
* Two signals equal in magnitude at base of Q_1 & Q_2 causes in
* In phase signal voltages at base of Q_1 & Q_2 causes in phase signal voltages to appear across R_E, which gets added.
* R_E causes s/g current and provides -Ve feedback.
* o/p is difference between two collector voltage, which are equal and same in phase.
* Difference o/p Vo is almost zero, negligibly small.



DC Analysis of differential Amplifier :-

(8)

The DC analysis means to obtain the operating point value I_{CQ} and V_{CEQ} for transistors used. The Supply voltage are DC, while the i/p signals are AC. So dc equivalent circuit can be obtained simply by reducing the i/p AC signals to zero.



DC Equivalent circuit

→ The Transistors Q_1 & Q_2 are matched transistor and hence for such a matched pair, we can assume same characteristics.

(i) Both Transistor have

ii) $R_{E_1} = R_{E_2}$ have $R_E = R_{E1} \parallel R_{E2}$

iii) $R_{C1} = R_{C2}$ denoted as R_C.

iv) $|V_{CC}| = |V_{EE}|$ both are measured with respect to ground.

Apply KVL to base-Emitter of Q_1,

$$-I_B R_S - V_{BE} + V_{EE} - 2 I_E R_E = 0 \longrightarrow (1)$$

$$I_C = \beta I_B \;\; \& \;\; I_C \simeq I_E \longrightarrow (2)$$

$$I_B = \frac{I_E}{\beta} \longrightarrow (3)$$

Sub (3) in (1)

$$-\frac{I_E}{\beta} R_S - V_{BE} - 2 I_E R_E = -V_{EE}$$

$$-I_E \left[\frac{R_S}{\beta} + 2R_E \right] - V_{BE} = -V_{EE}$$

$$\therefore V_{EE} = I_E\left(\frac{R_S}{\beta} + 2R_E\right) + V_{BE}.$$

$$\boxed{I_E = \frac{V_{EE} - V_{BE}}{\left(\frac{R_S}{\beta} + 2R_E\right)}}$$

Where $V_{BE} \simeq 0.6$ to 0.7 for silicon
0.2 for Ge.

In practice, generally $\frac{R_S}{\beta} << 2R_E$.

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E}.$$

Apply KVL to Transistor Q_1, o/p terminal

Now, $V_C = V_{CC} - I_C R_C \longrightarrow (3)$

$V_{CE} = V_C - V_E \longrightarrow (4)$.

Sub (3) in (4).

$V_{CE} = V_{CC} - I_C R_C + V_{BE}$. $\quad V_E = -V_{BE}$

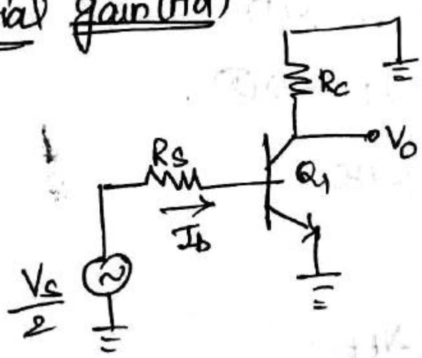
Where $I_C = I_{CQ}$, $V_{CE} = V_{CEQ}$.

$$\boxed{I_E = \frac{V_{EE} - V_{BE}}{R_S/\beta + 2R_E}}$$

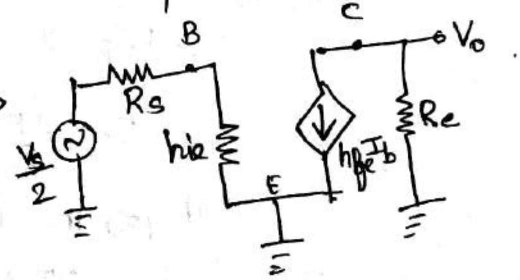
<u>Ac Analysis of differential amplifier using h-parameter</u>.

In Ac analysis the differential gain A_d, Common mode gain A_c, i/p impedance (Resistance) R_i & o/p Resistance R_o of the differential amplifier using h-parameter.

<u>Differential gain (A_d)</u>



Equivalent circuit



(6)

* For differential gain calculation two i/p signals must be different from each other.
* Two AC i/p S/g be equal in magnitude but 180° out of phase difference in between them.
* The magnitude of each AC i/p S/g V_{S1} & V_{S2} be $V_s/2$
* The two AC emitter current I_{E1} & I_{E2} are equal.
* The circuit can be analysed by considering only one transistor. This is called half circuit concept of Analysis.

Apply KVL in i/p loop.

$$\frac{V_s}{2} - i_b R_s - h_{ie} i_b = 0$$

$$-i_b(R_s + h_{ie}) = -V_s/2$$

$$\boxed{i_b = \frac{V_s}{2(R_s + h_{ie})}} \longrightarrow (1)$$

Apply KVL in o/p loop.

$$V_o = -h_{fe} I_b R_C \longrightarrow (2)$$

Sub (1) in (2)

$$V_o = -h_{fe} \cdot R_C \frac{V_s}{2(R_s + h_{ie})}$$

$$\boxed{\frac{V_o}{V_s} = \frac{-h_{fe} R_C}{2(R_s + h_{ie})}}$$

(−) sign ⇒ phase difference b/w i/p & o/p.

$V_d = V_1 - V_2$ [differential mode].

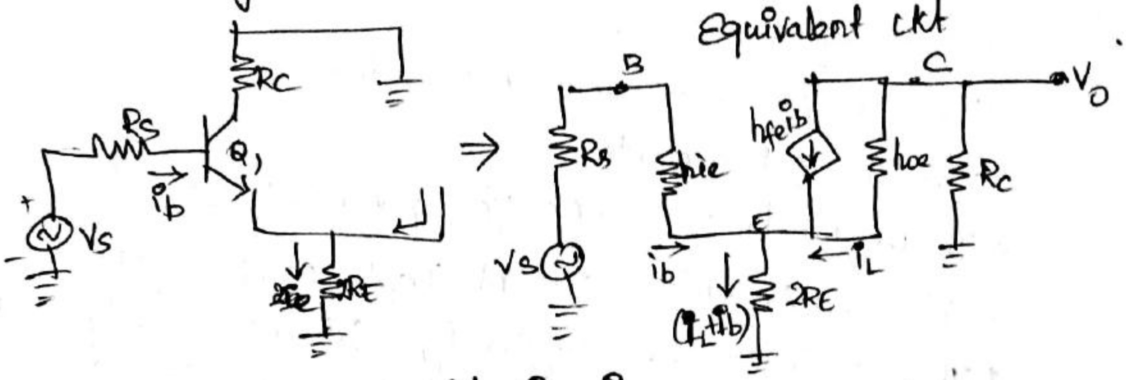
$$= \frac{V_s}{2} - \left(\frac{-V_s}{2}\right) = V_s$$

Magnitude of differential gain is, o/p double the i/p.

$$A_d = 2\frac{V_o}{V_s} = \frac{h_{fe} R_C}{(R_s + h_{ie})}$$

$$\boxed{A_d = \frac{h_{fe} R_C}{R_s + h_{ie}}}$$

Common mode gain (A_c)



* Emitter Resistance current $= i_L + i_b$

Emitter resistance $= 2R_E$.

$\therefore$ Current through $h_{oe} = (i_L - h_{fe} i_b)$.

step-1. Apply KVL in i/p side.

$$V_S - i_b R_S - i_b h_{ie} - 2R_E(i_b + i_L) = 0$$

$$V_S = i_b(R_S + h_{ie} + 2R_E) + i_L(2R_E) \longrightarrow ①$$

$$V_o = -i_L R_C \longrightarrow ②$$

step-2 Apply KVL in o/p side,

$$-\frac{(i_L - h_{fe} i_b)}{h_{oe}} - 2R_E(i_L + i_b) - i_L R_C = 0$$

$$-\frac{i_L}{h_{oe}} + \frac{h_{fe} i_b}{h_{oe}} - 2R_E i_L - 2R_E i_b - i_L R_C = 0$$

$$i_b\left[\frac{h_{fe}}{h_{oe}} - 2R_E\right] = i_L\left[\frac{1}{h_{oe}} + 2R_E + R_C\right]$$

$$i_b\left[\frac{h_{fe} - 2R_E h_{oe}}{\cancel{h_{oe}}}\right] = i_L\left[\frac{1 + 2R_E h_{oe} + R_C h_{oe}}{\cancel{h_{oe}}}\right]$$

$$\frac{i_L}{i_b} = \frac{h_{fe} - 2R_E h_{oe}}{1 + h_{oe}(2R_E + R_C)}$$

$$\boxed{i_b = \frac{i_L(1 + h_{oe}(2R_E + R_C))}{h_{fe} - 2R_E h_{oe}}} \longrightarrow ③$$

Sub eq (3) in (1).

$$V_S = \frac{[1+(2R_E+R_C)h_{oe}]}{[h_{fe}-2R_Eh_{oe}]}[R_S+h_{ie}+2R_E]i_L + 2R_E i_L.$$

$$\frac{V_S}{i_L} = \frac{[1+2R_Eh_{oe}+R_Ch_{oe}][R_S+h_{ie}+2R_E]+2R_E[h_{fe}-2R_Eh_{oe}]}{[h_{fe}-2R_Eh_{oe}]}$$

$$= \frac{\left\{\begin{array}{l} R_S+h_{ie}+2R_E+2R_ER_Sh_{oe}+2R_Eh_{oe}h_{ie}+4R_E^2h_{oe}+ \\ R_SR_Ch_{oe}+R_Ch_{ie}h_{oe}+2R_ER_Ch_{oe}+2R_Eh_{fe}-4R_E^2h_{oe} \end{array}\right\}}{[h_{fe}-2R_Eh_{oe}]}$$

$$\frac{V_S}{i_L} = \frac{2R_E[1+h_{fe}]+R_S[1+2R_Eh_{oe}]+h_{ie}[1+2R_Eh_{oe}]+h_{oe}R_C[R_S+h_{ie}+2R_E]}{[h_{fe}-2R_Eh_{oe}]} \longrightarrow (4)$$

Neglecting R_Ch_{oe} ⇒ because practically $R_Ch_{oe} \ll 1$

$$\frac{V_S}{i_L} = \frac{2R_E(1+h_{fe})+R_S(1+2R_Eh_{oe})+h_{ie}(1+2R_Eh_{oe})}{[h_{fe}-2R_Eh_{oe}]}$$

$$\frac{V_S}{i_L} = \frac{2R_E(1+h_{fe})+(1+2R_Eh_{oe})(R_S+h_{ie})}{h_{fe}-2R_Eh_{oe}}.$$

$$\therefore \quad i_L = \frac{(h_{fe}-2R_Eh_{oe})V_S}{2R_E(1+h_{fe})+(1+2R_Eh_{oe})(R_S+h_{ie})}$$

sub i_L in eq (2).

$$V_0 = \frac{-(h_{fe}-2R_Eh_{oe})V_SR_C}{2R_E(1+h_{fe})+(R_S+h_{ie})(1+2R_Eh_{oe})}$$

$$\frac{V_0}{V_S} = \frac{(2R_Eh_{oe}-h_{fe})R_C}{2R_E(1+h_{fe})+(R_S+h_{ie})(1+2R_Eh_{oe})} \longrightarrow (5)$$

Neglect $h_{oe}R_C \ll 1$ [Neglect h_{oe} all parameters]

Common mode:-

$$V_C = \frac{V_1+V_2}{2} = \frac{V_S+V_S}{2} = V_S \qquad \therefore A_C = \frac{V_0}{V_C} = \frac{-h_{fe}R_C}{2R_E(1+h_{fe})+(R_S+h_{ie})}$$

CMRR $= \left|\frac{A_d}{A_c}\right|$

$$= \left| \frac{\dfrac{h_{fe}R_C}{R_S+h_{ie}}}{\dfrac{h_{fe}R_C}{2R_E(1+h_{fe})+R_S+h_{ie}}} \right|$$

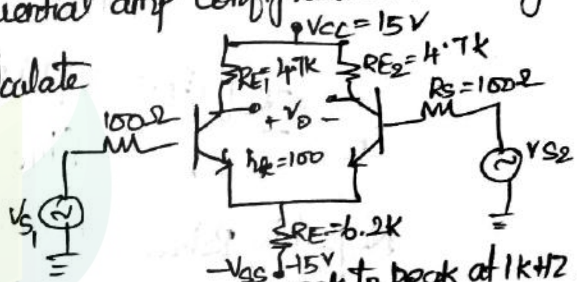
$$CMRR = \frac{R_S+h_{ie}+2R_E(1+h_{fe})}{R_S+h_{ie}}$$

Input Resistance, $R_P = \frac{V_S}{i_b} = 2(R_S+h_{ie})$ {Differential mode}.

o/p Resistance. $R_o = R_C$.

1) The dual i/p balanced o/p differential amp configuration, Assuming Silicon transistor $h_{ie} = 2.8K\Omega$. Calculate

1) operating point value
ii) Differential gain
iii) common mode gain
iv) CMRR.
v) o/p if $V_{S1} = 70mV$ peak to peak at 1KHz & $V_{S2} = 40mV$ peak to peak at 1KHz.



Solution

i) $I_{CQ} = I_E = \frac{V_{EE}-V_{BE}}{2R_E+\frac{R_S}{\beta}}$ $\qquad \beta = h_{fe} = 100$, $V_{BE} = 0.7V$

$$= \frac{15V-0.7}{2(6.8\times10^3)+\frac{100}{100}}$$

$\boxed{I_{CQ} = 1.05mA}$

$V_{CEQ} = V_{cc}+V_{BE}-I_CR_C$
$= 15+0.7-[1.05\times10^{-3}\times4.7\times10^3]$

$\boxed{V_{CEQ} = 10.75V}$

ii) Differential mode. $A_d = \frac{h_{fe}R_C}{R_S+h_{ie}} = \frac{100\times4.7\times10^3}{100+2.8\times10^3} = 162.06$ //.

iii) Common mode gain,

$$A_c = \frac{h_{fe} R_C}{2R_E(1+h_{fe}) + R_s + h_{ie}} = \frac{100 \times 4.7 \times 10^3}{2 \times 6.8 \times 10^3 (1+100) + 100 + 2.8 \times 10^3}$$

$$\boxed{A_c = 0.3414}$$

iv) CMRR.

$$\Rightarrow \frac{A_d}{A_c} = \frac{162.68}{0.34} = 474.65$$

$$CMRR = 20\log_{10}(474.65) = 53.52\,dB.$$

v) o/p voltage,

$$V_o = A_d V_d + A_c V_c.$$

$$V_o = (162.07)(30 \times 10^{-3}) + (0.34)(55 \times 10^{-3})$$

$$\boxed{V_o = 4.88V}$$

$$V_d = V_1 - V_2 = 70 - 40 = 30mV$$

$$V_c = \frac{V_1 + V_2}{2} = \frac{70 \times 10^{-3} + 40 \times 10^{-3}}{2} = 55mV$$

FET Input stages:-

→ In order to increase the i/p impedence (Z_i) of amplifiers a FET is used as 1st stage.

→ This kind of amplifiers consists of BJT & FET are termed as BIFET circuits

→ FET has lower overall gain than a two state BJT circuit. thus a two stage FET circuit is constructed by different ways

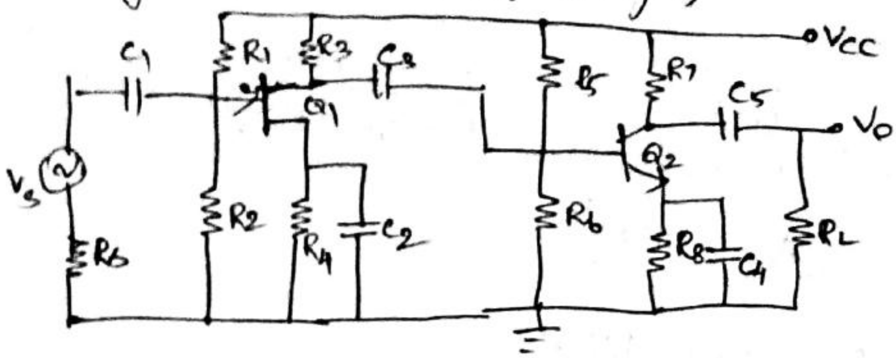
i) Capacitor Coupling BIFET amplifier.

→ The i/p stage provides very high Resistance and voltage gain usually ranging from 5 to 15.

→ stage 2 has typical Bipolar Voltage gain of 200 to 500 depending upon transistor parameter and resistor values

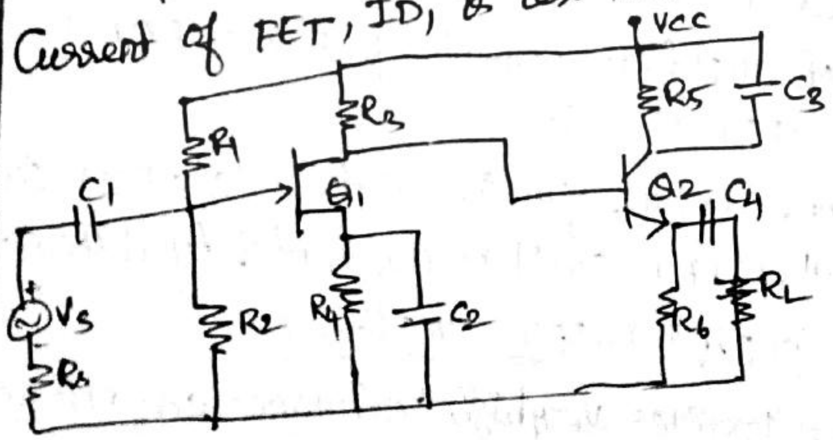
→ C_3 is the interstage coupling capacitor which couples FET

(First stage & BJT in second stage).



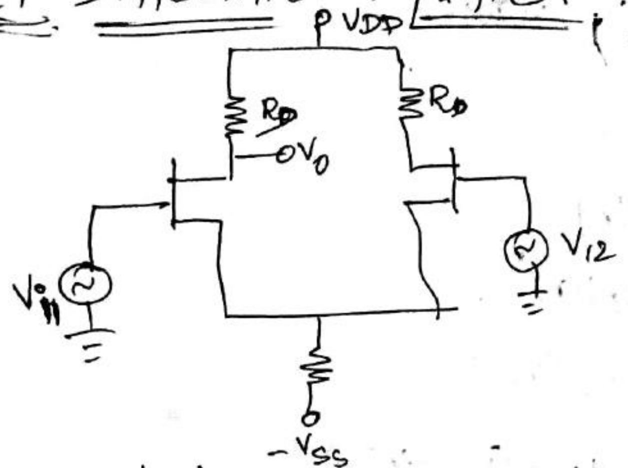
ii) **Direct coupled BJFET amplifier.**

* In this case 1st stage (FET) drain o/p is directly connected to the base of second stage (BJT) without coupling capacitor.
* In this figure, the transistor Q_1 is an N-channel JFET and Q_2 is PNP Transistor.
* The large voltage drop across the collector resistor R_5 causes a small voltage drop across Q_2 emitter resistor R_6.
* If the drain current of Q_1 is lower than the design level, the Q_2 transistor can also be driven into saturation.
* O/P voltage V_{CE} of Q_2 is increased when drain current of FET, I_{D1} is less than the I_{Dmax} design value.



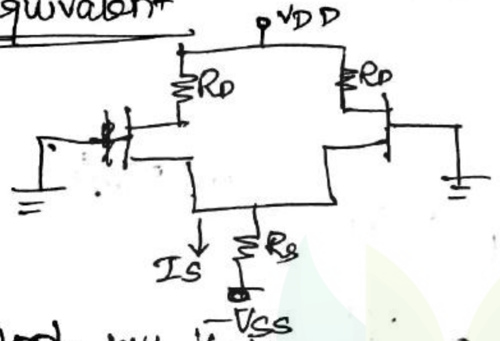
9

FET Differential Amplifier



Dual i/p
unbalanced o/p
JFET diff. ampr

DC equivalent



Apply KVL i/p

$$0 - V_{GS} - I_S R_S + V_{SS} = 0$$

$$I_S = \frac{V_{SS} - V_{GS}}{R_S}$$

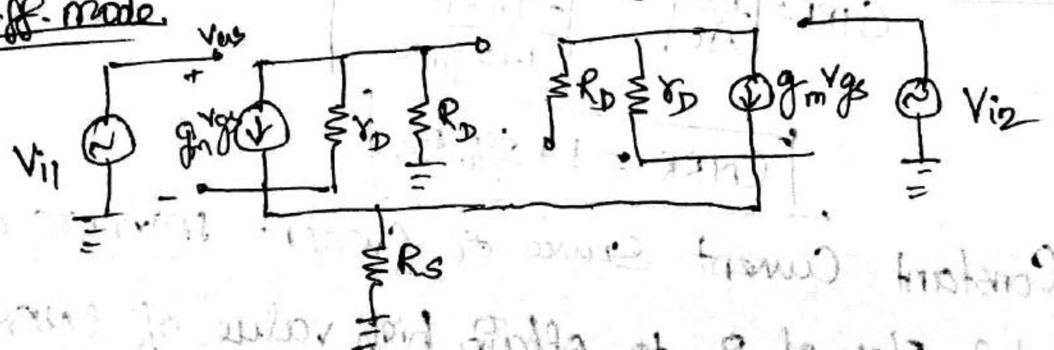
Apply KVL in o/p

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

$$V_{DS} = V_{DD} + V_{SS} - I_D R_D - I_S R_S$$

AC Analysis

Diff. mode



$$V_0 = V_{01} + V_{02}$$

$$V_{01} = I_0 (R_D \parallel r_d)$$

$$\Rightarrow -g_m V_{gs} (R_D \| r_d)$$

$$V_{o1} = -g_m V_{i1} (R_D \| r_d)$$

Considering V_{i2}.

$$V_{o2} = I_o (R_D \| r_d)$$

$$= +g_m V_{gs} (R_D \| r_d).$$

$$V_{o2} = +g_m V_{i2} (R_D \| r_d)$$

$$V_o = V_{o1} + V_{o2} = +g_m (R_D \| r_d) (-V_{i1} + V_{i2})$$

Common Mode

Apply KVL in i/p loop

$$V_i = V_{gs} + (2 g_m V_{gs}) R_s \Rightarrow V_i = V_{gs} (1 + 2 g_m R_s)$$

$$V_i = V_{gs} + (2 g_m V_{gs}) R_s$$

$$V_{gs} = \frac{V_i}{1 + 2 g_m R_s} \longrightarrow (1)$$

$$V_o = -g_m V_{gs} R_D \longrightarrow (2)$$

$$V_o = -g_m \frac{V_i}{1 + 2 g_m R_s} R_D$$

$$A_c = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + 2 g_m R_s}$$

CMRR

$$CMRR = \left| \frac{A_d}{A_c} \right| = \left| \frac{g_m R_D}{\frac{-g_m R_D}{1 + 2 g_m R_s}} \right|$$

$$\boxed{CMRR = 1 + 2 g_m R_s}$$

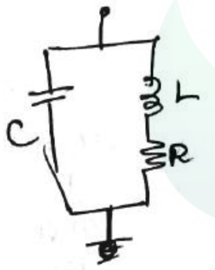
Constant current source or current mirrors can be used in place of R_s to obtain high value of CMRR.

SINGLE TUNED AMPLIFIER.

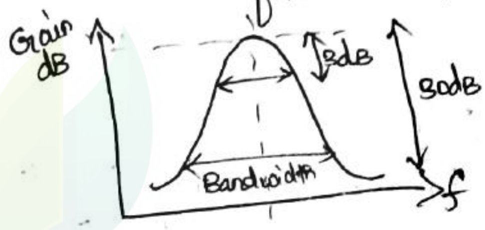
→ To amplify the selective range of frequencies the resistive load R_c is replaced by tuned circuit. The tuned Circuit is capable of amplifying a signal over a narrowband of frequencies centered at f_r. An amplifier with such a tuned circuit as a load are called <u>tuned Amplifier</u>.

→ Since tuned amplifier amplify narrow band of frequencies ⇒ Narrowband amplifiers.

Tuned circuit



Frequency Response of tuned Amp^r



→ LC ⇒ Tuned circuit which resonates at particular frequency.
The Resonance freq & impedance of tuned Circuit is,

$$\text{Resonant freq } (f_r) = \frac{1}{2\pi\sqrt{LC}}$$

$$\text{Impedance } Z_r = \frac{L}{C_2}$$

* At Resonance frequency the inductive & capacitive effect of tuned circuit cancel each other and resultant is like <u>Resistive</u>
* if freq ⇒ Above Resonant frequency the circuit is <u>capacitive</u>
* If frequency ⇒ Below Resonant frequency, the Circuit is <u>Inductive</u>

<u>Losses in tuned ckt</u> :-

Inductive coil } → Copper loss
Eddy current loss
Hysteresis Loss.

Q - Factor :- $= 2\pi \cdot \frac{\text{Maximum energy stored per cycle}}{\text{Energy dissipate per cycle}}$

Dissipation Factor $D = \frac{1}{Q}$.

Q Factor for Inductive :- $Q_L = \frac{\omega L_s}{R_s}$

Q Factor for capacitors. $Q_C = \frac{1}{C_s \omega R_s}$

Q. Factor [R || C] $\Rightarrow$ $Q = \omega R_p C_p$.

Bandwidth $= \frac{f_r}{Q_L}$

1) A tuned circuit Amplifier has maximum gain at a freq. 2MHz and Bandwidth 50KHz. Calculate Q Factor.

$$Q = \frac{f_r}{BW} = \frac{2\times10^{6}}{50\times10^{3}}$$

$$Q = 40.$$

Formula :-

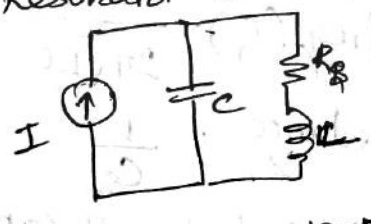
Parallel Resonant circuit.

$A_V = -g_m Q \omega L$

$f = \frac{1}{2\pi\sqrt{LC}}$

$Q = \frac{R_p}{\omega L}$

Series Resonant Circuit.



$\boxed{Q = \frac{\omega L}{R_s}}$

2) A resonant ckt has $C = 120pF$, $L = 100\mu H$, (series Resistance 5Ω)
Find quality factor & BW of circuit.

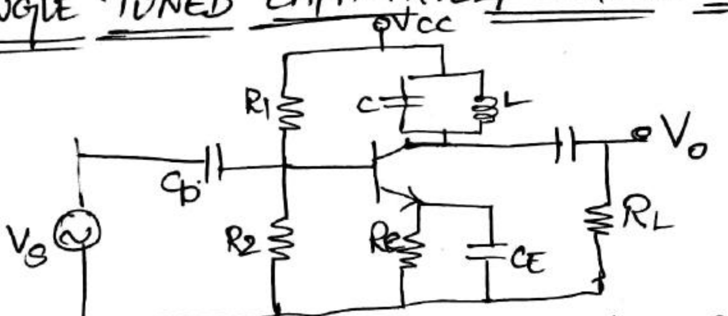
$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{100\times10^{-6}\times120\times10^{-12}}} = 1.45MHz$$

$$\omega = 2\pi f = 2\pi\times1.45\times10^{-6} = 9.125\times10^{6}$$

$$Q = \frac{\omega L}{R} = \frac{9.125\times10^{6}\times100\times10^{-6}}{5} = 182.57$$

$$BW = \frac{f_0}{Q} = \frac{1.45\times10^6}{182.57} \Rightarrow 7.957\,KHz.$$

Single Tuned Capacitively Coupled CE Amplifier



(Refer class notes)

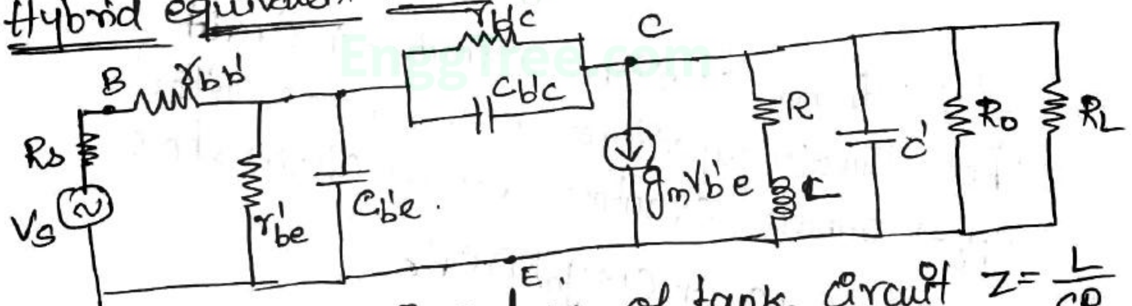
→ Resistors R_1 & R_2 provide biasing and R_E, C_E provide thermal stabilization.

→ The i/p signal is applied between base and Emitter.

The tank circuit is tuned in such a way that the resonant frequency becomes equal to the frequency of i/p signal.

→ Tuned amplifier amplifies only a selective range of frequency.

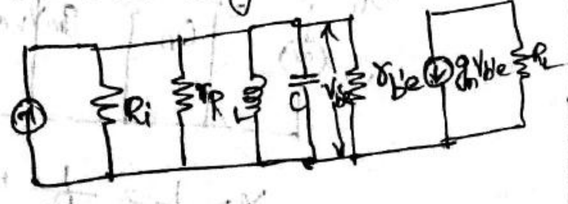
Hybrid equivalent circuit.



→ The resonance, impedance of tank circuit $Z = \frac{L}{CR}$ is high, o/p voltage is high either side of resonant frequency.

→ Admittance of series branch inductor is given by,

$$Y = \frac{1}{R+j\omega L} * \frac{R-j\omega L}{R-j\omega L}$$



$$= \frac{R-j\omega L}{R^2+\omega^2L^2}$$

$$= \frac{R}{R^2+\omega^2L^2} - \frac{j\omega L}{R^2+\omega^2L^2} \longrightarrow (1)$$

Admittance of the parallel circuit is given as,

$$Y = \frac{1}{R_p} + \frac{1}{j\omega L_p} \longrightarrow ②$$

Apply Millers theorem to the ckt,

$$C_{mi} = C_{b'e}(1+g_m R_L)$$

$$C_{mo} = C_{b'e}\left(\frac{1-g_m R_L}{g_m R_L}\right)$$

From ① & ②

$$R_p = \frac{R^2+\omega^2L^2}{R}$$

where $\omega_L >> R$

$$\therefore R_p = \frac{R\left(R+\frac{\omega^2L^2}{R}\right)}{R}$$

$$\therefore R_p = \frac{\omega^2L^2}{R}$$

$$\boxed{R_p = \omega L\, Q_0}$$

$$\omega L_p = \frac{R^2+\omega^2L^2}{\omega L}$$

$$L_p = \frac{R^2+\omega^2L^2}{\omega^2L^2}$$

$$L_p = \frac{R^2}{\omega^2L^2}+1$$

$$\boxed{Q_0 = \frac{R_p}{\omega_L}}$$

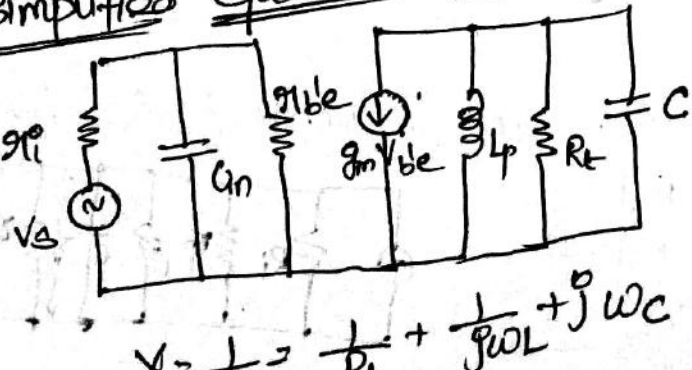
$C' \rightarrow$ External capacitance connected in circuit

$C_{b'e} \rightarrow$ Junction capacitance between base & Emitter

$C_{b'c} \rightarrow$ Junction capacitance between collector & base.

$$C_{in} = C_1 + C_{b'e} + (1+g_m R_L)C_{b'c}$$

<u>Simplified equivalent ckt:-</u>



$$Y = \frac{1}{Z} = \frac{1}{R_t} + \frac{1}{j\omega L} + j\omega C$$

(12)

$$Y = \frac{1}{R_t}\left[1 + \frac{R_t}{j\omega L} + R_t\, j\omega C\right]$$

$$= \frac{1}{R_t}\left[1 + \frac{R_t\,\omega_0}{j\omega_0\,\omega L} + \frac{R_t\,\omega_0 j\omega C}{\omega_0}\right] \left\{\text{Multiply } (\times)\ \frac{\omega_0}{\omega_0}\right\}.$$

$$Q = \frac{R_t}{\omega L}$$

$$= \frac{1}{R_t}\left[1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right].$$

Here $\delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1 \Rightarrow \frac{\omega}{\omega_0} = 1 + \delta$.

$$Z = \frac{R_t}{1 + jQ\left[1+\delta - \frac{1}{1+\delta}\right]}.$$

$$= \frac{R_t}{1 + jQ\delta\left(\frac{1+\delta/2}{1+\delta}\right)}$$

$$\boxed{Z = \frac{R_t}{1 + j2Q\delta}}$$

Gain

$$V_0 = -i_L \cdot Z$$

$$V_0 = -g_m V_{b'e} Z.$$

$$V_i = V_{b'e}$$

$$\therefore A_i = \frac{V_0}{V_i} = \frac{-g_m \cancel{V_{b'e}} Z}{\cancel{V_{b'e}}}$$

$$\boxed{A_i = -g_m \frac{R}{1 + jQ\delta}}$$

Condition

$$\left|\frac{A}{A_{ires}}\right| = \frac{1}{\sqrt{1 + (2Q\delta)^2}}$$

case(i) $\omega_1 < \omega_0$ (lower cutoff freq)

$$\frac{1}{\sqrt{2}} = \frac{1}{\sqrt{1 + (2Q\delta)^2}}$$

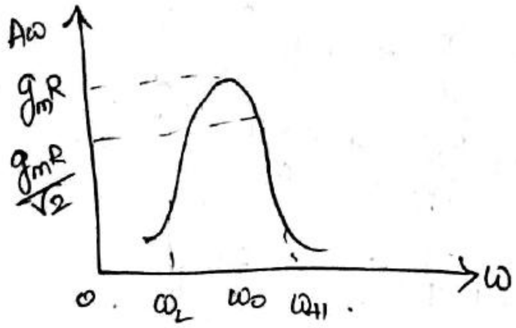
$$1 + 4Q^2\delta^2 = 2.$$

$$\boxed{\delta = \frac{-1}{2Q}}$$

case(ii) $\omega_2 > \omega_0$ (high cut off freq)

$$\boxed{\delta = \frac{1}{2Q}.}$$

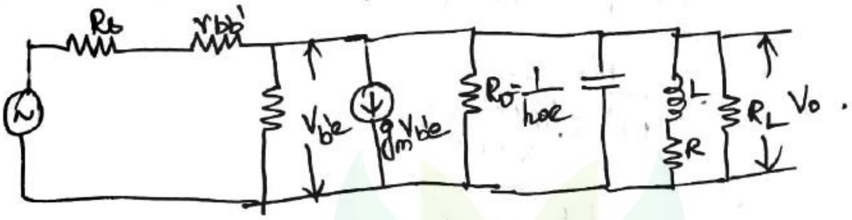
$$\text{Bandwidth} = f_2 - f_1 = \frac{\omega_0}{2\pi Q} \Rightarrow \frac{1}{2\pi RC}$$



FREQUENCY RESPONSE OF TUNED TRANSISTOR AMPLIFIER.

→ In order to obtain high gain, tuned amp^r can be used in cascade

→ The high voltage gain is accompanied by Narrow Bandwidth



$C = C' + C_{be} + (1 - A_v) C_{bc} \quad \{A_v = -g_m R_L\}$

$= \underbrace{C'}_{\text{External cap}} + \underbrace{C_{be}}_{\text{parasitic cap}} + \underbrace{(1 + g_m R_L) C_{bc}}_{\text{Miller's cap}}$

Admittance

$Y = \frac{1}{Z}$.

$Y = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C$.

÷ ~~R~~

$Y = \frac{1}{R}\left[1 + \frac{R}{j\omega L} + j\omega RC\right]$

× & ÷ by ω_0

$Y = \frac{1}{R}\left[1 + \frac{j\omega RC\omega_0}{\omega_0} - \frac{j\omega_0 R}{\omega\omega_0 L}\right]$

$\left\{ RC\omega_0 = \frac{R}{\omega_0 L} = Q \right\}$

$= \frac{1}{R}\left[1 + \frac{jQ\omega}{\omega_0} - \frac{jQ\omega_0}{\omega}\right]$.

$\therefore Y = \frac{1 + jQ\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}{R}$

$$\boxed{Z = \frac{R}{1 + jQ\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}}$$

Voltage gain:-

$A_v = \frac{V_o}{V_{in}}$.

$V_o = -g_m V_{b'e} Z$.

$V_{b'e} = V_i \cdot \frac{r_{b'e}}{r_{b'e} + r_{bb'}}$

$V_o = \frac{-g_m V_i r_{b'e} Z}{r_{b'e} + r_{bb'}}$

$\frac{V_o}{V_i} = A_v = \frac{-g_m r_{b'e} Z}{r_{bb'} + r_{b'e}}$.

(13)

$$= \frac{-g_m r_{b'e}}{r_{bb'} + r_{b'e}} \cdot \frac{R}{1+jQ\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

sub Z

$$A_v = \frac{-g_m R}{1+jQ\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

gain is maximum when $\omega = \omega_0$

$$|A_v| = g_m R.$$

At 3dB,

$$|A_v| = \frac{g_m R}{\sqrt{2}}$$

$$\frac{g_m R}{\left|1+jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right|} = \frac{g_m R}{\sqrt{2}}$$

$$\left|1+jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right| = \sqrt{2}$$

$$\sqrt{1+Q^2\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]^2} = \sqrt{2}$$

squaring on both sides,

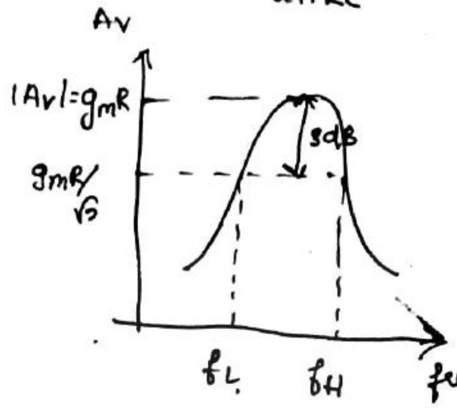
$$1+Q^2\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]^2 = 2$$

By solving we get,

$$BW = f_H - f_L$$

$$= \frac{\omega_0}{2\pi Q}$$

$$= \frac{1}{2\pi RC}$$



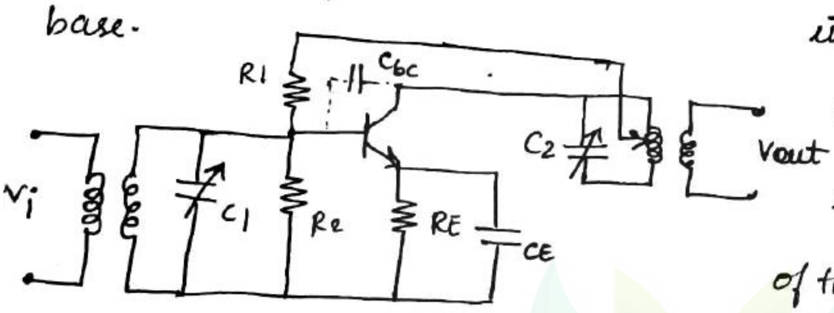
NEUTRALIZATION:-

→ In tuned RF amplifiers, transistors are used at the frequencies nearer to their unity gain bandwidths to amplify a narrow band of high frequencies.

→ At the center frequency, the inter junction capacitance between base and collector C_{bc} of the transistor becomes dominant.

→ Using CE configuration capacitance C_{bc} comes across input and output circuits of an amplifier.

→ As the reactance of Cbc at RF is low enough it provides the feedback path from collector-to-base.



→ If this feedback is positive with proper phase shift, then it is possible that circuit becomes unstable generating its own oscillations and stops working as amplifier.

→ To prevent these oscillations the stage gain of the RF amplifier has to be reduced to a level that ensures circuit stability.

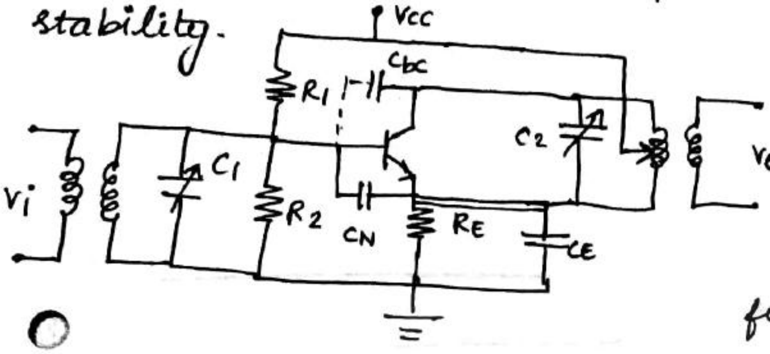
→ Q-factor can be reduced but selectivity will also be reduced.

→ Professor L.A. Hazeltine introduced a circuit in which the troublesome effect of the collector to base capacitance of the transistor was neutralized, by sending a signal which cancels the signal coupled from collector to base.

→ Thus neutralization can be achieved by feeding back, a portion of the output signal to the input in such a way that it has the same amplitude as the unwanted feedback but opposite in phase.

*Hazeltine Neutralization (Broadband Neutralization)

→ This method is employed in tuned RF amplifier to maintain stability.



→ The undesirable effect of the collector to base capacitance of the transistor is neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance.

→ A small value of variable capacitance C_N is connected from bottom of the output coil to the base of transistor

→ If internal capacitance C_{bc} feeds signal from top end of coil to the transistor base, C_N feeds a signal of equal magnitude but opposite polarity from the bottom of coil to the base.

→ The neutralizing capacitor C_N can be adjusted correctly to fully cancel the signal fed through C_{bc}.

→ Thus by adjusting C_N exact neutralization is achieved.

*Narrowband / Neutrodyne Neutralization Technique

→ In this method an additional coil is mounted at right angles to the coupled windings.

→ If the windings are properly polarized, ~~across~~. the voltage across L due to the circulating ~~circuit~~ current.

in the base circuit will have proper phase to cancel the signal coupled through C_{bc}.

POWER AMPLIFIER:-

→ Power Amplifier is an amplifier, which is capable of providing large amount of power to the load.

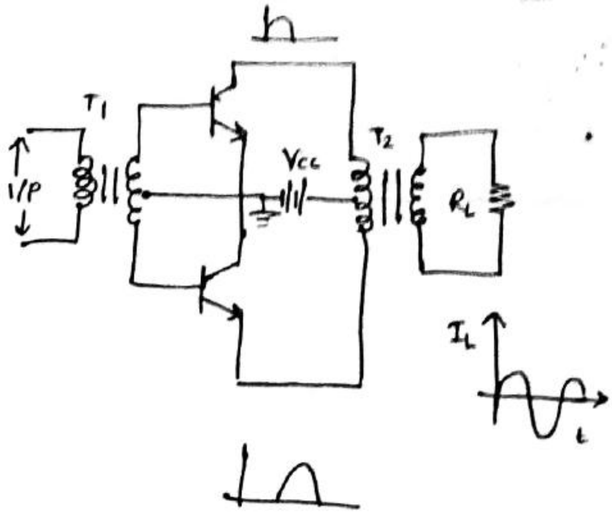
→ Power Amplifier can be classified as,

* Class A Amplifiers
* Class B Amplifiers
* Class C Amplifiers.

* class B Amplifier:-

→ class B amplifier conduct only for 180° or half of the input signal.

→ This condition is achieved by setting the Q-point at cut-off region.



class B push pull power Amplifier

→ Two centre tapped transformers T_1 and T_2 and two identical transistors Q_1 and Q_2 are used.

→ T_1 is the input transformer and is also called as phase splitter.

→ This produces two signal voltages which are 180° out-of-phase with each other.

→ These two signal voltages with opposite polarity drive the transistors Q_1 & Q_2. T_2 is the output transformer that couples ac output to load.

Operation:-

→ The transistors Q_1 and Q_2 are biased at cut-off. This is achieved by connecting emitter and base terminals together.

→ When there is no input signal Q_1 and Q_2 are in cut-off, hence no current is drawn from Vcc supply and there is no power dissipation.

→ During positive half-cycle, base of Q_1 becomes positive making Q_1 to operate as amplifier. Base of Q_2 is negative & Q_2 remains off.

→ During negative-half-cycle base of Q_2 becomes positive and Q_2 operates as amplifier. Q_1 remains OFF.

Power Relations:-

The DC input power applied to the circuit,

$$P_{dc} = I_{dc} \cdot V_{cc}$$

W.K.T,

$$I_{dc} = \frac{I_m}{\pi}, \text{ for halfwave sine signal,}$$

$$P_{dc}(in) = \frac{V_{cc} \cdot I_m}{\pi} \text{ (per transistor).}$$

$$P_{dc}(in) = \frac{2 V_{cc} \cdot I_m}{\pi} \text{ [considering both].}$$

The AC output power obtained across load is given as,

$$P_{ac}(out) = V_{rms} I_{rms}$$

$$= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$$

The overall efficiency,

$$\eta = \frac{P_{out}}{P_{in}} \times 100$$

$$= \frac{\frac{V_m I_m}{2}}{\frac{2 V_{cc} I_m}{\pi}} \times 100$$

$V_m = V_{CC}$

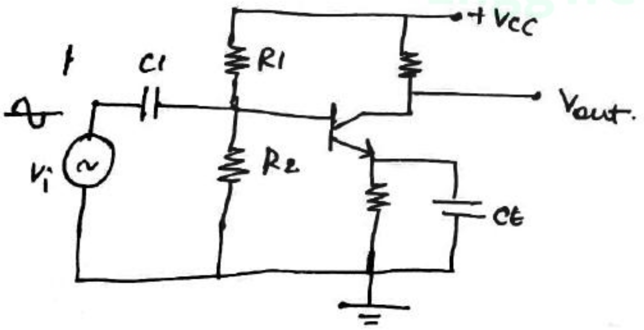
$\therefore \ \% \eta = \frac{\pi}{4} \times 100$

$\boxed{\text{Effeciency} = 78.5\%}$

Class A amplifier :-

→ The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

→ Q point in this case is approximately the mid-point of the load line.

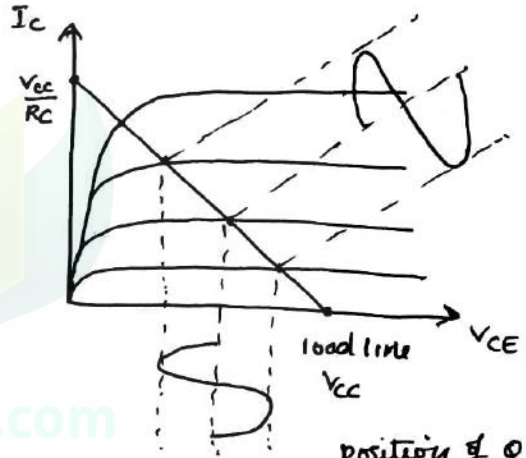


→ For all values of input signal the transistor remains in the active region.

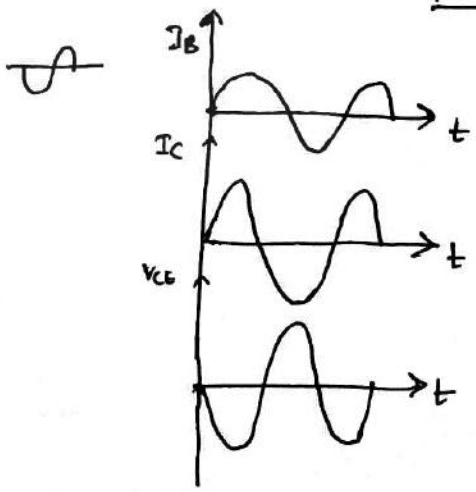
→ Collector voltage varies w.r.t the a.c input signal for the full cycle (360°).

→ Class A amplifiers reproduces the output faithfully and without distortion.

→ But the Effeciency is very small.



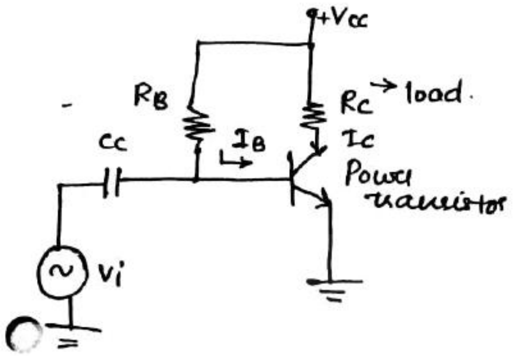
position of Q-point



current & voltage waveform

(a) SERIES FED CLASS-A AMPLIFIER:-

→ A simple series fed class-A Amplifier is shown as below.



→ The only difference between this circuit and the small signal version is that the signals handled by the large signal circuit is in the range of volts and the transistor that used is a power transistor.

→ This transistor is capable of operating in the range of a few tens of watts.

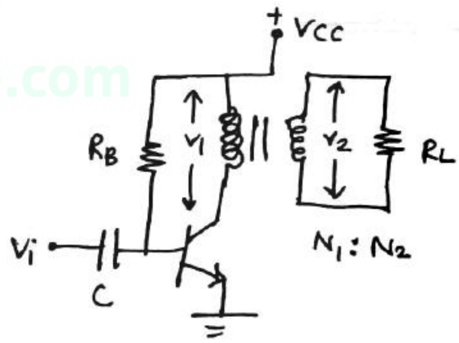
→ This circuit has poor power effeciency.

→ The β of power transistor is generally less than 100.

(b) Transformer coupled class A Amplifier.

→ In this type of class A Amplifier to set up or step down voltage and current a transformer is used.

→ This form of class A amplifier having maximum effeciency of 50% uses a transformer to couple the output signal to the load.



Power gain:-

→ It is the ratio of the power delivered to the load to the input power.

Power gain $\boxed{A_p = \frac{P_L}{P_{in}}}$

For ac power the voltage is expressed as rms,

$$P_L = \frac{V_L^2}{R_L}, \quad P_{in} = \frac{V_{in}^2}{R_{in}}$$

$$\therefore A_P = \frac{\frac{V_L^2}{R_L}}{\frac{V_{in}^2}{R_{in}}} = \frac{V_L^2}{V_{in}^2}\left(\frac{R_{in}}{R_L}\right)$$

W.K.T,

$$\frac{V_L}{V_{in}} = A_V \rightarrow \text{voltage gain}$$

$$\boxed{A_P = A_V^2 \frac{R_{in}}{R_L}}$$

Dc Quiscent power:-

$$P_{DQ} = I_{CQ} V_{CEQ}$$

→ It is the product of Q point current and voltage.

→ This is the maximum power a class A Amplifier must handle.

Output Power:-

→ It is the product of rms load current & the rms load voltage.

Maximum peak voltage,

$$V_{cmax} = I_{CQ} R_C$$

V_{cmax} is $0.707 V_{cmax}$.

Maximum peak current,

$$I_{cmax} = \frac{V_{CEQ}}{R_C}$$

I_{cmax} is $0.707 I_{cmax}$

$$\therefore P_{outmax} = (0.707 I_c)(0.707 V_c)$$

$$\boxed{P_{outmax} = 0.5 I_{CQ} V_{CEQ}}$$

Effeciency:-

→ It is the ratio of power delivered to the load to the power from dc supply.

$$P_{DC} = I_{CC} V_{CC} = 2 I_{CQ} V_{CEQ}$$

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{0.5 I_{CQ} V_{CEQ}}{2 I_{CQ} V_{CEQ}} = 0.25$$

* CLASS C AMPLIFIER :-

→ In class C amplifier conduction occurs for much

SYLLABUS 1) voltage, current series feedback Amp 2) voltage, current shunt
1) Oscillators x phase shift, x wein x Hartley x colpits x crystal

Unit-V Feedback Amplifiers & oscillators

Feedback Amplifier

Feedback plays an important role in almost all electronic circuits. It is almost invariably used in the Amplifier to improve its performance and to make it more Ideal.

What is feedback?

When a part of the output signal is fed to the input of the circuit then it is referred to as feedback. This feedback parameters may be voltage or current.

Feedback Amplifier

A part of output is sampled and feedback to the input of the Amplifier is called feedback Amplifier.

Types of feedback: (Theory)

(i) positive feedback (Regenerative or direct feedback)

When input signal and part of output signal are in phase, the feedback is called positive feedback amplifier.

(ii) Negative feedback (degenerative or inverse).

When input signal and part of the output signal are in out of phase, the feedback is called Negative feedback.

Note: positive feedback results in oscillations and hence not used in Amplifiers.

Negative feedback gain (A_f)

If the feedback signal V_f is out of phase with input signal V_s then $V_i = V_s - V_f$ so the input voltage applied to the basic Amplifier is decreased, so the output is decreased, Hence the voltage gain is reduced.

$$\text{gain } A_f = \frac{V_o}{V_s} = \frac{V_o}{V_i + V_f}$$

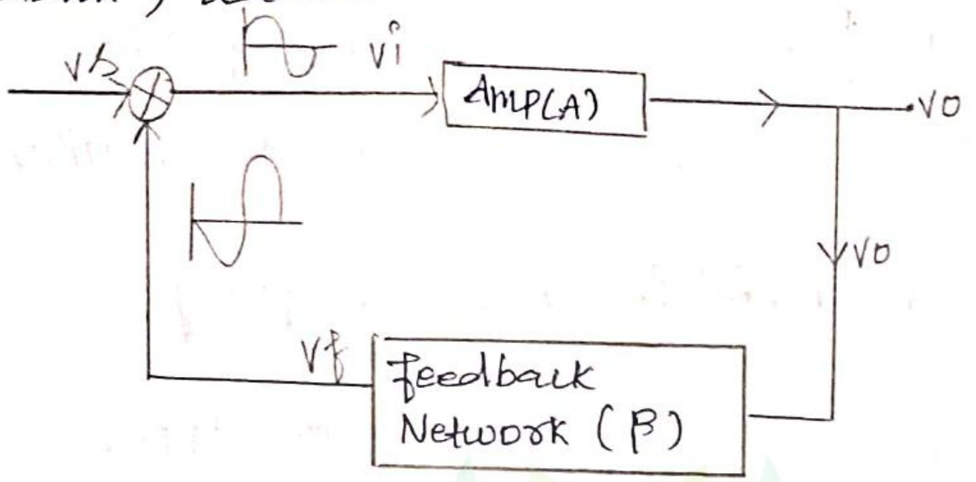
$\div V_o$

$$A_f = \frac{V_o/V_o}{V_i/V_o + \frac{V_f}{V_o}} = \frac{1}{\frac{1}{A} + \beta} = \frac{1}{\frac{1 + A\beta}{A}}$$

$$= \frac{A}{1 + A\beta} \qquad \boxed{A_f = \frac{A}{1 + A\beta}} \qquad |A_f| < |A|$$

If $|A\beta| \gg 1$ $\quad A_f \simeq 1/\beta$ gain is stable.

Negative feedback is used to improve the performance of electronic Amplifier. Negative Feedback always helps to increase the band width, decrease distortion and Noise. (3)



Effects of Negative feedback

(i) stabilisation of gain

The gain $A_f = \frac{A}{1+A\beta}$ —(1)

Differentiating w.r to A, we get.

$$\frac{dA_f}{dA} = \frac{dA}{(1-A\beta)^2} = \frac{1}{(1+A\beta)}\frac{1}{(1+A\beta)}$$

Divide A_f on both sides

$$\frac{dA_f}{A_f} = \frac{dA}{(1+A\beta)^2} \cdot \frac{1}{A_f} = \frac{dA}{(1+\cancel{A\beta})^2} \cdot \frac{\cancel{1+A\beta}}{A}$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{1+A\beta} \qquad \boxed{\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{1}{1+A\beta}}$$

$\frac{dA_f}{A_f}$ = fractional change in amplifier voltage gain.

$\frac{dA}{A}$ = fractional change in voltage gain without feedback.

The term $\boxed{\frac{1}{1+A\beta}}$ is called sensitivity The Reciprocal of sensitivity is called desensitivity.

(2) Increase in bandwidth (cutoff frequency).

Bandwidth is the difference between the upper cut off frequency (f_1) and lower cutoff frequency (f_1)

The product of voltage gain and the bandwidth of an amplifier without feedback and with feedback remains the same.

$$\boxed{A_f \times BW_f = A \times BW}$$

As the voltage gain of a feedback amplifier reduces by the factor $\frac{1}{1+A\beta}$ is bandwidth would be increased by $1+A\beta$ (i.e) $Bw_f = BW(1+A\beta)$

Due to Negative feedback

Upper cut off frequency f_{of} is increased by the factor $(1+A\beta)$ and lower cut off frequency

f_{1f} is decreased by the factor $(1+A\beta)$. The upper and lower 3db frequency with negative feedback given by (5)

$$\boxed{f_{2f} = f_2(1+A\beta) \quad f_{1f} = \frac{f_1}{1+A\beta}}$$

(3) Decreased Distortion

Let open loop voltage gain A Total harmonic distortion D feedback ratio, β The distortion will reduce to $\boxed{D_f = \frac{D}{1+A\beta}}$

(4) Decreased Noise.

There are many sources of Noise in an amplifier depending upon the active device used. Noise N can be reduced by a factor of $\frac{1}{1+A\beta}$ in a similar manner to non-linear distortion noise with the Negative feedback $\boxed{N_D = \frac{N}{1+A\beta}}$

(5) Increase in Input Impedance.

As amplifier should have high input impedance so that it will not load the procedure stage or the input voltage sources. This can be acheived with the help of Negative series voltage feedback

$$\boxed{Z_{if} = Z_i (1+A\beta)}$$

Input impedance is increased by a factor $(1+A\beta)$

⑥ Decrease in output impedance.

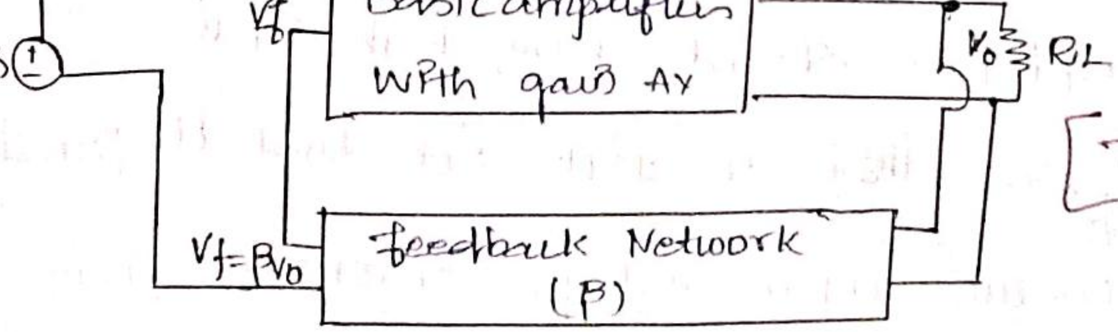
An Amplifier with low output impedance is capable of delivering power to the load without much loss. This can acheived by employing negative series voltage feedback in an Amplifier

$$\boxed{Z_{of} = \frac{Z_o}{1+A\beta}}$$

output impedance is reduced by a factor $(1+A\beta)$.

1) Voltage Series feedback

This series connection increases the input resistance and voltage feedback tends to decrease the output resistance of the Amplifier



[TOPOLOGY]

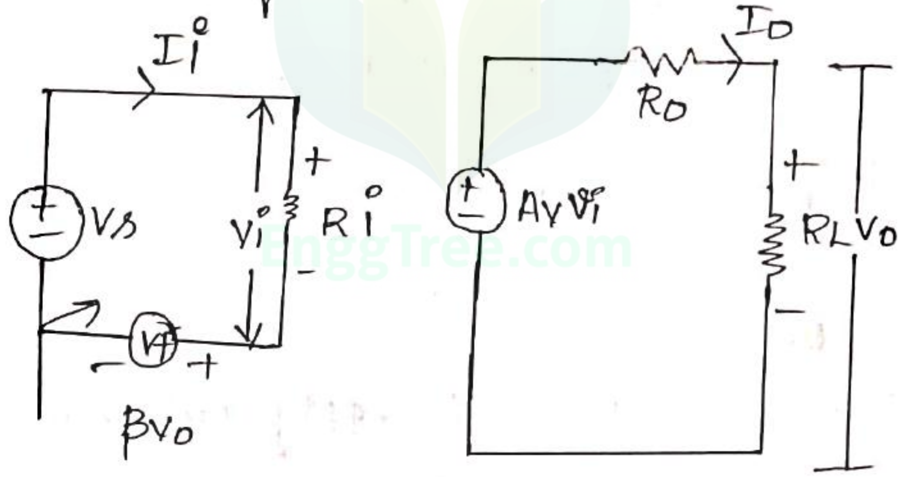
The input of the feedback Network is in parallel with the output of the Amplifier. A fraction of the output voltage through the feedback amplifier Network is applied in series with input voltage of the amplifier. Thus feedback is otherwise called True feedback amplifier

$$\boxed{\beta = \frac{V_f}{V_o}}$$

To derive input and output resistance [R_{if} & R_{of}].

Consider the Equivalent circuit (Thevinins)

Step :1



[EQUIVALENT CIRCUIT]

$R_{if} = \frac{V_s}{I_1}$

Step 2: obtain Expression for Vs.

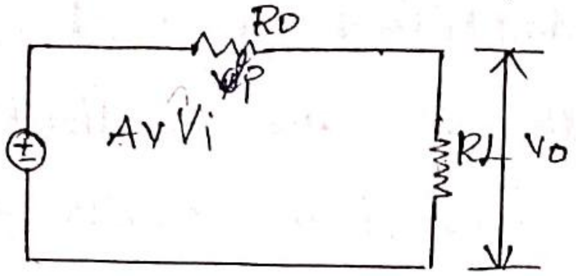
Apply KVL in input side.

$$V_s - I_i R_i - V_f = 0 \qquad \therefore (V_f = \beta V_o)$$

$$V_s = I_i R_i + V_f$$

$$V_s = I_i R_i + \beta V_o$$

Step 3: obtain Vo using voltage division



$$V_o = A_v v_i \frac{R_L}{R_L + R_o}$$

$$V_o = A_v v_i$$

But $v_i = I_i R_i$

Step 4: obtain R_{if}

Substitute (V_o) in (V_s)

$$V_s = I_i R_i + A_v v_i$$

$$V_s = I_i R_i + A_v I_i R_i \beta$$

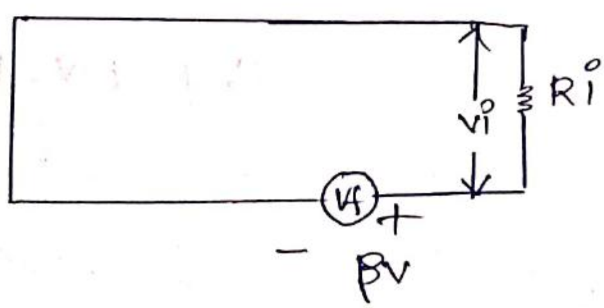
$$V_s = I_i (R_i + A_v R_i \beta)$$

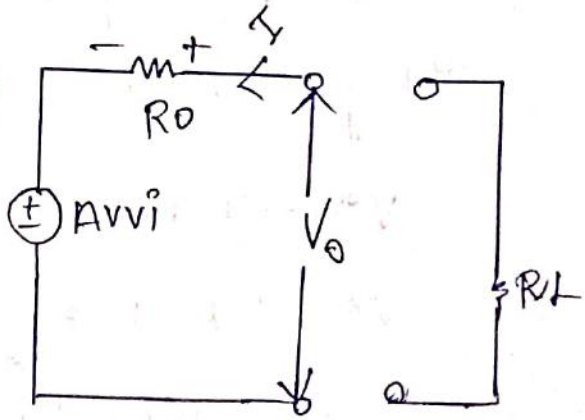
$$\frac{V_s}{I_i} = R_{if} = R_i(1+\beta A_v)$$

$$\boxed{R_{if} = R_i(1+\beta A_v)}$$

To derive R_{of}

→ Remove R_L and apply external voltage V & get I at that time short circuit the source voltage.





Applying KVL on output side.

$A_V v_i + I R_0 - V_0 = 0 \Rightarrow A_V v_i + I R_0 = V_0$

We know that $v_i = -v_f = -\beta V_0$

$$-A_V \beta V_0 + I R_0 = V_0$$

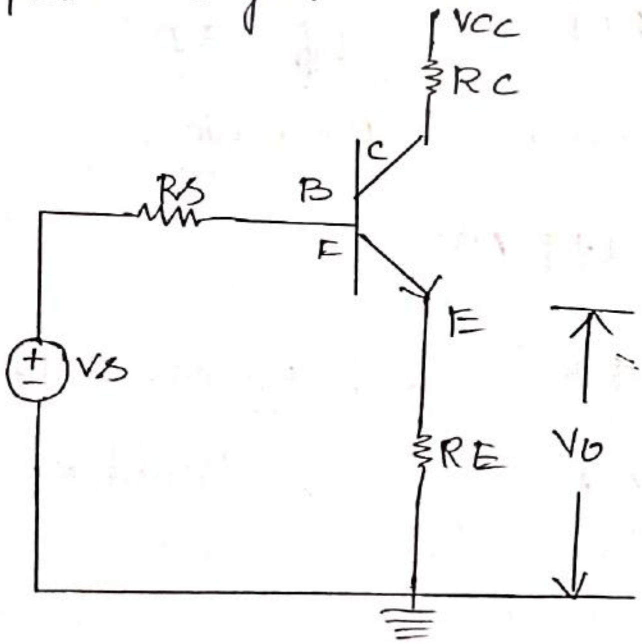
$$I R_0 = V_0 + A_V \beta V_0 = V_0(1+\beta A_V)$$

$$R_{of} = \frac{V_0}{I} = \frac{R_0}{1+\beta A_V}$$

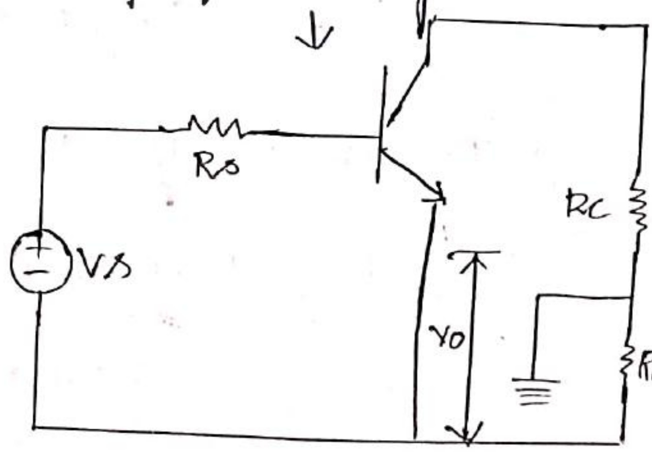
$$\boxed{R_{of} = \frac{R_0}{1+\beta A_V}}$$

Voltage series feedback Amplifier [Example].

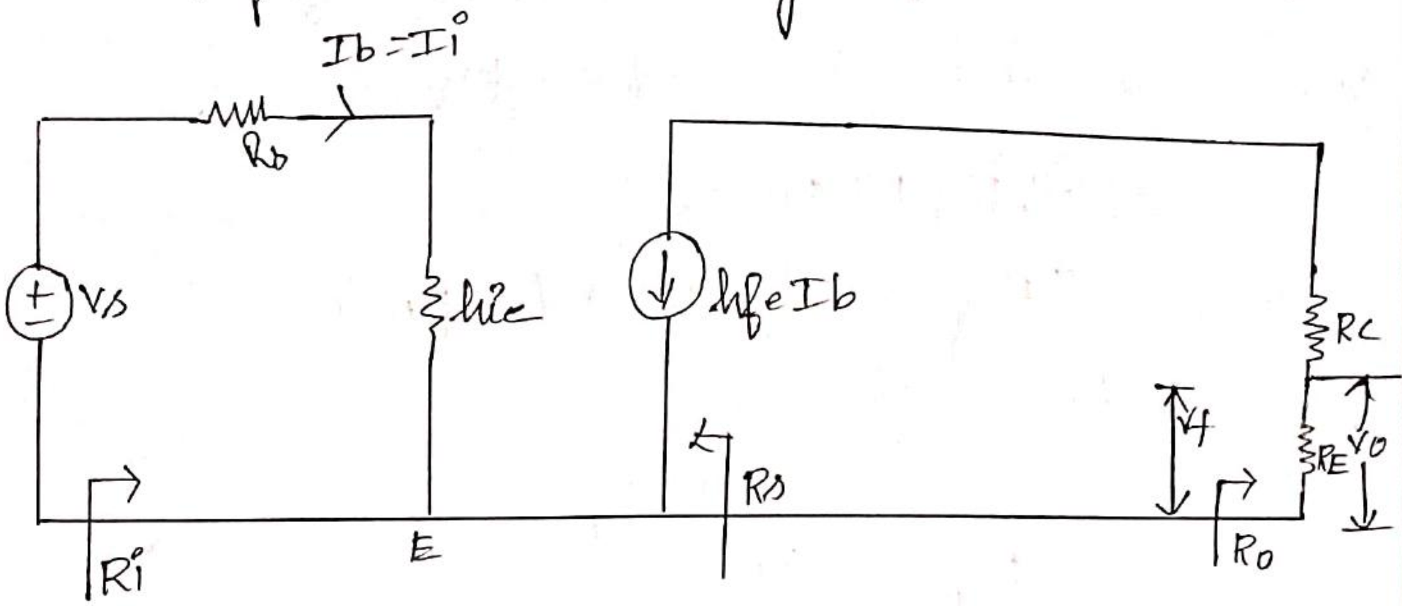
Emmitter follower is the Example for voltage series feedback Amplifier. The feedback signal is the voltage V_f across R_E and the sampled signal is V_0 across R_E



Simplified diagram



Equivalent circuit Diagram.



1.) β = feedback factor $= \dfrac{V_f}{V_o} = 1$

2.) Voltage gain $A_V = \dfrac{V_o}{V_s} = \dfrac{h_{fe} I_b R_E}{V_s}$

To derive Vs

Apply KVL to input side $V_s - I_b R_s - I_b h_{ie} = 0$

$$V_s = I_b (R_s + h_{ie})$$

$$A_V = \frac{h_{fe} \cancel{I_b} R_E}{\cancel{I_b}(R_s + h_{ie})} = \frac{h_{fe} R_E}{(R_s + h_{ie})}$$

3.) Desensitivity $D = 1 + \beta A_V$

$$D = 1 + \frac{h_{fe} R_E}{(R_s + h_{ie})} \Rightarrow \frac{R_s + h_{ie} + h_{fe} R_E}{R_s + h_{ie}}$$

4.) $A_{vf} = \frac{A_v}{D} = \frac{h_{fe}R_E}{\cancel{R_s+h_{ie}}} \times \frac{\cancel{R_s+h_{ie}}}{R_s+h_{ie}+h_{fe}R_E}$

$$A_{vf} = \frac{h_{fe}R_E}{R_s+h_{ie}+h_{fe}R_E}$$

$$h_{fe}R_E \gg R_s+h_{ie}$$

$$A_{vf} = \frac{h_{fe}R_E}{h_{fe}R_E} \simeq 1$$

5.) Input Resistance $R_i = R_s+h_{ie}$

6.) $R_{if} = R_i \times D = (\cancel{R_s+h_{ie}}) \times \frac{R_s+h_{ie}+h_{fe}R_E}{(\cancel{R_s+h_{ie}})}$

$$\boxed{R_{if} = R_s+h_{ie}+h_{fe}R_E}$$

7.) $\boxed{R_o = \infty}$

8.) $R_{of} = \frac{\alpha}{1+\beta A_v} = \frac{\infty}{\infty} = \infty$ (without considering R_L)

9.) Output Resistance with feedback and considering $R_L = R_E$

$$R_{ef} = \underset{R_L\to\infty}{Lt} \quad R_{ef} = \underset{R_E\to\infty}{Lt} \frac{R_E(R_s+h_{ie})}{R_s+h_{ie}+h_{fe}R_E}$$

$$R_{ef} = \frac{1\,(R_s+h_{ie})}{0\,(R_s+h_{ie}+h_{fe}/0)}$$

$$R_{of} = \frac{R_s + h_{ie}}{h_{fe}}$$

Anna University Questions: [PROBLEM ON VOLTAGE SERIES]

1) In the BJT Emitter follower circuit, the circuit component values are $R_s = 600\Omega$, $R_C = 4.7k\Omega$, $R_E = 2k\Omega$, $h_{fe} = 80$, $h_{ie} = 5k\Omega$ calculate A_{vf}, R_{if}, R_{of} and R_{of}'

Solution: It is given that emitter follower circuit that is voltage series feedback amplifier

$$A_v = \frac{h_{fe} R_E}{R_s + h_{ie}} = \frac{80 \times 2 \times 10^3}{(600 + 5 \times 10^3)} = 28.57.$$

$A_v \rightarrow$ voltage gain without feedback.

Desensitivity $D = 1 + A_v \beta \quad (\beta = 1)$

$$D = 1 + 28.57 \times 1 = 29.57$$

i) $$A_{vf} = \frac{A_v}{D} = \frac{28.57}{29.57} = 0.966 \simeq 1$$

Where $A_{vf} \rightarrow$ voltage gain with feedback.

Input Resistance without Resistance feedback

ii) $R_i = R_s + h_{ie}$

$= 600 + 5\times10^3$

$\boxed{R_i = 5.6K\Omega}$.

Input Resistance with feedback.

$R_{if} = R_i \times D$

$= 5.6\times10^3 \times 29.57$

$\boxed{R_{if} = 165.592K\Omega}$.

output Resistance without feedback and not considering external load Resistance ($R_L = R$)

$R_o = \infty$

iii) $R_{of} = \frac{R_o}{D} = \frac{1}{0\times29.57} = \frac{1}{0} = \infty$

This indetermining can be resolved by first finding R'_{of} and then apply $R_L \to \infty$

output resistance with feedback and considering (R_L)

not given

iv) $R'_{of} = \frac{R'_o}{D} = \frac{R_L}{D} = \frac{R_E}{D} = \frac{2\times10^3}{29.57} = 67.64\Omega$.

$R_{of} = \lim_{R_L\to\infty} R'_{of} = \frac{R_s + h_{ie}}{h_{fe}} = \frac{600 + 5\times10^3}{80}$

$\boxed{R'_{of} = 70\Omega}$

Current Series feedback.

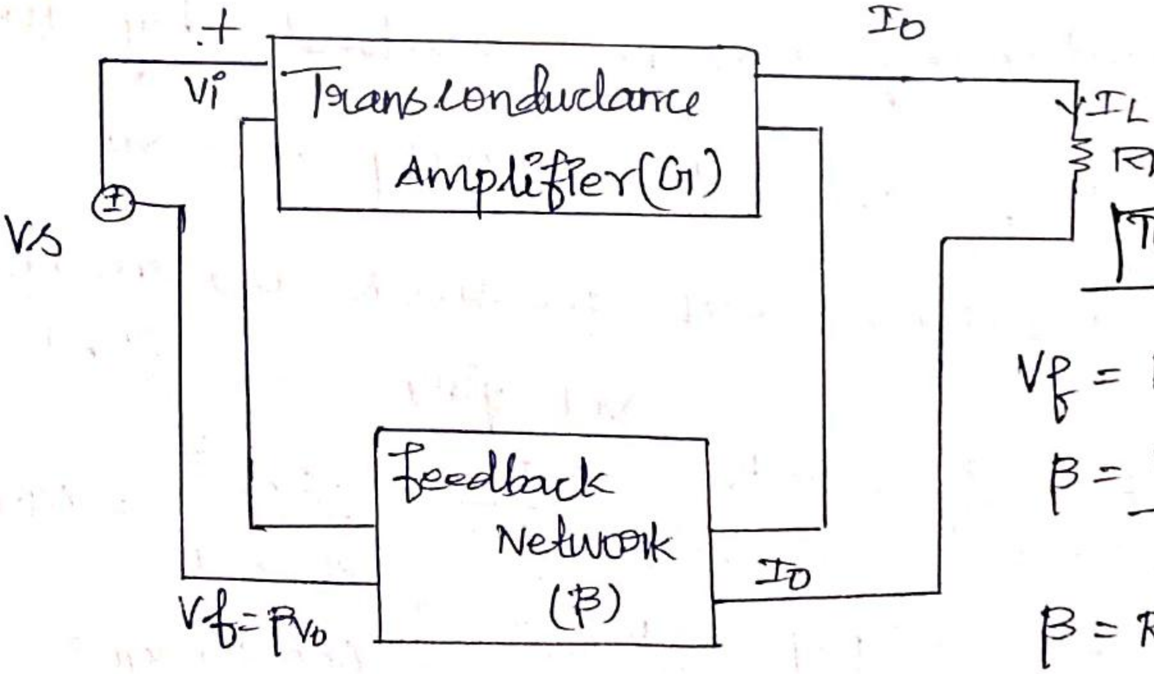
→ A voltage is developed which is proportional to the output current $V_f \propto V_o$

→ This is called current feedback even though it is a voltage that subtracts from the input voltage.

→ Because of the series connection as the input and output, the input and output resistance get increased

→ This type of amplifier is called transconductance amplifier it is denoted by

$$\boxed{\beta = \frac{V_f}{I_o}}$$



TOPOLOGY.

$V_f = \beta I_o$

$\beta = \frac{V_f}{I_o}$

$\beta = R = \frac{1}{G}$

15

→ One of the most common method of applying the current series feedback is to place a resistor R_E between the Emitter load of a CE amplifier and ground.

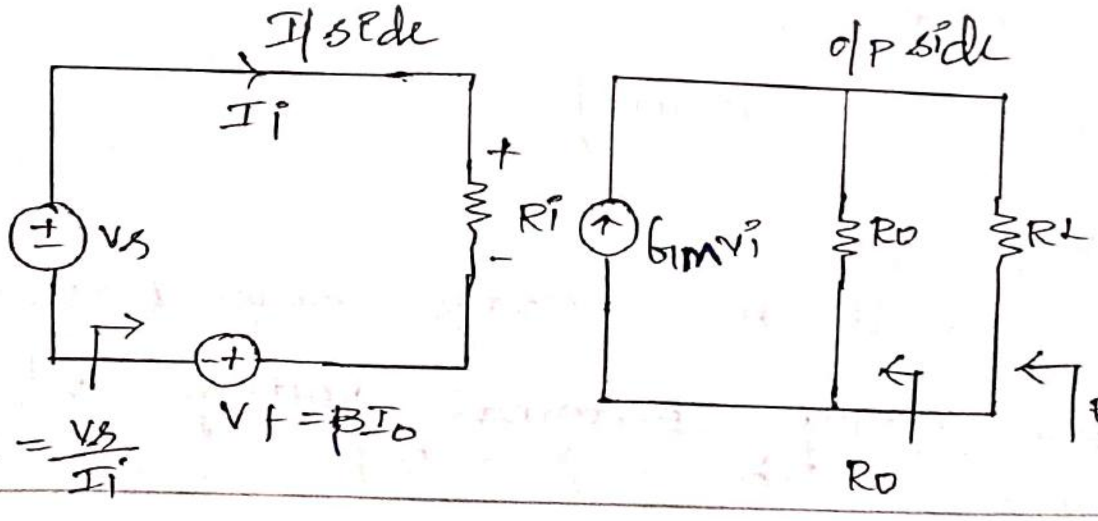
As the CE amplifier has a high gain this is most often used with series negative feedback so that it can afford to lose some gain.

To derive input and output Resistance [R_{if} & R_{of}]

In current series feedback topology amplifier input circuit is represented by Thevenin's Equivalent circuit and output circuit by Norton's equivalent circuit is derived.

To derive (k_1, k')

Step : 1 Draw the equivalent circuit (Thevinin's)



$G_m V_i = I$

$\frac{1}{R} V_i = I$

$R_{if} = \frac{V_S}{I_i}$

Step 2: Obtain Expression of V_s

Apply KVL at input side

$$V_s - I_i R_i - V_f = 0$$

Substitute V_f

$$V_s - I_i R_i - \beta I_o = 0$$

$$V_s = I_i R_i + \beta I_o$$

Step 3: Obtain Expression for I_o consider o/p side apply current division rule

$$I_o = G_M V_i \frac{R_o}{R_o + R_L} = G_M V_i$$

Where $\boxed{G_M = \frac{G_M R_o}{R_o + R_L}}$

Step 4: Sub I_o in V_s.

$$V_s = I_i R_i + \beta G_M V_i = I_i R_i + \beta G_M I_i R_i$$

$$V_s = I_i R_i (1 + \beta G_M)$$

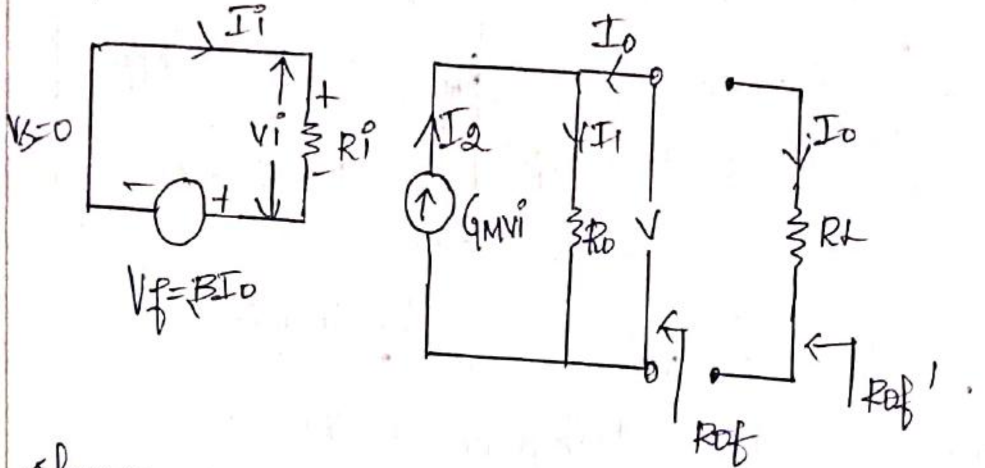
$$\frac{V_s}{I_i} = \boxed{R_{if} = R_i (1 + \beta G_M)}$$

To derive R_{of}:

→ Short circuit the voltage source (i.e) $V_s = 0$

Remove R_L apply External voltage 'V' find I, so $= \frac{V}{I} = R_{of}$.

Step 1: Draw the equivalent circuit



Step 2: domie I in the output side

$$I = \frac{V}{R_o} - G_M v_i$$

from input side $v_i = -V_f = -\beta I_o = \beta I \; (I_o = -I)$

Substitute in I

$$I_o = \frac{V}{R_o} - G_M \beta I_o$$

$$\frac{V}{R_o} = I_o + G_M \beta I_o = I_o = (1+G_M\beta)$$

$$\frac{V}{I_o} = R_o(1+G_M\beta)$$

Step 3: Obtain $R_{of} = \frac{V}{I_o} = R_o(1+G_M\beta)$

Step 4: $R'_{of} = R_{of} \parallel R_L = \frac{R_{of} \cdot R_L}{R_{of}+R_L}$

Sub R_{of} $\quad R'_{of} = \frac{R_o(1+G_M\beta)R_L}{R_o(1+G_M\beta)+R_L}$

$$\boxed{R'_{of} = \frac{R_o R_L (1+G_M\beta)}{R_o+R_L + R_o G_M \beta}}$$

Now ÷ by R_o+R_L

$$R'_{of} = \frac{\frac{R_o R_L}{R_o + R_L}(1+G_{IM}\beta)}{\frac{\cancel{R_o + R_L}}{\cancel{R_o + R_L}} + \frac{R_o G_{IM}\beta}{R_o + R_L}}$$

$\frac{R_o R_L}{R_o + R_L} \rightarrow R_o$

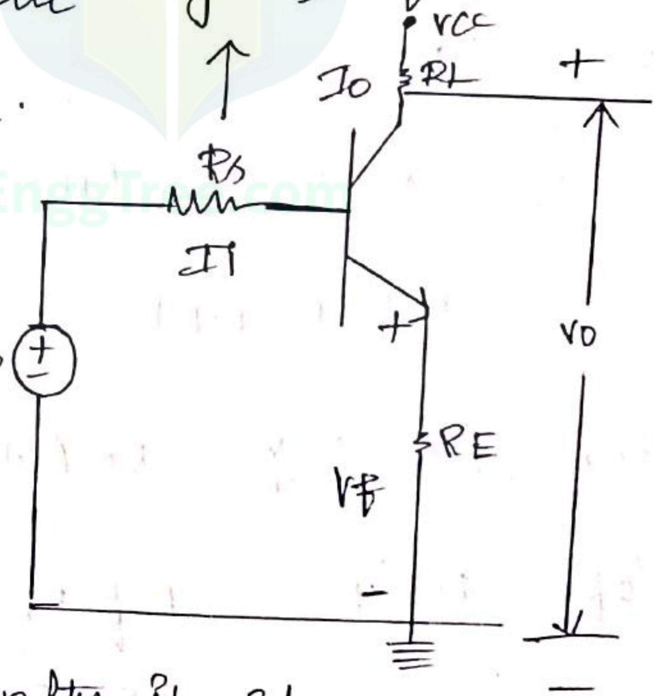
$$\boxed{R_{of} = \frac{R_o'(1+G_{IM}\beta)}{1+\beta G_{IM}}}$$

Example for current series feedback.

→ CE amplifier with unbypassed R_E.

→ sampled signal is I_o and feedback signal is V_f.

Step 1: Identify the feedback topology set $I_o = 0$ (open circuit o/p signal) $V_f = 0$ so this is current feedback.



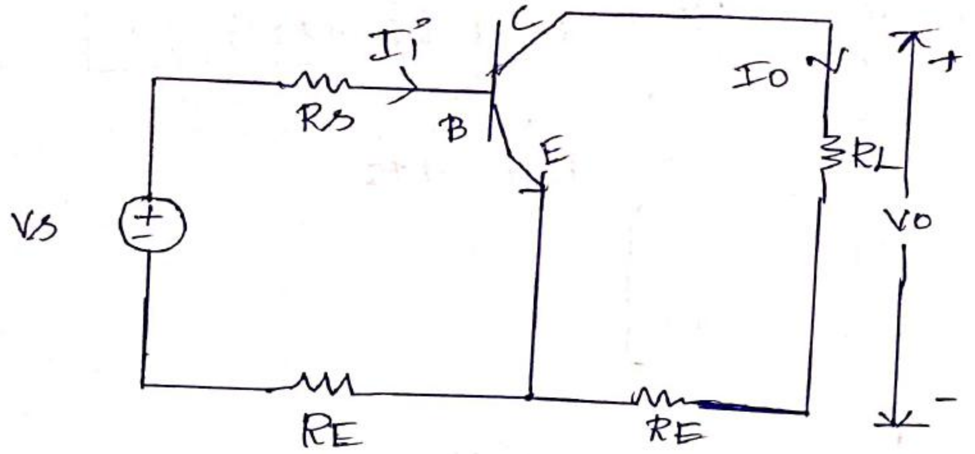
Step 2: Draw the simplified diagram.

for i/p side → open circuit the o/p side

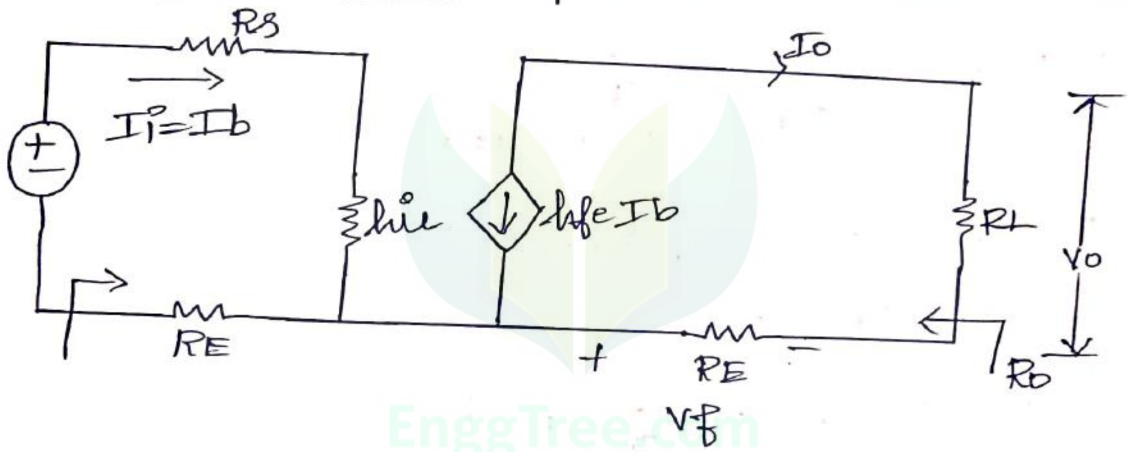
$I_o = 0$ RE appears on the i/p side.

For o/p side → open circuit the i/p side $I_i = 0$ RE appears on output side.

After draw the Diagram.



Step3: Draw the H-parameter Model circuit



Step4: calculate β

$$\beta = \frac{V_f}{I_o} = -\frac{\cancel{I_o} R_E}{\cancel{I_o}} = -R_E$$

Step5: open loop Transfer gain GM

$$G_M = \frac{I_o}{V_i} = \frac{V_o}{V_i = V_s} - h_{fe} I_b$$

$$G_M = \frac{-h_{fe} I_b}{V_s}$$

Consider input side

$$\boxed{I_b (R_s + h_{ie} + R_E) = V_s}$$

$$\frac{I_b}{V_s} = \frac{1}{R_s + h_{ie} + R_E}$$

$$\therefore \boxed{G_{IM} = \frac{-h_{fe}}{R_s + h_{ie} + R_E}}$$

Step 6: Calculate D, G_{Mf}, R_{if}, R_{of}, R'_{of}, A_{vf}.

$$D = 1 + \beta G_{IM} = 1 + \frac{h_{fe} R_E}{R_s + h_{ie} + R_E}$$

$$D = \frac{R_s + h_{ie} + R_E + h_{fe} R_E}{R_s + h_{ie} + R_E}$$

$$\boxed{D = \frac{R_s + h_{ie} + (1 + h_{fe}) R_E}{R_s + h_{ie} + R_E}}$$

(1) $$G_{Mf} = \frac{G_{IM}}{D} = \frac{-h_{fe}}{\cancel{R_s + h_{ie} + R_E}} \times \frac{\cancel{R_s + h_{ie} + R_E}}{R_s + h_{ie} + (1 + h_{fe}) R_E}$$

$$G_{Mf} = \frac{-h_{fe}}{R_s + h_{ie} + (1 + h_{fe}) R_E}$$

If $(1 + h_{fe}) R_E >> R_s + h_{ie}$ $\quad (1 + h_{fe} = h_{fe})$

$$G_{mf} = \frac{-h_{fe}}{(1+h_{fe})R_E} \simeq \frac{-1}{R_E} \simeq \frac{1}{\beta}$$

2) Voltage gain with feedback amplifier

$$A_{vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s} = G_{mf} R_L$$

$$A_{vf} = \frac{-h_{fe} R_L}{R_s + h_{ie} + (1+h_{fe})R_E}$$

3) Input Resistance without feedback

$$\boxed{R_i = R_s + h_{ie} + R_E}$$

4) Input Resistance with feedback

$$R_{if} = R_i D$$

$$= \cancel{(R_s + h_{ie} + R_E)} \times \frac{R_s + h_{ie} + (1+h_{fe})R_E}{\cancel{R_s + h_{ie} + R_E}}$$

$$\boxed{R_{if} = R_s + h_{ie} + (1+h_{fe})R_E}$$

5) output Resistance without feedback

$$R_o = \infty$$

$$R_{of} = R_o(1+\beta G_M) = \infty$$

$$R'_{of} = R_{of} \parallel R_L = R_L.$$

PROBLEM ON CURRENT SERIES FEEDBACK

Problem: For current series feedback amplifier

$R_E = 1.2K\Omega$, $R_s = 1K\Omega$, $R_L = 2.2K\Omega$, $h_{ie} = 1.1K\Omega$.

hfe = 50 , Determine Gmp , Avf , Rif , Rof , R'of ,

Solution:

$\beta = -R_E - \boxed{-1.2\times10^{3}}$

$G_m = \frac{-h_{fe}}{R_s + h_{ie} + R_E} = \frac{-50}{1\times10^{3} + 1.1\times10^{3} + 1.2\times10^{3}}$

$\boxed{G_m = -0.015}$

$D = 1 + \beta G_M = 1 + (-1.2\times10^{3})(-0.015)$

$\boxed{D = 19}$

$G_{mf} = \frac{G_M}{D} = \frac{-0.015}{19} = -7.89\times10^{-4}$

$A_{vf} = G_{mf} R_L = -7.89\times10^{-4} \times 2.2\times10^{3}$
$= -1.7368.$

$R_i = R_s + h_{ie} + R_E$
$= 1\times10^{3} + 1.1\times10^{3} + 1.2\times10^{3}$

$R_i = 3.3\times10^{3}\ \Omega$

$R_{if} = R_i \times D = 3.3\times10^{3} \times 19 = 62.7K\Omega.$

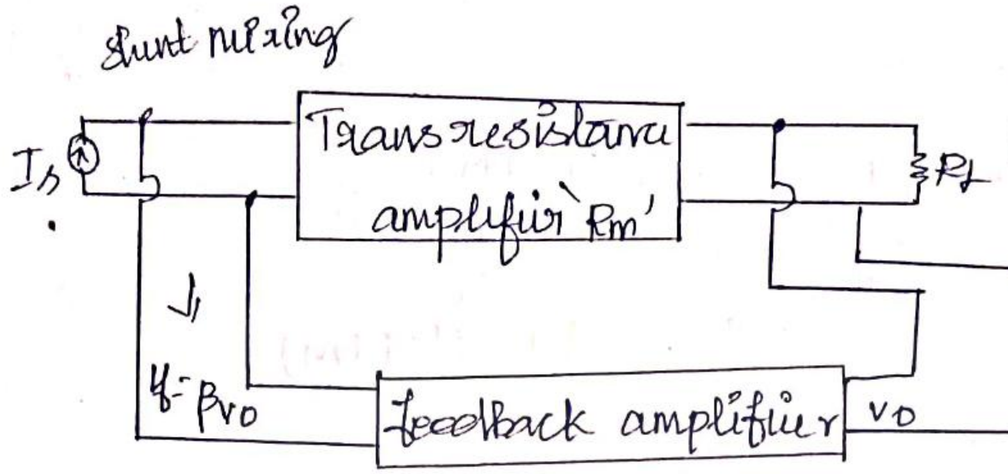
$R_o = \infty \quad R_{of} = R_o(1+\beta G_M) = \infty$

$R'_{of} = R_L = 2.2\times10^{3}\ \Omega.$

Voltage shunt feedback.

→ shunt derived, shunt fed feedback connection

→ feedback signal $I_f \propto V_o$ voltage.



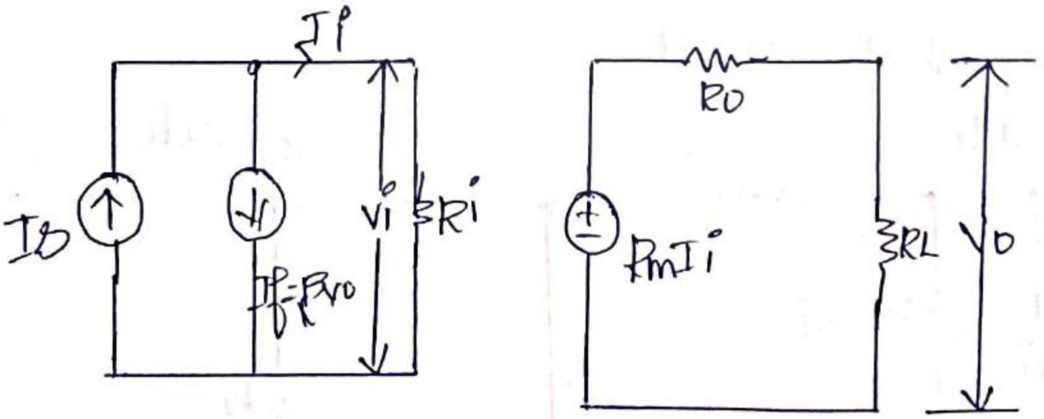
[TOPOLOGY]

$$\beta = \frac{I_f}{V_o}$$

→ This is otherwise called as transresistance amplifier *To derive input resistance and

$R_{if} = V_i / I_s$.

Step1: draw the Equivalent circuit (Thevinins).



Step2: Apply KVL at input side

$$I_s = I_i + I_f = I_i + \beta V_o$$

Step 3: obtain V_o, consider output side & Apply voltage division Rule.

$$V_0 = \frac{R_m I_i R_L}{R_L + R_0} \quad \left[\text{Let } R_m = \frac{R_m R_L}{R_0 + R_L} \right]$$

$$\boxed{v_0 = R_m I_i}$$

Step 4: sub v_0 in I_s

$$I_s = I_i + R_m \beta I_i = I_i (1 + \beta R_m)$$

we know that $R_{if} = \dfrac{V_i}{I_s} = \dfrac{V_i}{I_i (1+\beta R_m)}$, $\dfrac{V_i}{I_i} \rightarrow R_i$

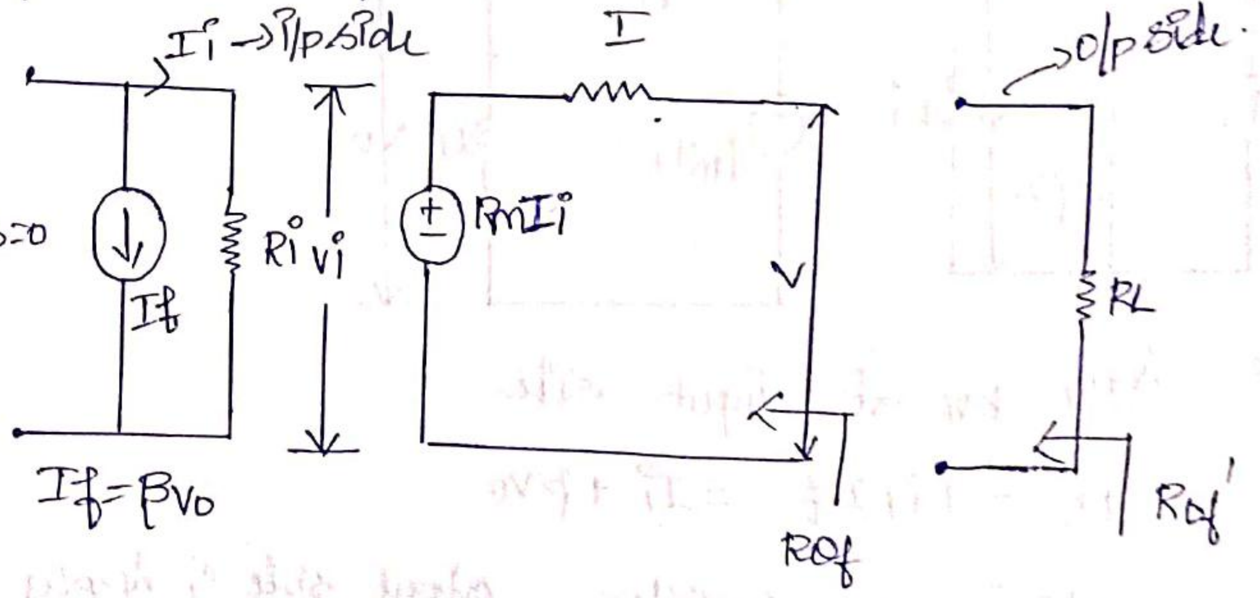
$$\boxed{R_{if} = \frac{R_i}{1 + \beta R_M}}$$

To derive R_{of}

Remove R_L & open circuit the current source,

$I_s = 0$

Step 1: Draw Equivalent circuit



$I_f = \beta V_0$

Step 2: Apply KVL & obtain I from o/p side

$$R_m I_i + I R_o - V = 0 \qquad \therefore \; I = \frac{V - R_m I_i}{R_o}$$

from i/p side $\quad I R_o = V - R_m I_i$

$I_i = -I_f = -\beta V$ substitute in equation (1) I.

$$I = V - R_m(-\beta V) = \frac{V + R_m \beta V}{R_o}$$

$$I = \frac{V(1+\beta R_m)}{R_o} \qquad \therefore \; \frac{V}{I} = R_{of} = \frac{R_o}{1+\beta R_m}.$$

Step 3: Obtain R_{of}

$$R'_{of} = R_{of} \parallel R_L = \frac{R_{of} R_L}{R_{of} + R_L}$$

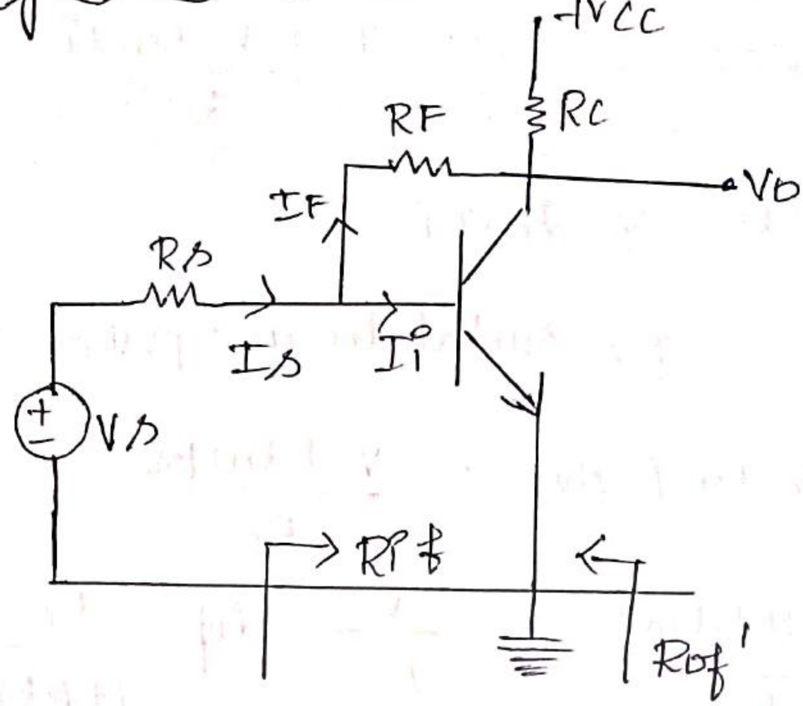
Sub R_{of}' = $$R_{of}' = \frac{\dfrac{R_o}{\cancel{1+\beta R_M}} R_L}{\dfrac{R_o}{\cancel{1+\beta R_m}} + R_L}$$

$\div$ $R_o + R_L$

$$R'_{of} = \frac{\underbrace{R_o R_L / R_o + R_L}_{R_o'}}{1 + \dfrac{1 + \beta R_m R_L}{R_o + R_L}} \Rightarrow \frac{R_o'}{1+\beta R_M}$$

$$R'_{of} = \frac{R_o'}{1+\beta R_M}.$$

Voltage shunt feedback Example.



Step1: Identify the feedback in the given diagram set $V_O = 0$ (i,e) short ckt the outside feedback feedback becomes zero, so feedback signal is voltage.

→ output voltage $V_O > V_i$

$$I_F = \frac{V_i - V_O}{R_F} = \frac{-V_O}{R_F} \approx \beta V_O$$

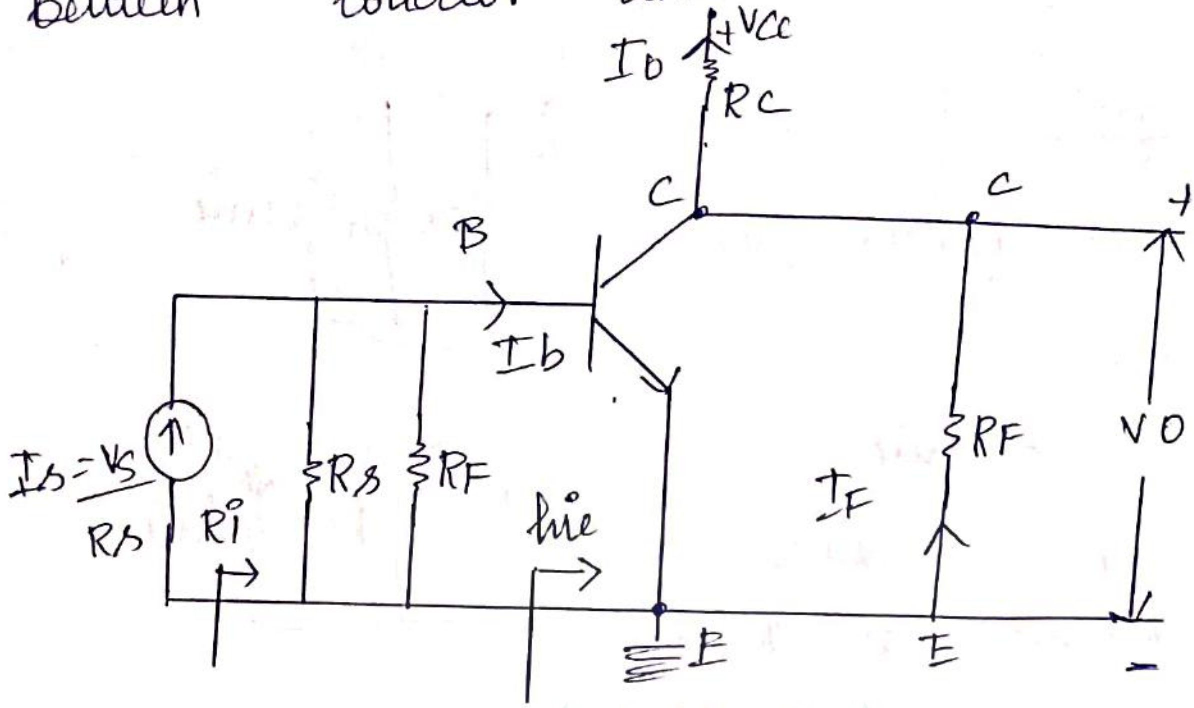
$$\boxed{\beta = \frac{I_F}{V_O}}$$

→ $I_s = I_i + I_F$ (shunt mixing)

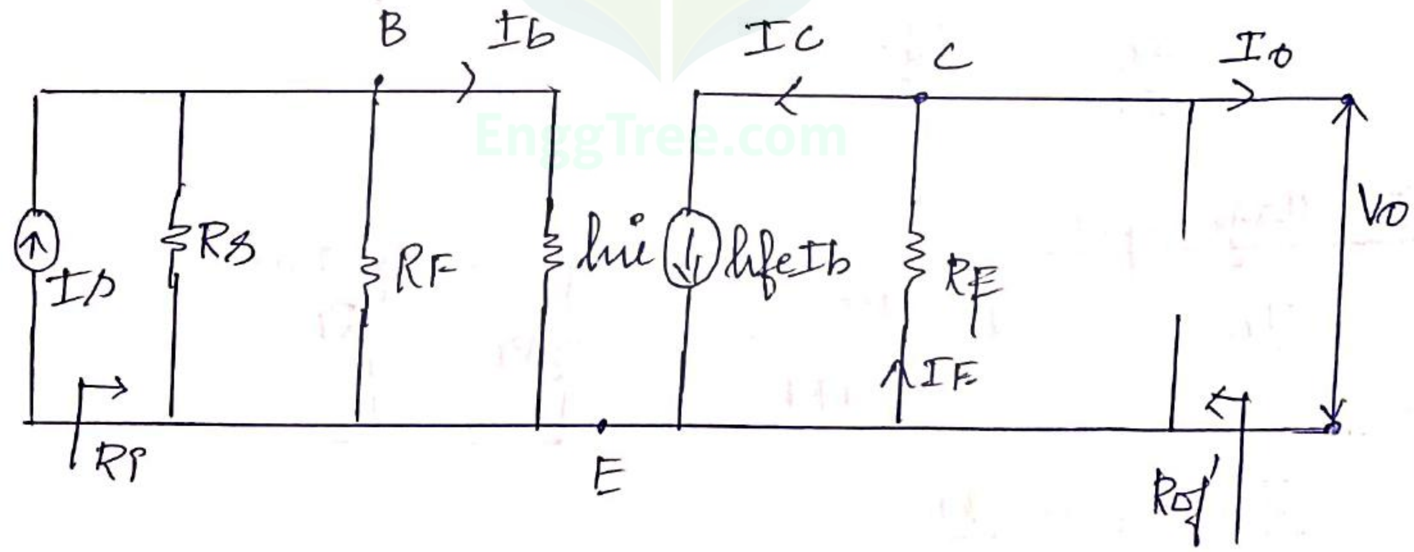
Step 2: obtain the simplified diagram.

To obtain i/p side short ckt the o/p side $V_O = 0$ this will place RF between base & Emitter

∴ To obtain o/p side → $v_i = 0$ this will place RF between collector and Emitter



Step 3: Replace transistor by h-parameter model



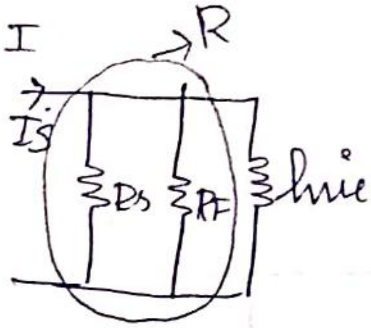
Step 4: calculate β

$$\beta = \frac{I_R}{V_O} = \frac{-V_O/RF}{V_O} = -\frac{1}{RF} \qquad I_F = \frac{-V_O}{RF}$$

Step 5: calculate openloop transistor gain

$$R_M = \frac{V_O}{I_S} = \frac{I_O R_L}{I_S}$$

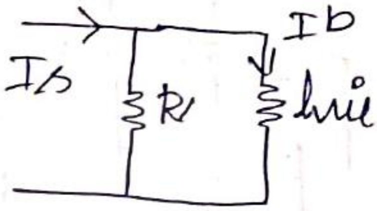
But $\frac{I_o}{I_s} = \frac{I_b}{I_s} \times \frac{I_c}{I_b} \times \frac{I_o}{I_c}$



Ist stage gain $\frac{I_b}{I_s} = ?$

using current division rule

$$I_b = I_s \frac{R}{R+h_{ie}}$$

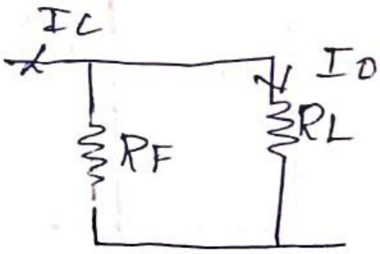


$$\frac{I_b}{I_s} = \frac{R}{R+h_{ie}}$$ where $R = \frac{R_S R_F}{R_S+R_F}$

IInd stage gain → transistor curr gain

$$\frac{I_c}{I_b} = h_{fe}$$

III stage gain



$$I_o = -I_c \frac{R_F}{R_F+R_L}$$

$$\frac{I_o}{I_c} = -\frac{R_F}{R_F+R_L}$$

Now substitute all gain in $\frac{I_o}{I_s}$

So $$\frac{I_o}{I_s} = \frac{R}{R+h_{ie}} \times h_{fe} \times \frac{-R_F}{R_F+R_L}$$

$$\therefore \frac{I_O}{I_S} = \frac{-R_F R h_{fe}}{(R+h_{ie})(R_F+R_L)}$$ sub this in R_M

$$R_m = \frac{I_O}{I_S} R_L = \frac{-h_{fe} R_F R_L}{(R+h_{ie})(R_F+R_L)}$$

Step 6: Calculate $D, R_{mF}, A_{vf}, R_{if}, R_{of}, R_{of}'$

$$D = 1+\beta R_M = 1+\frac{(1+h_{fe})\, R\, \cancel{R_F}\, R_L}{(+R_F)(R_F+R_L)(R+h_{ie})}$$

$$D = \frac{1+h_{fe} R R_L}{(R_F+R_L)(R+h_{ie})}$$

1) $R_{mf} = R_m / D$

2) $A_{vf} = \frac{V_O}{V_S} = \frac{I_O}{I_S / R_S} = \frac{R_{mf}}{R_S}$

3) $R_i = R_S \| R_F \| h_{ie}$

4) $R_{if} = \frac{R_i}{D}$

5) $R_O = R_F$ 6) $R_{of} = \frac{R_O}{1+\beta R_m} = \frac{R_F}{1+\beta R_M}$

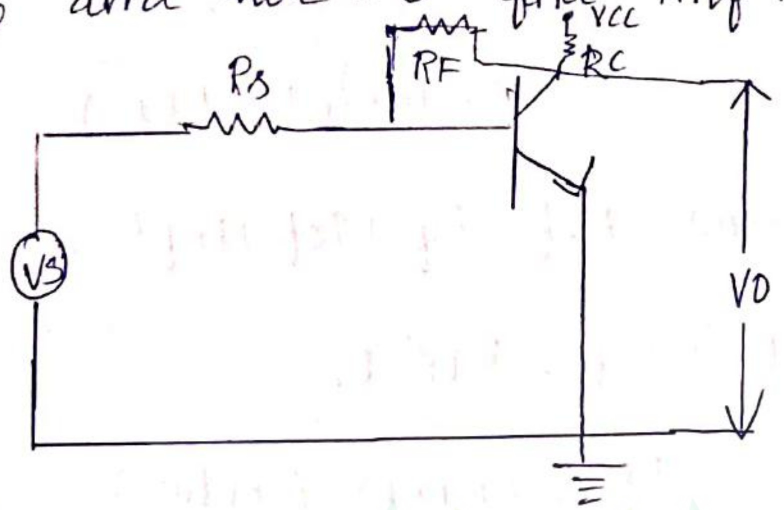
7) $R_{of}' = R_{of} \| R_C \Rightarrow R_O' = R_F \| R_C = \frac{R_F R_C}{R_F+R_L}$

(or)

$R_{of}' = R_O' / D$

University Problem: (Voltage Shunt feedback)

The circuit of fig has the following parameters $R_C = 4k\Omega$, $R_F = 40k\Omega$, $R_S = 10k\Omega$, $h_{ie} = 1.1k\Omega$, $h_{fe} = 50$ and $h_{oe} = 0$ find R_{mf}, A_{vf} R_{if} and R_{of}'.



Solution:

Type of feedback is – voltage shunt

$$\beta = -\frac{1}{R_F} = \frac{-1}{40\times10^3} = -2.5\times10^{-5}$$

$$\rightarrow R_m = \frac{-h_{fe} R R_F R_L}{(R+h_{ie})(R_F+R_L)} \qquad R_L = R_C.$$

where $R = \frac{R_S R_F}{R_S+R_F} = \frac{10\times10^3 \times 40\times10^3}{10\times10^3 + 40\times10^3} = 8000\,\Omega.$

$$R_m = \frac{-50 \times 8000 \times 40\times10^3 \times 4\times10^3}{(8000+1.1\times10^3)\ (40\times10^3+4\times10^3)}$$

$$\boxed{R_m = -159.8k\Omega}$$

$$D = 1+\beta R_m = 1+2.5\times10^{-5} \times 159.8\times10^3$$
$$= 4.996 = 5$$

$$R_{mf} = \frac{R_m}{D} = \frac{-159.8\times10^3}{5} = -31.96k\Omega.$$

$\rightarrow$ $$A_{vf} = R_{mf}/R_s = \frac{-31.96\times10^3}{10\times10^3} = -3.196$$

$\rightarrow$ $R_i = R_s || R_F || h_{ie}$

$$\frac{1}{R_i} = \frac{1}{R_s} + \frac{1}{R_F} + \frac{1}{h_{ie}}$$

$$= \frac{1}{10\times10^3} + \frac{1}{40\times10^3} + \frac{1}{1.1\times10^3}$$

$$\frac{1}{R_i} = 1.034\times10^{-3}$$

$$\therefore R_i = \frac{1}{1.034\times10^{-3}} = 967.03\Omega.$$

$\rightarrow$ $$R_{if} = \frac{R_i}{D} = \frac{967.03}{5} = 193.4\Omega$$

$$R_o = R_F = 40\times10^3$$

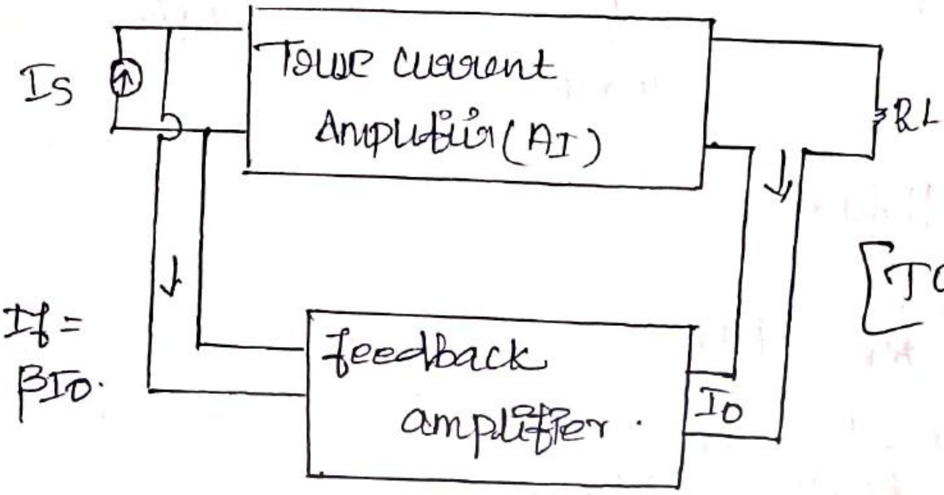
$\rightarrow$ $$R_{of}' = \frac{R_o'}{D} = \frac{R_C || R_F}{D} = \frac{\frac{R_C R_F}{R_C + R_F}}{D}$$

$$R_{of}' = \frac{\frac{4\times10^3 \times 40\times10^3}{4\times10^3 + 40\times10^3}}{4.996} = 727.85\Omega.$$

$$R_{of}' = 728\Omega.$$

Current Shunt feedback.

→ series derived shunt feedback



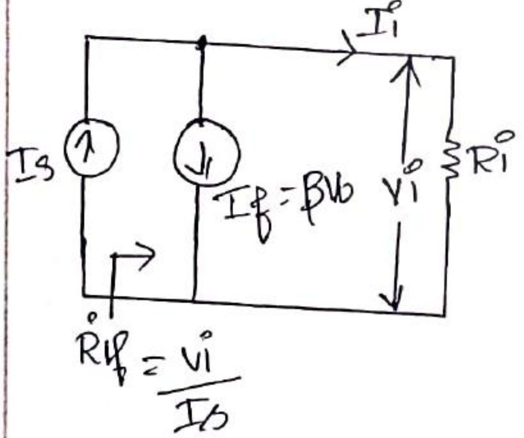
[TOPOLOGY]

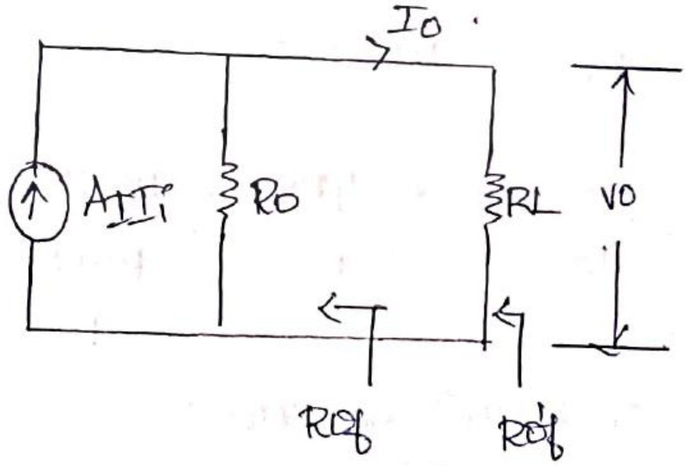
→ Ri↑, Ro↓

→ True current amplifier

→ Current feedback factor $\beta = \frac{I_f}{I_o}$.

To derive input Resistance with feedback (R_{if}) (NORTON Equivalent circuit)





apply KCL at input side

$$I_s = I_i + I_f = I_i + \beta I_o.$$

from output side, using current division

$$I_o = \frac{A_I I_i R_o}{R_o + R_L}$$

Assume

$$\frac{A_I R_o}{R_o + R_L} = A_I$$

$I_o = A_I I_i$

substitute I_o in I_s

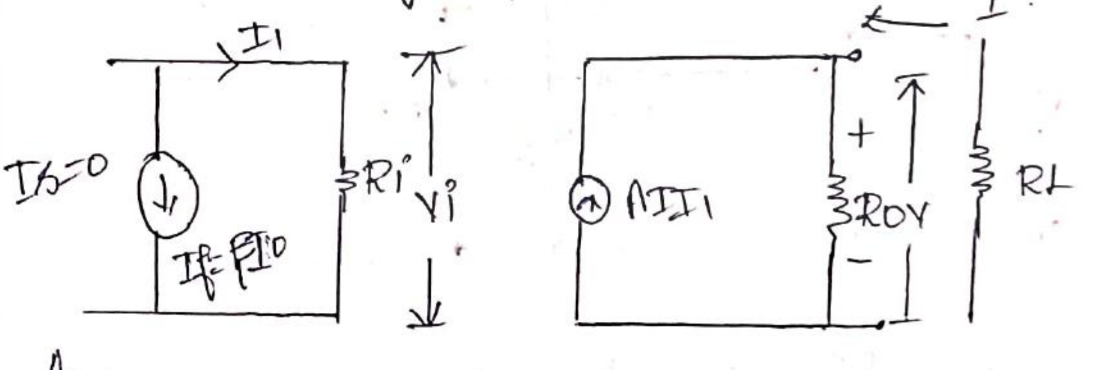
$I_s = I_i + \beta A_I I_i = I_1(1+\beta A_I)$

$\therefore R_{if} = \frac{V_1}{I_s}$ substitute I_s

$$R_{if} = \frac{V_1}{I_1(1+\beta A_I)} \quad \boxed{R_{if} = \frac{R_i}{1+\beta A_I}}$$

To derive Output Resistance (R_{of}).

Remove R_L i.e. open circuit the source Apply external voltage & find $\frac{V}{I}$



Apply KVL at Node

$I = \frac{V}{R_o} - A_I I_i$ We know that $I_f = \beta I_1$

$I_i = -I_f = -\beta(-I) = \beta I$

$I = \frac{V}{R_o} - A_I \beta I$

$I + A_I \beta I = \frac{V}{R_o}$

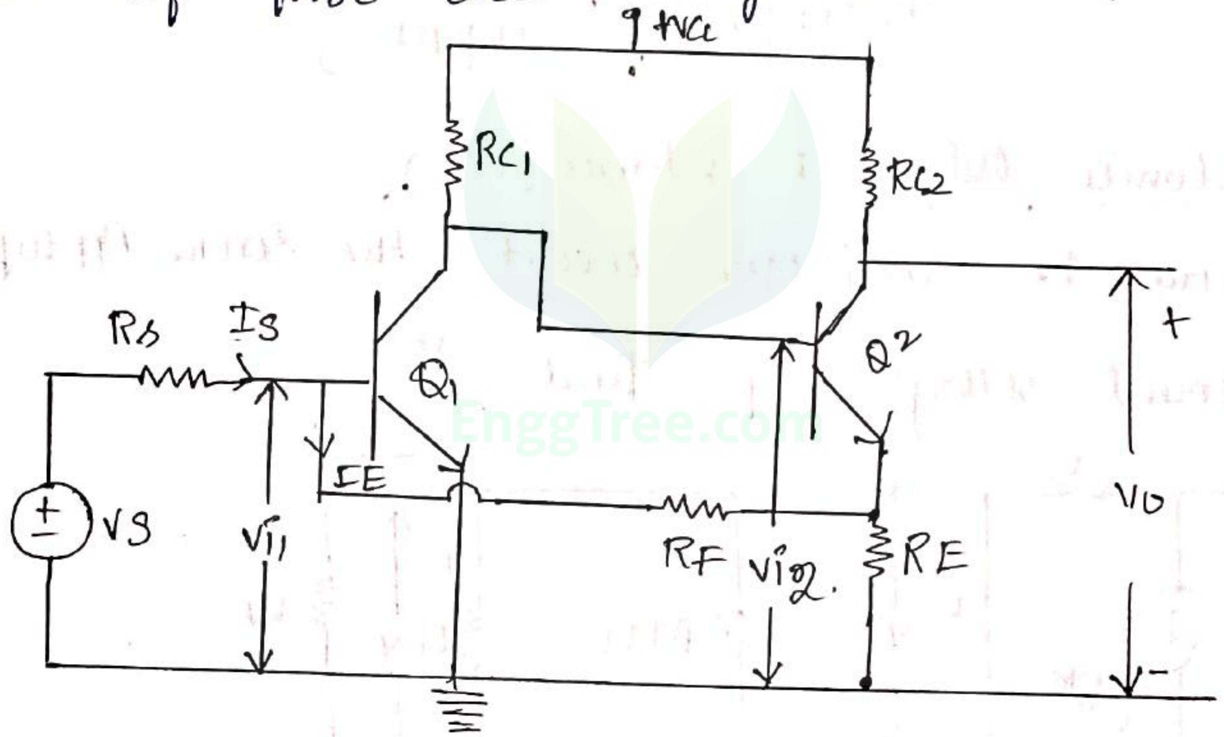
$$I(1+A_I\beta) = \frac{V}{R_O}$$

$$\frac{V}{I} = R_O(1+A_I\beta)$$

$$\boxed{R_{of} = R_O(1+A_I\beta)}$$

Current shunt feedback. [EXAMPLE]

cascade connection of two transistors with feedback from the Emitter of Second Transistor to the base of first one through Resistor R_F



Step 1: To Identify Topology.

If $V_O = 0$ feedback signal will not be zero,

If $I_O = 0$ open circuit feedback signal zero

So feedback is current and it is in parallel with the input

Step 2: To find the simplified diagram open circuit the output side and short circuit input side

a.) To find input side, set $I_0 = 0$

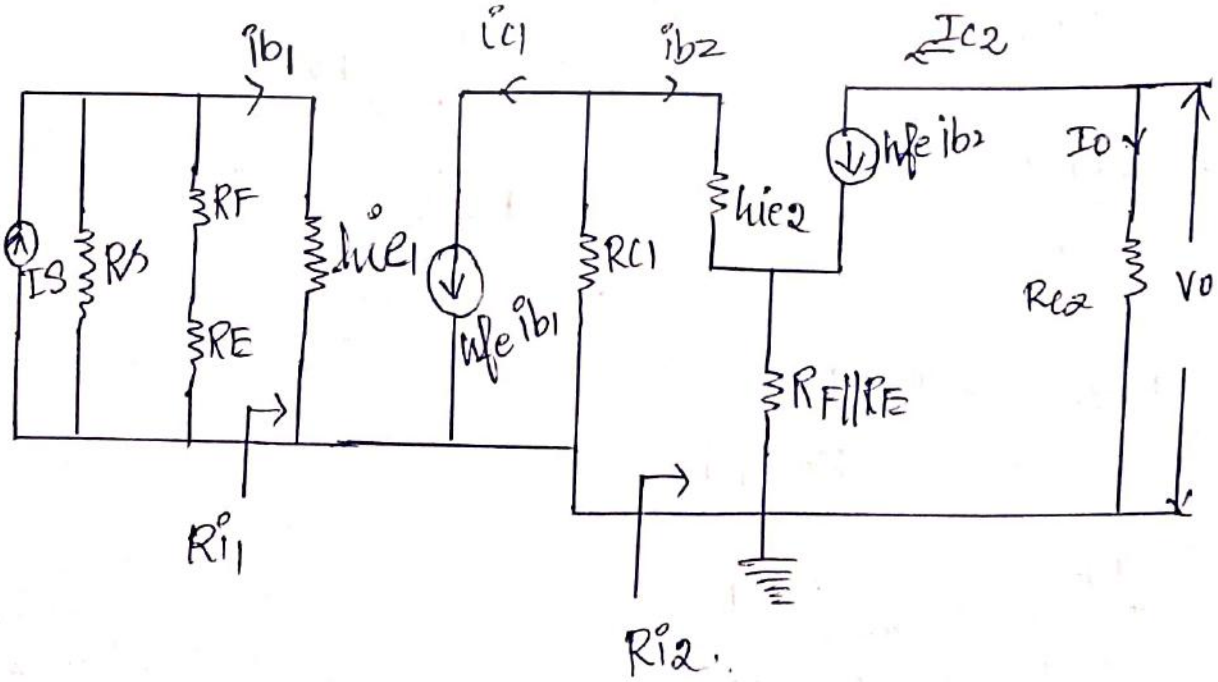
→ R_F & R_E appears in series across Q_1

b. To find output side, set $V_i = 0$ short circuit input of Q_1

→ R_F and R_E appears in parallel

Step 3: use Norton's Equivalent → feedback signal is current.

Step 4: Replace transistor with h-parameters equivalent circuit.



Step 5: calculate 'β'

$$\beta = \frac{\text{feedback signal}}{\text{output signal}} = \frac{I_f}{I_o}$$

$$\beta = \frac{\cancel{I_o}\dfrac{R_E}{R_E+R_F}}{\cancel{I_o}} = \frac{R_E}{R_E+R_F}$$

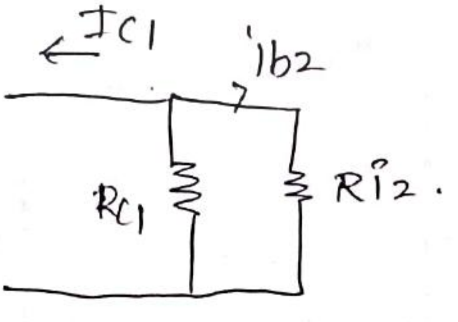
Step 6: open loop current gain (A_I)

$$A_i = \frac{I_o}{I_s} = \frac{-I_{C2}}{I_s} = \frac{-I_{C2}}{I_{b2}} \times \frac{I_{b2}}{I_{C1}} \times \frac{I_{C1}}{I_{b1}} \times \frac{I_{b1}}{I_s}$$

where $\frac{I_{C2}}{I_{b2}} = -h_{fe}$ (Q_2 gain)

$$\frac{I_{C1}}{I_{b1}} = h_{fe} \text{ (}Q_1\text{ gain)}$$

$$\frac{I_{b2}}{I_{C1}} = ?$$



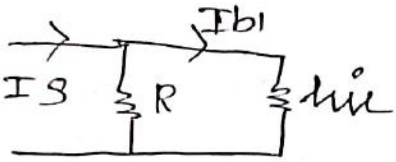
$$I_{b2} = -I_{C1}\frac{R_{C1}}{R_{C1}+R_{i2}}.$$

$$\frac{I_{b2}}{I_{C1}} = \frac{-R_{C1}}{R_{C1}+R_{i2}}.$$

Where

$$R_{i2} = h_{ie} + (1+h_{fe})\, R_E \| R_F$$

$$\frac{I_{b1}}{I_s} = ?$$



$\rightarrow R = R_s \| (R_F + R_E)$

$$I_{b1} = \frac{I_s R}{R + h_{ie}}$$

$$\frac{I_{b1}}{I_s} = \frac{R}{R + h_{ie}}$$

$$A_I = (-h_{fe}) \times \left(\frac{-R_{C1}}{R_{C1} + R_{i2}}\right)(h_{fe})\left(\frac{R}{R + h_{ie}}\right)$$

$$A_I = \frac{h_{fe}^2\, R_{C1}\, R}{(R_{C1} + R_{i2})(R + h_{ie})}$$

Step 7: calculate D, R_i, R_{if}, R_o, R_{of}, A_{vf}

$$D = 1 + \beta A_I$$

$$R_i = R_s \| (R_F + R_E) \| h_{ie}$$

$$R_{if} = R_i / D$$

$$R_o = \infty$$

$$R_{of} = R_o \times D = \infty$$

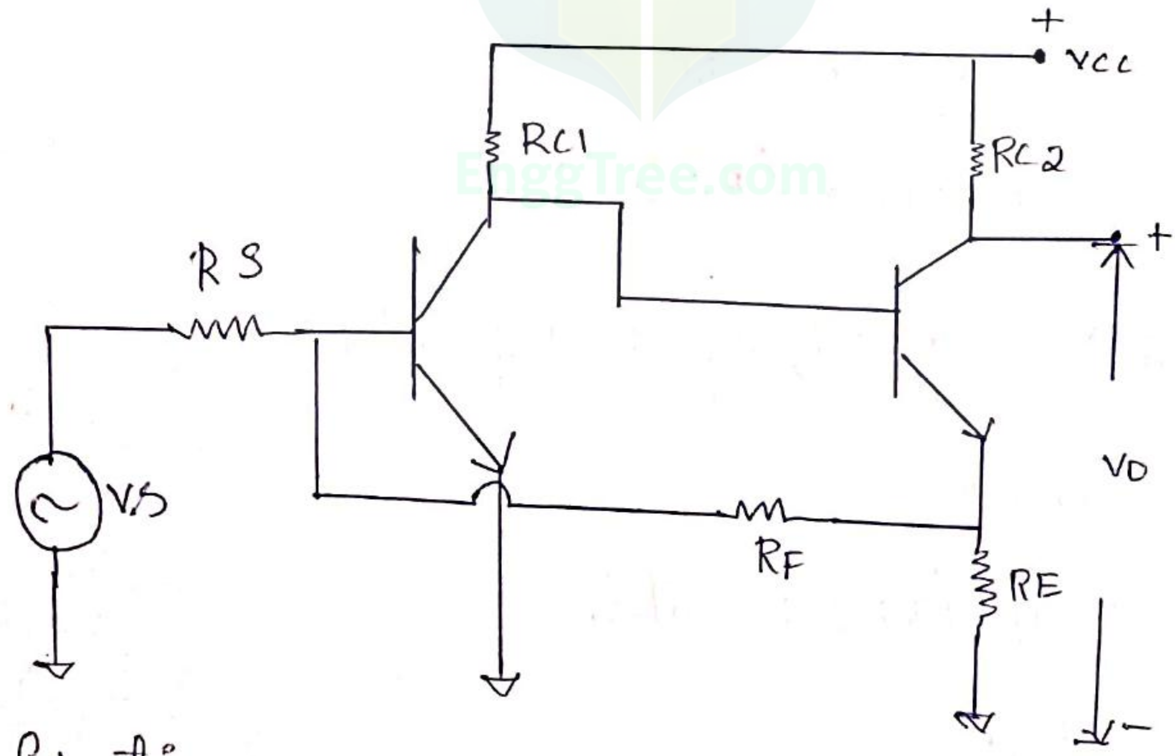
$R_{of}' = R_{E2}$

$A_{If} = A_I / D$

$$A_{vf} = \frac{V_o}{V_s} = \frac{-I_{C2} R_{C2}}{I_s R_s} = \frac{A_{If} R_{C2}}{R_s}$$

CURRENT SHUNT FEEDBACK AMPLIFIER

Problem: Identify the Nature of feedback in the given figure let $R_{C1} = 3k\Omega$, $R_{C2} = 500\Omega$, R_E, 50Ω, $R_s = R_F = 1.2k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1k\Omega$, $h_{re} = h_{oe} = 0$. Determine overall Voltage gain (A_{vf}), A_{if}, R_{if}, R_{of}.



Solution

$$\beta = \frac{R_E}{R_E + R_F} = \frac{50}{50 + 1.2 \times 10^3} = 0.04$$

Current gain $A_I = \dfrac{h_{fe}^2 \; R_{C1} R_1}{(R_{C1} + R_{i2})\,(R + h_{ie})}$

Where

$R = R_S \,||\, (R_F + R_E)$

$= 1.2\times10^3 \,||\, 1250$

$\dfrac{1}{R_{eq}} = \dfrac{1}{R_1} + \dfrac{1}{R_2} \ldots$

$= \dfrac{1}{1.2\times10^3} + \dfrac{1}{1250}.$

$\dfrac{1}{R_{eq}} = 1.633\times10^{-3}$

$R = R_{eq} = \dfrac{1}{1.633\times10^{-3}}$

$R_{i2} = h_{ie} + (1+h_{fe})(R_E||R_F)$

$= 1.1\times10^3 + (1+50)\;(50||1.2\times10^3)$

$= 1.1\times10^3 + 51\left(\dfrac{50\times1.2\times10^3}{50+1.2\times10^3}\right)$

$= 1.1\times10^3 + 51\times48$

$\boxed{R_{i2} = 3548\,\Omega}$

$A_I = \dfrac{h_{fe}^2 \; R_{C1} R_1}{(R_{C1} + R_{i2})\,(R + h_{ie})}$

$$= \frac{(50)^2 \times 3\times10^3 \times 612.2448}{(3\times10^3 + 3548)\ (612.2448 + 1.1\times10^3)}$$

$$A_I = \frac{4.59183\times10^9}{11.2117\times10^6} = 409.55 \Rightarrow 410.$$

$$D = 1+\beta A_I = 1+0.04\times409.55 = 17.38$$

$$A_{If} = \frac{A_I}{D} = \frac{409.55}{17.38} = 23.56$$

$$A_{vf} = \frac{A_{If} R_{C2}}{R_S} = \frac{23.56\times500}{1.2\times10^3} = 9.8166$$

$$R_i = R_S \,||\, (R_F + R_E) \,||\, h_{ie}$$

$$\frac{1}{R_i} = \frac{1}{R_S} + \frac{1}{R_F+R_E} + \frac{1}{h_{ie}}$$

$$\frac{1}{R_i} = \frac{1}{1.2\times10^3} + \frac{1}{1250} + \frac{1}{1.1\times10^3}$$

$$\frac{1}{R_i} = 2.542\times10^{-3} \qquad R_i = \frac{1}{2.542\times10^{-3}} = 393.32\,\Omega.$$

$$R_{if} = R_i/D = \frac{393.32}{17.38} = 22.63\,\Omega.$$

Verified N. [signature] 13/9/19

$R_o = \infty$, $R_{of} = \infty$ $\quad R'_{of} = R_{C2} = 500\,\Omega.$

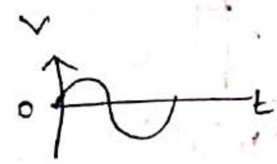
Oscillators:-

A circuit which is used to generate a periodic Voltage without an AC Input s/g is called as oscillator.

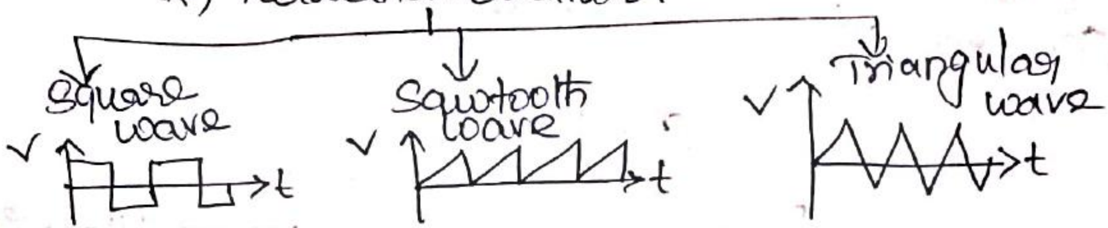
Classification of oscillators:-

1) According to waveform Generated.

*) Sinusoidal oscillator →



*) Relaxation oscillator.



2) According to frequency Generated.

* Audio frequency oscillator – upto 20KHZ
* Radio frequency oscillator :– 20 KHZ to 30MHZ
* Very high frequency oscillator – 30MHZ to 300MHZ
* Ultra high frequency oscillator – 300MHZ to 3GHZ
* Microwave frequency oscillator – above 3GHZ.

3) According to fundamental mechanism involved.

* Negative Resistance oscillator.
* Feedback oscillator

4) According to types of Circuit used

1. LC Tuned oscillator – Hartley, Colpitts, Clapp Oscillator.

2. RC Phase shift oscillator.
3. Wein bridge oscillator.

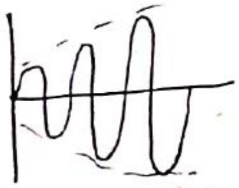
} RC oscillator.

Conditions for oscillators (Barkhausen Criteria).

i) $|A\beta| = 1$ ie, magnitude of Product of open loop gain of amplifier & β (gain) unity

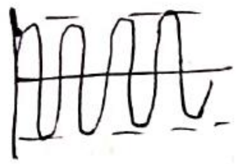
2) The total phase shift around the closed loop is zero or 360 degree.

* $|A\beta| > 1$



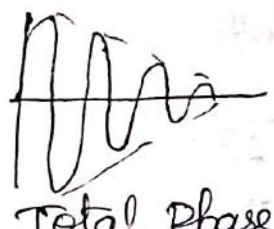
Total phase is 0 ~~or~~ 360° (Growing type)

* $|A\beta| = 1$



Total phase shift 0 or 360° (Switched Type).

* $|A\beta| < 1$



Total phase shift 0° or 360° (decaying type)

Oscillator

- RC oscillator
  - * RC phase shift oscillator
  - * wein bridge oscillator
- LC oscillator
  - * Hartley oscillator
  - * Colpitts oscillator
  - * clapp oscillator.

WEIN BRIDGE OSCILLATOR:-

Principle:-

* It is an RC oscillator which uses wein bridge as feedback Network.

* It uses two CE amplifier. Each stage provide 180° phase shift. Hence total shift is 360°.

Construction:-

* Frequency sensitive arms are R_1C_1 series and R_2C_2 parallel.

* The i/p to feedback (bridge) is applied from Collector of Q_2 through coupling capacitor C_2.

* Capacitor are varied to vary the frequency.

* R_4 is unbypassed emitter resistance.

Working:-

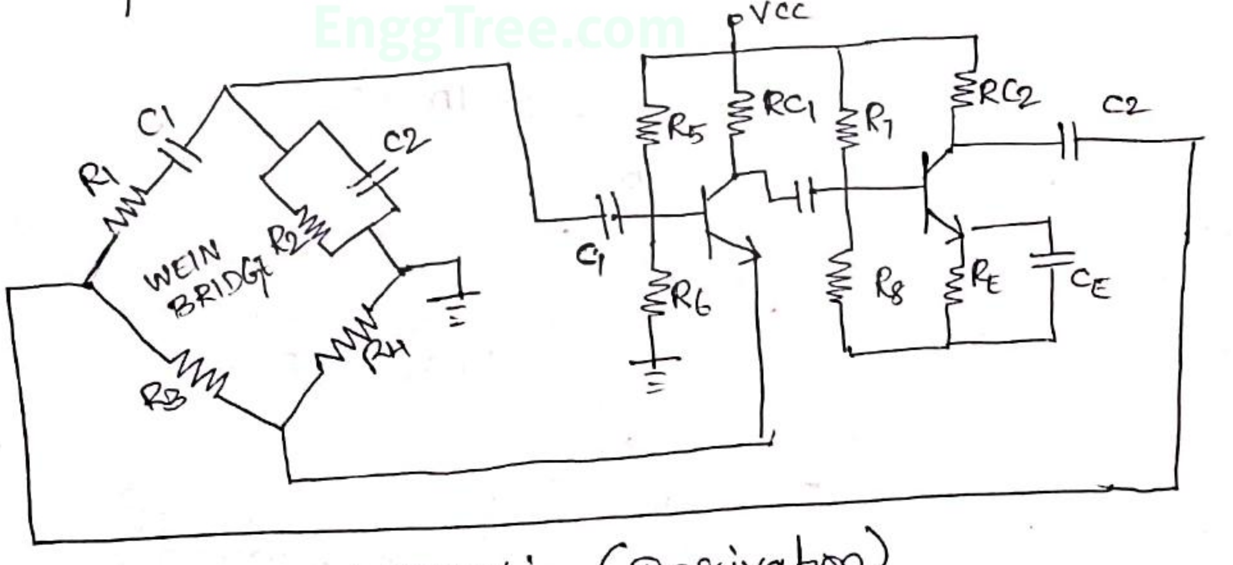
→ Amplitude stabilization $A \geq 3$.

→ Two stage amplifiers provide gain >3, which distort the o/p i.e, produce oscillation. The gain is controlled by providing negative feedback without bypassing R_4 in 1st stage

→ The feedback Network is called lead-lag Network. This is because at very low frequencies it act like a lead Network while at very high frequencies it work like lag Network.

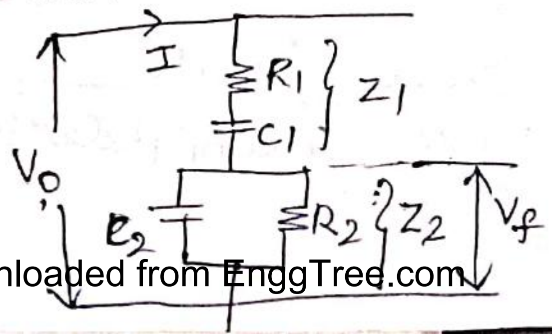
→ At balanced condition of weinbridge the phase shift for the s/g frequency is 0 (or) 360°.

→ The inphase voltage is amplified to reproduce the o/p at all other frequencies, the bridge is off balance that is the feedback and o/p voltage do not have the correct phase relationship to sustain oscillations.



FREQUENCY OF OSCILLATION:- (Derivation)

Consider equivalent Ckt,



$$Z_1 = R_1 + \frac{1}{j\omega C_1} \longrightarrow (1)$$

$$Z_2 = R_2 \| \frac{1}{j\omega C_2} = \frac{\frac{1}{j\omega C_2} \times R_2}{R_2 + \frac{1}{j\omega C_2}}.$$

$$Z_2 = \frac{\frac{R_2}{j\omega C_2}}{\frac{R_2 j\omega C_2 + 1}{j\omega C_2}}$$

$$Z_2 = \frac{R_2}{R_2 j\omega C_2 + 1} \longrightarrow (2)$$

Put current through the ckt as I,

$$I = \frac{V_{in}}{Z_1 + Z_2} \longrightarrow (3).$$

Similarly voltage across Z_2 can be written as,

$$V_f = I Z_2 \longrightarrow (4)$$

Substitute eq (3) in (4) we get

$$V_f = \frac{Z_2}{Z_1 + Z_2} V_{in} \Rightarrow \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2}$$

$$\beta = \frac{V_f}{V_{in}} = \frac{Z_2}{Z_1 + Z_2} \longrightarrow (5)$$

Sub (1) & (2) in (5).

$$\beta = \frac{\frac{R_2}{R_2 j\omega C_2 + 1}}{\frac{1 + j\omega R_1 C_1}{j\omega C_1} + \frac{R_2}{1 + j\omega R_2 C_2}}$$

$$= \frac{\frac{R_2}{1 + R_2 j\omega C_2}}{\frac{(1 + j\omega R_1 C_1)(1 + j\omega R_2 C_2) + j\omega R_2 C_1}{(j\omega C_1)(1 + j\omega R_2 C_2)}}.$$

$$\Rightarrow \frac{j\omega C_1}{1 + j\omega R_2 C_2 + j\omega R_1 C_1 - \omega^2 R_1 C_1 R_2 C_2 + j\omega C_1 R_2} \Rightarrow \frac{j\omega C_1 R_2}{(1 - \omega^2 R_1 C_1 R_2 C_2) + j\omega [R_2 C_2 + R_1 C_1 + R_2 C_1]} \longrightarrow (6)$$

Now multiply & divide by conjugate term, we get (45)

$$\beta = \frac{j\omega R_2C_1\left[(1-\omega^2R_1R_2C_1C_2) - j\omega(R_1C_1+R_2C_2+R_2C_1)\right]}{(1-\omega^2R_1R_2C_1C_2)^2 + \omega^2(R_1C_1+R_2C_2+R_2C_1)^2}$$

$$\beta = \frac{j\omega R_2C_1(1-\omega^2R_1R_2C_1C_2) + \omega^2R_2C_1(R_1C_1+R_2C_2+R_2C_1)}{(1-\omega^2R_1R_2C_1C_2)^2 + \omega^2\left[R_1C_1+R_2C_2+R_2C_1\right]^2} \quad \text{— (7)}$$

Inorder to consider zerophaseshift Imaginary part is equate to zero,

$$\frac{\omega R_2C_1(1-\omega^2R_1C_1R_2C_2)}{(1-\omega^2R_1R_2C_1C_2)^2+\omega^2(R_1C_1+R_2C_2+R_2C_1)^2} = 0$$

$$1-\omega^2R_1C_1R_2C_2 = 0$$

$$\omega^2R_1C_1R_2C_2 = 1$$

$$\omega^2 = \frac{1}{R_1C_1R_2C_2}$$

$$\omega = \frac{1}{\sqrt{R_1C_1R_2C_2}} \qquad \boxed{\omega = 2\pi f}$$

$$2\pi f = \frac{1}{\sqrt{R_1C_1R_2C_2}}$$

$$\boxed{f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}} \longrightarrow (8)$$

$R_1 = R_2 = R$, $C_1 = C_2 = C$

$$\boxed{f = \frac{1}{2\pi RC}}$$

Using $\omega = \frac{1}{RC}$ in (7) we get

$$\boxed{\beta = 1/3}$$

According to Barkhausan,

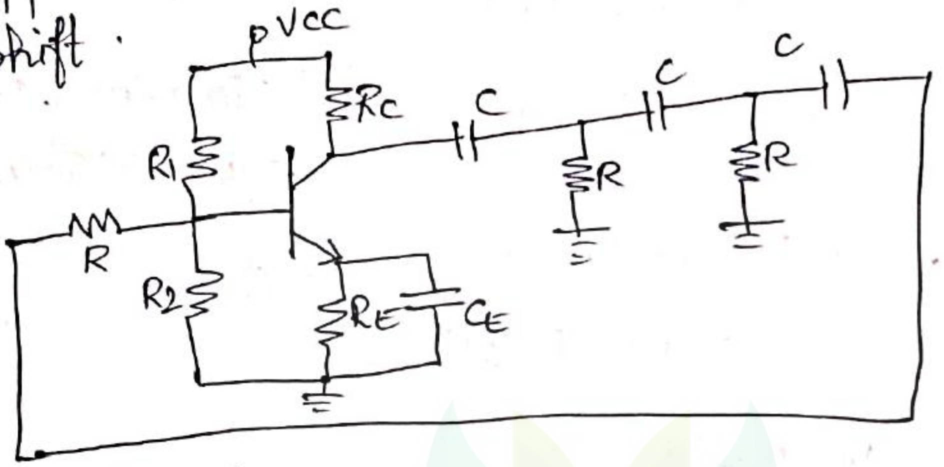
$$|A\beta| \geq 1 \qquad \therefore A \geq 3$$

$|A \cdot \frac{1}{3}| \geq 1$ ... Gain is 3.

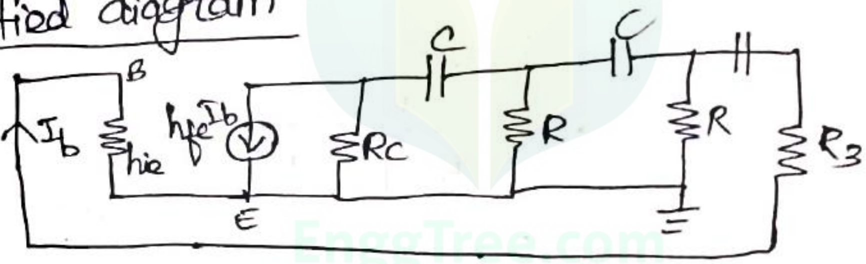
Rc phase shift oscillator :-

Introduction:-

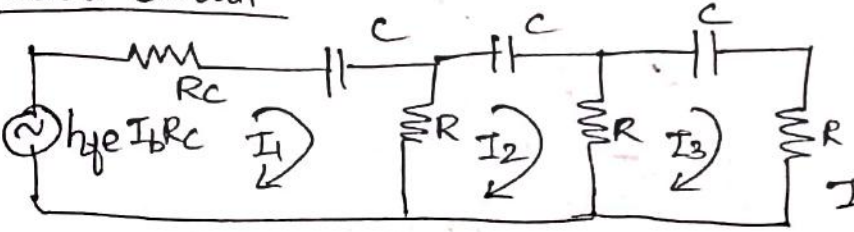
→ Rc phase shift oscillators are used to generate AC s/g of Audio frequency range. It is used in low frequency application, we know that CE amplifier produce 180° phase shift.



Simplified diagram.



Equivalent Circuit



$I_3 = I_b$.

WORKING:-

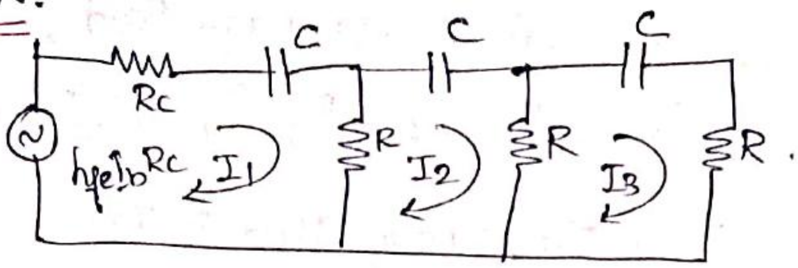
→ The feedback s/g is Coupled through the feedback Resistor R_3 in series with an amplifier stage input resistor. In order to make the three sections identical R_3 is chosen as

$R_3 = R - R_i$. R_i → Input Resistance h_{ie}.

→ when DC is ON, the movement of charge through (R, C) Produce noise signal (with frequency 0 to ∞)

→ Let the amplified voltage V_o at the o/p Port that is between collector and emitter of Transistor. V_o is larger than V_{in} and is 180° out of phase with V_{in}.

DERIVATION:-



$I_3 = I_b$.

Apply KVL to loop 1:-

$$R_cI_1 - jX_cI_1 + R(I_1 - I_2) + h_{fe}I_bR_c = 0$$

$$R_cI_1 - jX_cI_1 + RI_1 - RI_2 + h_{fe}I_3R_c = 0 \longrightarrow (1)$$

$$\Rightarrow I_1(R_c + R - jX_c) - RI_2 + h_{fe}I_3R_c = 0$$

Apply KVL in Loop 2:-

$$-jX_cI_2 + R(I_2 - I_1) + R(I_2 - I_3) = 0$$

$$-jX_cI_2 + RI_2 - RI_1 + RI_2 - RI_3 = 0$$

$$-RI_1 + I_2(2R) - I_2jX_c - RI_3 = 0$$

$$-RI_1 + I_2(2R - jX_c) - RI_3 = 0 \longrightarrow (2)$$

Apply KVL in Loop 3:-

$$-jX_cI_3 + RI_3 + R(I_3 - I_2) = 0$$

$$-jX_cI_3 + RI_3 + RI_3 - RI_2 = 0$$

$$-RI_2 + I_3(2R - jX_c) = 0 \longrightarrow (3)$$

Write (3) in Matrix form,

$$\begin{bmatrix} R_c + R - jX_c & -R & h_{fe}R_c \\ -R & 2R - jX_c & -R \\ 0 & -R & 2R - jX_c \end{bmatrix} = 0.$$

$$(R_c + R - jX_c)\left[(2R - jX_c)^2 - R^2\right] + R(-R)\left[2R - jX_c\right] + h_{fe}R_cR^2 = 0$$

$$(R_c + R - jX_c)\left[4R^2 + j^2X_c^2 - 2 \times 2R\,jX_c - R^2\right] - R^2\left[2R - jX_c\right] + h_{fe}R_cR^2 = 0$$

$$(R_c+R-jX_c)\left[4R^2-X_c^2-4RjX_c-R^2\right]-2R^3+jX_cR^2+h_{fe}R_cR^2=0.$$

$$4R_cR^2-R_cX_c^2-4RX_cjR_c-R^2R_c+4R^3-RX_c^2-4R^2jX_c-R^3-jX_c4R^2+jX_c^3$$
$$+4Rj^2X_c+jX_cR^2-2R^3+jX_cR^2+h_{fe}R_cR^2=0.$$

Seperate Real & Imaginary Part,

$$3R_cR^2+h_{fe}R^2R_c-X_c^2R_c-5RX_c^2+R^3+j(X_c^3-6R^2X_c-4RX_cR_c)=0$$

Equate Imaginary Part to Zero.

$$X_c^3-6R^2X_c-4RX_cR_c=0.$$

$$X_c\left[X_c^2-6R^2-4RR_c\right]=0.$$

$$X_c^2-6R^2-4R_cR=0.$$

$$\boxed{X_c^2=6R^2+4R_cR}$$

$$\frac{1}{\omega^2C^2}=6R^2+4R_cR.$$

$$\omega^2=\frac{1}{C^2(6R^2+4RR_c)}\Rightarrow\frac{1}{C^2R^2\left(6+\frac{4R_c}{R}\right)}.$$

where $\frac{R_c}{R}=K$,

$$\omega=\frac{1}{\sqrt{C^2R^2(6+4K)}}$$

$$\omega=2\pi f,\quad 2\pi f=\frac{1}{CR\sqrt{6+4K}}$$

$$\boxed{f=\frac{1}{2\pi RC\sqrt{6+4K}}}$$

To Derive Gain:-

Substitute X_c^2 in Real part, equals to zero.

$$3R^2R_c+h_{fe}R^2R_c-X_c^2R_c-5RX_c^2+R^3=0.$$

sub X_c^2 in above equation.

$$3R^2R_c+h_{fe}R^2R_c-(6R^2+4RR_c)R_c-5R(6R^2+4RR_c)+R^3=0$$

$$3RR_c+h_{fe}R^2R_c-6R^2R_c-4RR_c^2-30R^3-20R^2R_c+R^3=0.$$

$$h_{fe}R^2R_c - 29R^3 - 23R^2R_c - 4RR_c^2 = 0.$$

$$h_{fe}R^2R_c = 29R^3 + 23R^2R_c + 4RR_c^2.$$

$$h_{fe} = \frac{29R^3}{R^2R_c} + \frac{23R^2R_c}{R^2R_c} + \frac{4RR_c^2}{R^2R_c}.$$

We know $k = \frac{R_c}{R}$

$$h_{fe} = \frac{29}{k} + 23 + 4k.$$

Differentiate h_{fe} w.r to k.

$$\frac{dh_{fe}}{dk} = -\frac{29}{k^2} + 0 + 4.$$

$$-\frac{29}{k^2} + 4 = 0.$$

$$\frac{-29 + 4k^2}{k^2} = 0.$$

$$4k^2 = 29$$

$$k^2 = 29/4$$

$\boxed{k = 2.7}$ Sub k in h_{fe}.

$$h_{fe} = \frac{29}{2.7} + 23 + 4(2.7) = \boxed{44.54} \Rightarrow h_{fe}.$$

PROBLEM:-

1) In an RC phase shift oscillator if $R_1 = R_2 = R_3 = 200k\Omega$ and $C_1 = C_2 = C_3 = 100pF$. Find the frequency of oscillations

$$f = \frac{1}{2\pi RC\sqrt{6}} \Rightarrow \frac{1}{2 \times 3.14 \times 200 \times 10^3 \times 100 \times 10^{-12} \times \sqrt{6}}$$

$$\boxed{f = 3.248\ KHz}$$

Advantage:-

*) Good freq. stability
*) O/p is pure sine
*) Freq. independent of active device

Disadv

I) It is only suitable for Audio freq.
II) Difficult to control amplitude of oscillation

Problem

2) In a wein bridge oscillator if R=100kΩ and freq. of oscillation is 10kΩ, find C.

$$f = \frac{1}{2\pi RC}$$

$$C = \frac{1}{2\pi Rf}$$

$$C = \frac{1}{2\pi \times 100\times10^3 \times 10\times10^3}$$

$$\boxed{C = 159\,PF}$$

HARTLEY OSCILLATOR:-

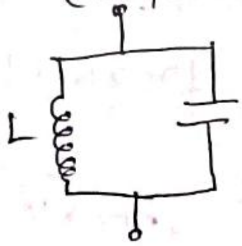
→ It is an LC oscillator commonly used a local oscillator in radio receivers.

LC oscillator working:-

→ A circuit which produces electrical oscillations of any desired frequency is known as Tank Circuit.

→ A simple oscillatory circuit consist of capacitor (C) and inductance coil (L) in parallel.

Tank circuit (simple ckt)



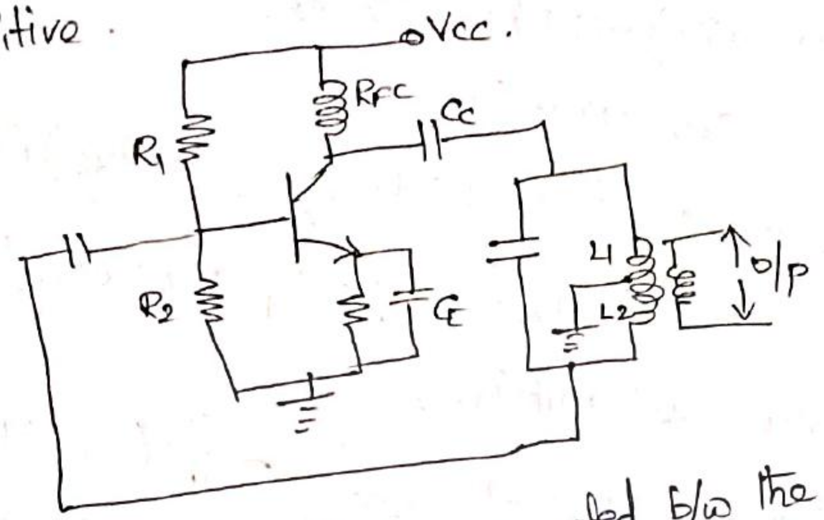
→ Tank circuit consist of 2 coils L_1 & L_2. The L_1 is inductively coupled to L_2 and it act as Auto Transformer.

→ The coil called RFC (Radio frequency choke) connected between collector & Vcc.

→ It act as a load for the collector & permit only DC current but blocks AC.

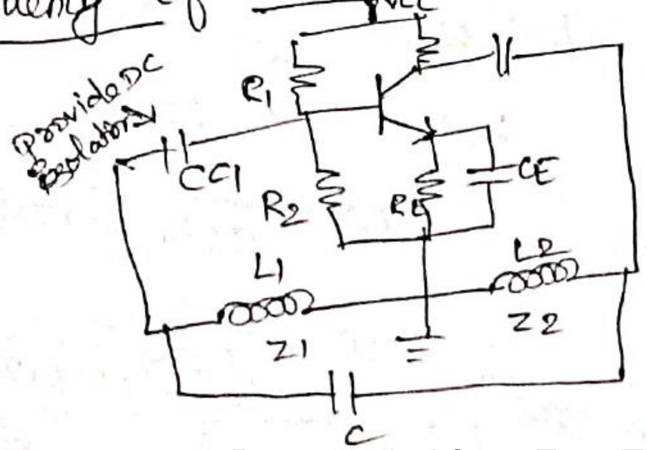
→ AutoTransformer introduces phase shift of 180° The phase reversal between the o/p & i/p voltage occurs because they are taken from opposite ends of coil with respect to tap. (9)

→ The Transistor also introduces a 180° Phase shift, therefore therefore the total phase shift 360° and hence the feedback is Positive.



Working:-
i) The capacitor CC, connected b/w the collector and the tuned circuit is called coupling capacitor.
ii) It permits only the AC current to pass to the Tank circuit. The capacitor CB called blocking capacitor. Further blocks the DC current. R1, R2, RE used to provide DC bias to the Transistor.
iii) The circuit is energized by switch ON the supply; the collector current flow to oscillation are produced because of positive feedback from the tank circuit.

Frequency of oscillation derivation:-



Derivation:-

$$Z_1 = j\omega L_1$$

$$Z_2 = j\omega L_2$$

$$Z_3 = \frac{1}{j\omega C} = \frac{-j}{\omega C}.$$

The General equation for oscillator is,

$$h_{ie}(Z_1+Z_2+Z_3) + Z_1Z_2(1+h_{fe}) + Z_1Z_3 = 0 \longrightarrow (1)$$

Sub Z_1, Z_2, Z_3 in (1)

$$h_{ie}\left(j\omega L_1 + j\omega L_2 + \frac{1}{j\omega C}\right) + j^2\omega L_1 \omega L_2(1+h_{fe}) + j\omega L_1 \cdot \frac{1}{j\omega C} = 0$$

$$h_{ie}\, j\omega\left[L_1 + L_2 - \frac{1}{\omega^2 C}\right] - \omega^2 L_1 L_2 - \omega^2 L_1 L_2 h_{fe} + \frac{L_1}{C} = 0$$

Taking Imaginary = 0

$$\omega h_{ie}\left[L_1 + L_2 - \frac{1}{\omega^2 C}\right] = 0.$$

$$L_1 + L_2 = \frac{1}{\omega^2 C}$$

$$\boxed{\omega^2 = \frac{1}{(L_1+L_2)C}}$$

$$(2\pi f)^2 = \frac{1}{(L_1+L_2)C}$$

$$\boxed{f = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}}$$

Condition for oscillation:-

Real part = 0.

$$-\omega^2 L_1 L_2 - \omega^2 L_1 L_2 h_{fe} + \frac{L_1}{C} = 0$$

$$\omega^2 L_1 L_2 (1+h_{fe}) - \frac{L_1}{C} = 0.$$

$$\frac{L_1}{C} = \omega^2 L_1 L_2 (1+h_{fe}) \longrightarrow (2)$$

sub ω^2 in (2).

$$\frac{L_1}{C} = \frac{1}{(L_1+L_2)C} L_1 L_2 (1+h_{fe})$$

To derive Gain

$$L_1 = \frac{L_1 L_2}{L_1 + L_2}(1 + h_{fe})$$

$$\frac{L_1 + L_2}{L_2} = (1 + h_{fe})$$

$$\boxed{h_{fe} = \beta = \frac{L_1}{L_2}}$$

Equivalent Inductance Leq,

$$L_{eq} = L_1 + L_2 + 2M$$

$$h_{fe} = \frac{L_1 + M}{L_2 + M}$$

$$Z_1 = j\omega L_1 + j\omega M$$

$$Z_2 = j\omega L_2 + j\omega M$$

$$\boxed{\text{Frequency } f = \frac{1}{2\pi\sqrt{L_{eq} \cdot C}}}$$

Problem

1) In Hartley oscillator $L_2 = 0.4mH$, $C = 0.004\mu F$, if the frequency of oscillator is 120KHz. Find the value of L_1. Neglect the mutual Inductance,

Soln

$$f = \frac{1}{2\pi\sqrt{(L_1 + L_2)C}}$$

To find L_1

Squaring,

$$f^2 = \frac{1}{4\pi^2(L_1 + L_2)C}$$

$$L_1 + L_2 = \frac{1}{4\pi^2 f^2 C}$$

$$L_1 = \left(\frac{1}{4\pi^2 f^2 C}\right) - L_2$$

$$= \left(\frac{1}{4\times3.14^2\times(120\times10^3)^2\times(0.004\times10^{-6})}\right) - 0.4\times10^{-3}$$

$$\boxed{L_1 = 0.04\,mH}$$

2) In Hartley oscillator, the value of capacitor in tuned circuit is 500pF and two series of coils have inductance 38μH & 12μH. Find the frequency of oscillation & feedback factor β.

$$f = \frac{1}{2\pi\sqrt{LC}}. \qquad L = L_1 + L_2 = 38\times10^{-6} + 12\times10^{-6}$$

$$L = 50\,\mu H$$

$$C = 500\,pF.$$

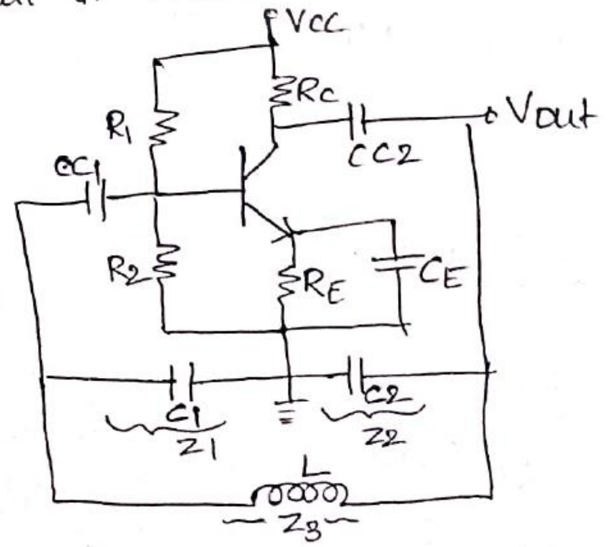
$$f = \frac{1}{2\pi\sqrt{50\times10^{-6}\times500\times10^{-12}}}$$

$$\boxed{f = 1\,MHz}$$

$$\beta = \frac{L_1}{L_2} = \frac{38\times10^{-6}}{12\times10^{-6}} = 3.166$$

COLPITTS OSCILLATOR:-

→ It is a LC oscillator of high frequency. An oscillator in which a parallel tuned tank circuit has two voltage dividing capacitor in series, with their common connection going to be emitter circuit in Transistor.



Construction:-

→ The Resistors R_1, R_2 & R_E Provide DC bias to Transistor.

→ C_E is bypass capacitor CC_1 & CC_2 are Coupling capacitor.

→ The feedback N/w Consisting of capacitors C_1 & C_2 and inductor L determines the frequency of oscillator.

WORKING:-

→ when the Supply +Vcc is ON, the current produced in tank circuit and Consequently damped harmonic oscillation occur in circuit.

→ The oscillatory current in tank circuit produces AC voltage across C_1 & C_2. the terminal 3 is grounded (zero Potential)

→ If the terminal 1 is +ve w.r.to 3. at any instant, terminal 2 will be negative potential w.r.to 3.

the Phase difference of 1 & 2 will be 180°. CE provides other 180°. Total phase shift at 360°.

→ It is used in s/g generators for frequencies 1MHz to 500MHz [USED IN SUPER HETERODYNE RADIO RECEIVER].

Frequency of oscillation Derivation:-

$$\left.\begin{aligned} Z_1 &= \frac{-j}{\omega C_1} \\ Z_2 &= \frac{-j}{\omega C_2} \\ Z_3 &= j\omega L \end{aligned}\right\} \rightarrow (1)$$

Condition for sustained oscillator,

$$h_{ie}(Z_1+Z_2+Z_3)+(1+h_{fe})(Z_1Z_2)+Z_1Z_3=0 \rightarrow (2)$$

Sub (1) in (2),

$$h_{ie}\left(\frac{-j}{\omega C_1}-\frac{j}{\omega C_2}+j\omega L\right)+(1+h_{fe})\left(\frac{-j}{\omega C_1}\times\frac{-j}{\omega C_2}\right)+\left(\frac{-j}{\omega C_1}\right)(j\omega L)=0.$$

Taking j outside. $\boxed{j^2=-1}$

$$-jh_{ie}\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)-\frac{(1+h_{fe})}{\omega^2 C_1 C_2}+\frac{L}{C_1}=0 \rightarrow (3)$$

Equating imaginary Part to zero,

$$h_{ie}\left(\frac{1}{\omega C_1}+\frac{1}{\omega C_2}-\omega L\right)=0$$

$$\frac{1}{\omega}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)=\omega L$$

$$\omega^2=\frac{C_2+C_1}{C_1C_2L} \quad \text{--- (4)}$$

$$\omega=\sqrt{\frac{C_1+C_2}{C_1C_2L}}$$

$\boxed{\omega=2\pi f}$

$$2\pi f=\sqrt{\frac{C_1+C_2}{C_1C_2L}}$$

$$\boxed{f=\frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{C_1C_2L}}}$$

To Derive Gain:-

Equate Real part (3) to zero,

$$\frac{-(1+h_{fe})}{\omega^2C_1C_2}=\frac{-L}{C_1}$$

Sub ω^2 (from 4) in above eqn $\Rightarrow \dfrac{1+h_{fe}}{\left(\frac{C_2+C_1}{C_1C_2L}\right)C_1C_2}=\dfrac{L}{C_1}$

$$\Rightarrow 1+h_{fe}=\frac{C_1+C_2}{C_1}$$

$$h_{fe}=\left(\frac{C_1+C_2}{C_1}\right)-1$$

$$=\frac{C_1+C_2-C_1}{C_1}$$

$$\boxed{h_{fe}=\frac{C_2}{C_1}} \Rightarrow \text{GAIN}$$

Problem

1) In Colpitts oscillator $C_1=1nF$ and $C_2=100nF$, If the freq. of oscillation is 100KHZ. Find the value of L. Also find minimum gain required for obtaining oscillations.

Solution

$$f=\frac{1}{2\pi}\sqrt{\frac{C_1+C_2}{C_1C_2L}}$$

squaring,

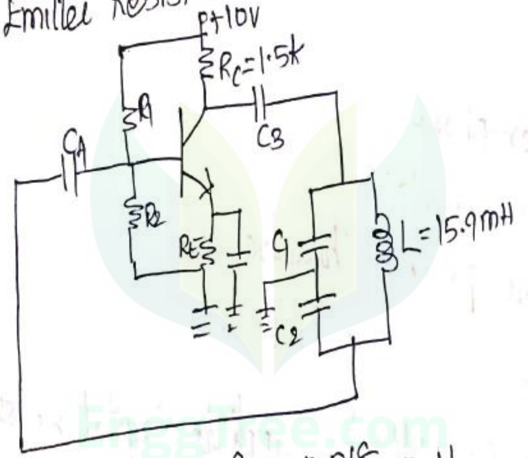
$$f^2 = \frac{1}{4\pi^2}\left(\frac{C_1+C_2}{C_1C_2L}\right)$$

$$L = \frac{C_1+C_2}{f^2 4\pi^2 C_1C_2} = \frac{101\,nF}{(100\times10^3)^2\times4\times3.14\times1\times10^{-9}\times100\times10^{-9}}$$

$$\boxed{L = 2.55\,mH}$$

$$Gain = \frac{C_2}{C_1} = \frac{100\,nF}{1\,nF} = 100$$

2) For the colpitts oscillator circuit shown in Fig, Find the values of
a) Feedback fraction
b) Minimum Gain to sustain oscillations
c) Emitter Resistor RE



a) Feedback fraction $= \frac{C_1}{C_2} = \frac{0.018}{0.16} = 0.11$

b) $A_{v(min)} = \frac{1}{\text{feedback fraction}} = \frac{C_2}{C_1} = \frac{1}{0.11} = 9$

c) We know $A_V = \frac{R_C}{R_E}$

$$R_E = \frac{R_C}{A_V} = \frac{1500}{9} = 167\,\Omega.$$

3) Determine the circuit oscillation frequency for Transistor Colpitts oscillator, $L = 100\,\mu H$, $C_1 = 0.005\,\mu F$, $C_2 = 0.01\,\mu F$.

$$f = \frac{1}{2\pi\sqrt{LC}}, \quad C = \frac{C_1C_2}{C_1+C_2} = \frac{0.005\times10^{-6}\times0.01\times10^{-6}}{0.005\times10^{-6}+0.01\times10^{-6}}$$

$$f = \frac{1}{2\pi\sqrt{100\times10^{-6}\times3.3\times10^{-9}}} \qquad \boxed{C = 3.3\,nF}$$

$$\boxed{f = 277\,KHZ}$$

CRYSTAL OSCILLATOR:-

Principle:-

→ The general LC oscillator suffers from frequency instability due to temperature effect & loss within LC elements

→ For low frequency physically large elements (LC) are required and it is difficult to obtain >10MHz frequency.

→ CRYSTAL OSCILLATOR works on the principle of Piezo-electric effect.

Application:-

→ Microphone.
→ Taperecorder
→ Loudspeaker (headset)

Operation:-

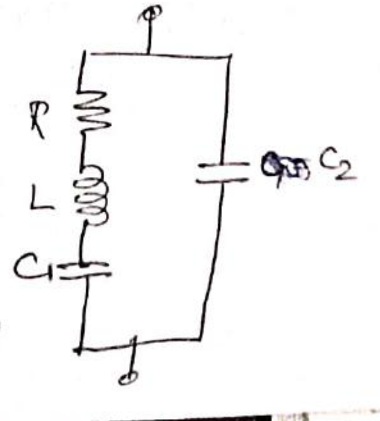
→ when AC voltage is applied crystal wafer vibrates, the frequency of vibration equal to resonant frequency of crystal.

COLPITTS CRYSTAL OSCILLATOR:-

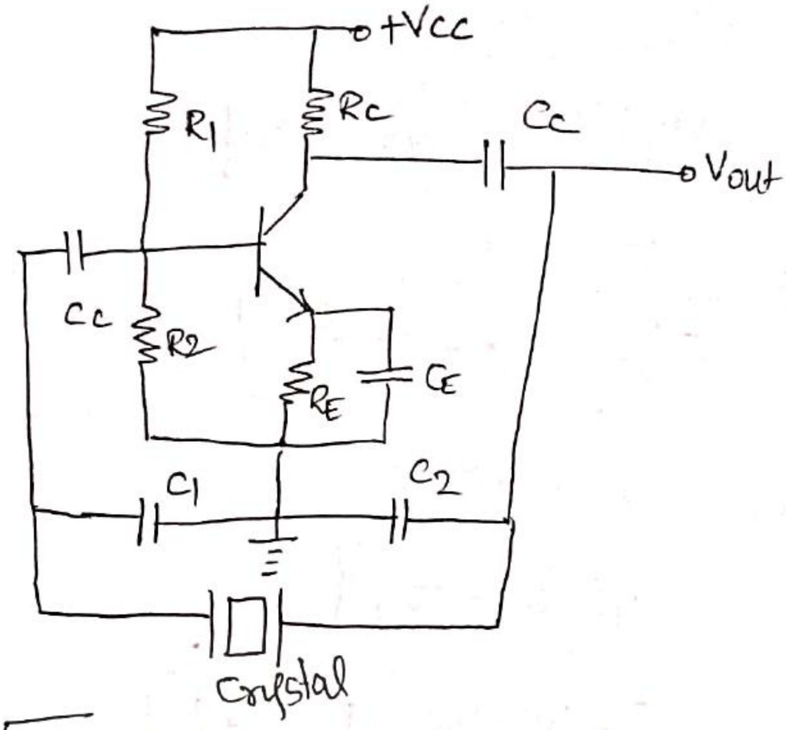
→ In Colpitts oscillator inductor is replaced by crystal to make colpitts crystal oscillator. In this type, a piezo-electric crystal usually quartz, is used as resonant ckt replaced on LC circuit.

Frequency of oscillation:-

Consider the equivalent ckt,



where, C_m → mounting capacitance.
R → internal frictionlessloss
L → Mass of crystal indicated by inertia



$$f = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}} \qquad \boxed{Q = \frac{L\omega}{R}}$$

From equivalent ckt,

$$Z = \left(j\omega L + \frac{1}{j\omega C_1}\right) \parallel \frac{1}{j\omega C_2}$$

$$= \frac{\left(j\omega L + \frac{1}{j\omega C_1}\right)\left(\frac{1}{j\omega C_2}\right)}{j\omega L + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}}$$

$$= \frac{\frac{j\omega L}{j\omega C_2} + \frac{1}{j^2\omega^2 C_1 C_2}}{j\omega L + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2}} \qquad j^2 = -1$$

$$Z = \frac{\left(\frac{L}{C_2} - \frac{1}{\omega^2 C_1 C_2}\right)}{j\omega\left[L - \frac{1}{\omega^2 C_1} - \frac{1}{\omega^2 C_2}\right]}$$

$$= \frac{1\left(L - \frac{1}{\omega^2 C_1}\right)}{C_2 j\omega\left[L - \frac{1}{\omega^2 C_1} - \frac{1}{\omega^2 C_2}\right]}$$

Taking LCM,

$$Z = \frac{(\omega^2 C_1 L - 1)}{\omega^2 C_1 \times C_2 j\omega\left[L - \frac{1}{\omega^2 C_1} - \frac{1}{\omega^2 C_2}\right]}$$

$$Z = \frac{\omega^2 C_1 L - 1}{C_2 j\omega\left[\omega^2 C_1 L - \frac{\omega^2 C_1}{\omega^2 C_1} - \frac{\omega^2 C_1}{\omega^2 C_2}\right]}$$

$$= \frac{\omega^2 C_1 L - 1}{C_2 j\omega\left[\omega^2 C_1 L - 1 - \frac{C_1}{C_2}\right]}.$$

Taking C_1L outside.

$$= \frac{C_1L\left[\omega^2 - \frac{1}{C_1L}\right]}{C_1L\, j\omega C_2\left[\omega^2 - \frac{1}{C_1L} - \frac{C_1}{C_2 C_1 L}\right]} \Rightarrow \frac{\cancel{C_1L}\left[\omega^2 - \frac{1}{C_1L}\right]}{\cancel{C_1L}\, j\omega C_2\left[\omega^2 - \frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right]}$$

$$\omega_s^2 = \frac{1}{LC_1}$$

$$\omega_p^2 = \frac{1}{L}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)$$

$$\therefore \boxed{Z = \frac{\omega^2 - \omega_s^2}{j\omega C_2(\omega^2 - \omega_p^2)}}$$

Advantage:-

→ very high Q as a resonant circuit which results in good frequency stability for the oscillator.

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Problem

1) A crystal has $L = 0.03H$, $C = 0.065pF$, $C_M = 1pF$ with $R = 5.5K\Omega$ find,

* Series Resonant frequency.
* Parallel resonant frequency.
* By what percent does the Parallel resonant frequency exceed the series resonant frequency?
* Find the Q-factor of circuit.

*) $f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.33 \times 0.0625 \times 10^{-12}}}$

$= 1.087 \text{ MHZ}.$

*) $C_{eq} = \frac{CC_M}{C + C_M} = \frac{0.065 \times 1}{0.065 + 1} = 0.061 \text{ PF}.$

$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{0.33 \times 0.061 \times 10^{-12}}} = 1.121 \text{MHZ}.$

* ~~fp~~ % increase $\Rightarrow \frac{1.121 - 1.087}{1.087} \times 100 = 3.127\%.$

* $Q = \frac{\omega_s L}{R} = \frac{2\pi f_s L}{R} = \frac{2\pi \times 1.087 \times 10^6 \times 0.33}{5.5 \times 10^3}$

$= 409.789.$

2) A Quartz crystal has $L = 3H$, $C_S = 0.05PF$, $R = 2000\Omega$ & $C_M = 10PF$. Calculate series & Parallel resonant frequencies f_s & f_p.

i) $f_s = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{3 \times 0.05 \times 10^{-12}}}$

$\boxed{f_s = 410.936 \text{KHZ}}$

ii) $C_{eq} = \frac{C_M C}{C_M + C} = \frac{10 \times 10^{-12} \times 0.05 \times 10^{-12}}{10 \times 10^{-12} + 0.05 \times 10^{-12}} = 4.9751 \times 10^{-14} F.$

iii) $f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{3 \times 4.975 \times 10^{-14}}} = 411.962 \text{KHZ}$